1990 Data Book

High Performance Analog Integrated Circuits
for
ATE
Disk Drive
Instrumentation
Video
Military

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

1990 Data Book

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General Disclaimer

Specifications contained in this databook are current as of the publication date shown. Each datasheet is a controlled document. Current revisions, if any, to these specifications are maintained at the factory and are available upon request. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement. Proprietary devices have patents pending.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Today's customer demands higher performance products with improved quality and higher reliability. They also require superior service and reasonable prices. Elantec, founded in 1983, set its mission to become a major supplier to the high performance analog market by providing superior performance, outstanding quality and service at competitive prices.

Elantec products serve a wide variety of applications in diverse commercial, industrial and military markets. Applications that include video processing and distribution, high resolution graphics, Automatic Test Equipment (ATE), medical monitoring and diagnostic equipment, Local Area Networks (LANs), disk drives, military guidance and control systems, radar, Electronic Counter Measures (ECM), and satellites.

Elantec's commitment to high performance analog products presents a line up focused on high speed—devices ranging up to 1 GHz bandwidth and 7000 V/μs slew rate; and high output power—up to 5 amps and 70V. The product portfolio includes operational amplifiers, buffer amplifiers, current mode feedback amplifiers, voltage comparators and transistor arrays. In addition, Elantec provides high performance ASIC products for disk drives, ATE and video applications.

Manufacturing is performed at Elantec's factory in Milpitas. The wafer fabrication area is dedicated to high speed Complementary Bipolar processes. Extensive design, assembly and test capabilities are also located at the factory. All manufacturing capabilities are Mil certified and of the highest quality.

At Elantec, Quality and Reliability mean far more than rigorous quality control monitoring and reliability testing. We believe that quality and reliability must be "designed," rather than "tested" into our products. Our Quality and Reliability commitment begins with product conception and is carried through design, wafer fabrication, assembly, and testing to the final Quality Assurance acceptance inspection prior to shipment.

We also recognize that superior product performance and outstanding quality alone are not sufficient to satisfy the specialized needs of our customers, particularly in the dynamics of today's environment. Customer service is critical. Providing an extra measure of service in areas such as thoroughly specified and controlled datasheets, offering "customer specials"—non-standard electrical and mechanical processing for specific customer requirements, supporting space level processing options, providing accurate order status, predicting and avoiding potential problems, and assuring on-time deliveries.

Superior performance—outstanding quality and service—all at competitive prices—our mission to serve you.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EHA2400 Series
4 Channel Programmable Amp

Features
- Programmability
- Low offset voltage—4 mV (EHA2400A)
- High slew rate—30 V/μs
- Wide gain bandwidth—40 MHz
- High gain—150,000 V/V
- Low offset current—5 nA
- High input impedance—30 MΩ
- Low crosstalk— −110 dB
- Single capacitor compensation
- Short circuit protected output
- DTL/TTL/CMOS compatible digital inputs

Applications
- Analog signal selection/ multiplexing
- Op amp gain selection, P.G.A.
- Add-subtract functions
- Filter characteristic programmability
- Integrator characteristic selection
- Comparator level control
- Adjustable frequency oscillators

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EHA1-2400-2	−55°C to +125°C	CerDIP	MDP0021
EHA1-2400/883B	−55°C to +125°C	CerDIP	MDP0021
EHA1-2405-5	0°C to +75°C	CerDIP	MDP0021
EHA1-2400A-2	−55°C to +125°C	CerDIP	MDP0021
EHA1-2400A/883B	−55°C to +125°C	CerDIP	MDP0021
EHA1-2405A-5	0°C to +75°C	CerDIP	MDP0021

Truth Table

D1	D0	EN	Selected Channel
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None

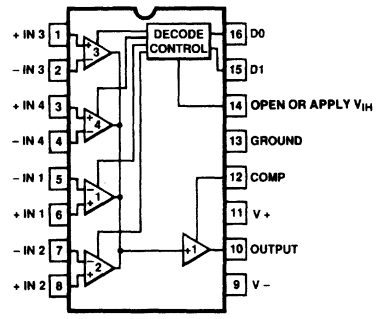
General Description

The EHA2400/2400A/2405/2405A is a series of versatile four-channel high-speed programmable monolithic amplifiers. They have four operational amplifier channels, any one of which may be electronically selected and connected to a single output stage through DTL/TTL/CMOS compatible address inputs. The device formed by the output and the selected pair of differential inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. For higher accuracy applications, the EHA2400A and EHA2405A have a tightened input offset voltage specification of 4 mV maximum. Other features of these Complementary Bipolar amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains of 10 or more, and all four channels of the device are compensated for unity gain with a single 15 pF capacitor. The compensation pin may also be used to limit the output swing through suitable clamping diodes. Elantec's careful design of the front end makes possible an "A" version with 4 mV maximum of input offset voltage.

Each channel of the EHA2400/2400A/2405/2405A can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This ability makes these amplifiers excellent components for multiplexing, signal selection, mathematical function designs, signal generators, active filters, and data acquisition designs.

Elantec's EHA2400/883B and EHA2400A/883B comply with MIL-STD-883 Revision C in all aspects. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing-Monolithic Products.*

Connection Diagram



2400-1

Absolute Maximum Ratings

Voltage between V+ and V−	45V	T_A	Operating Temperature Range
Differential Input Voltage	±V Supply		EHA2400A, EHA2400 $-55°C \le T_A \le +125°C$
Output Current	Short Circuit Protected		EHA2405A, EHA2405 $0°C \le T_A \le +75°C$
Internal Power Dissipation	(See Curves)		Storage Temperature Range $-65°C \le T_A \le +150°C$
			Maximum Junction Temperature 175°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 2 kΩ, unless otherwise specified.

V_{IL} +0.5V, V_{IH} = +2.4V, limits apply to each of the four channels, when addressed.

Parameter	Description	Test Conditions	Temp	EHA2400/A				EHA2405/A				Units
				Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	(EHA2400A/ EHA2405A)*	25°C		0.5	4*	I		0.5	4*	I	mV
			Full			6*	I			6*	III	mV
V_{OS}	Offset Voltage	(EHA2400/ EHA2405)	25°C		4	9	I		4	9	I	mV
			Full			11	I			11	III	mV
I_B	Bias Current (Note 1)		25°C		50	200	I		50	250	I	nA
			Full			400	I			500	III	nA
I_{OS}	Offset Current (Note 1)		25°C		5	50	I		5	50	I	nA
			Full			100	I			100	III	nA
R_{IN}	Input Resistance (Note 1)		25°C		30		V		30		V	MΩ
V_{CM}	Common Mode Range		Full	±9			I	±9			II	V
A_V	Large Signal Voltage Gain (Note 2)		±25°C	50k	150k		I	50k	150k		I	V/V
			Full	25k			I	25k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)		Full	80	100		I	74	100		II	dB
V_O	Output Voltage Swing		Full	±10	±12		I	±10	±12		II	V
I_O	Output Current (Note 2)		±25°C	±10	±20		I	±10	±20		I	mA
I_S	Supply Current		25°C		4.8	6.0	I		4.8	6.0	I	mA
PSRR	Power Supply Rejection Ratio (Note 5)		Full	74	90		I	74	90		II	dB

(* = Preliminary Specification)

EHA2400 Series
4 Channel Programmable Amp

Channel Select Characteristics

Parameter	Description	Test Conditions	Temp	EHA2400/A				EHA2405/A				Units
				Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
I_{INL}	Digital Input Current	V_{IN} = 0V	Full		0.1	1.5	I		0.1	1.5	II	mA
I_{INH}	Digital Input Current	V_{IN} = +5V	Full		5		V		5		V	nA
CT	Crosstalk (Note 7)		25°C	−80	−110		I	−74	−110		I	dB

AC Electrical Characteristics V_S = ±15V, R_L = 2 kΩ, unless otherwise specified.

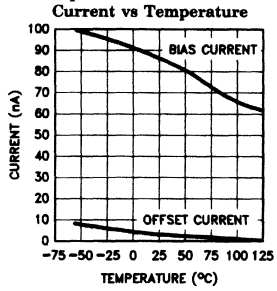
V_{IL} = +0.5V, V_{IH} = +2.4V, limits apply to each of the four channels, when addressed.

Parameter	Description	Test Conditions	Temp	EHA2400/A				EHA2405/A				Units
				Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
FPBW1	Full Power Bandwidth (Notes 2, 8, 9)		25°C	300	500		IV	300	500		IV	kHz
FPBW2	Full Power Bandwidth (Notes 2, 4, 9)		25°C	95	125		I	95	125		I	kHz
GBW1	Gain Bandwidth (Note 8)		25°C	20	40		IV	20	40		IV	MHz
GBW2	Gain Bandwidth (Note 4)		25°C	4	8		IV	4	8		IV	MHz
t_r1	Rise Time (Notes 4, 10)		25°C		20	45	I		20	50	I	ns
OS	Overshoot (Notes 4, 10)		25°C		25	40	I		25	40	I	%
SR1	Slew Rate (Notes 8, 11)		25°C	20	30		IV	20	30		IV	V/µs
SR2	Slew Rate (Notes 4, 11)		25°C	6	8		I	6	8		I	V/µs
t_s	Settling Time (Notes 4, 12)		25°C		1.5	2.5	IV		1.5	2.5	IV	µs
t_{sd}	Output Delay (Note 6)		25°C		100	250	IV		100	250	IV	ns

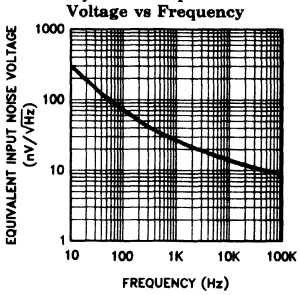
Note 1: Unselected channels have approximately the same input parameters.
Note 2: V_{OUT} = ±10V.
Note 3: Two tests are performed. V_{CM} = 0V to +5V and V_{CM} = 0V to −5V.
Note 4: A_V = +1, C_{COMP} = 15 pF, R_L = 2 kΩ, C_L = 50 pF.
Note 5: Two tests are performed. V+ = +15V, and V− is changed from −10V to −20V. V− = −15V, and V+ is changed from +10V to +20V.
Note 6: To 10% of final value; output then slews at normal rate to final value.
Note 7: Unselected input to output; V_{IN} = ±10V.
Note 8: A_V = +10, C_{COMP} = 0, R_L = 2 kΩ, C_L = 50 pF.
Note 9: Full power bandwidth based on slew rate measurement using: FPBW = SR/(2π V_P).
Note 10: V_{OUT} = ±200 mV.
Note 11: V_{OUT} = ±5V.
Note 12: To 0.1% of final value.

Typical Performance Curves

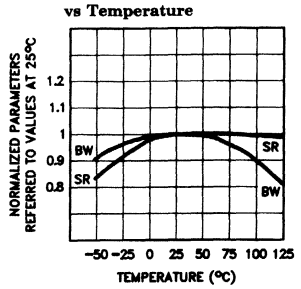
Input Bias and Offset Current vs Temperature



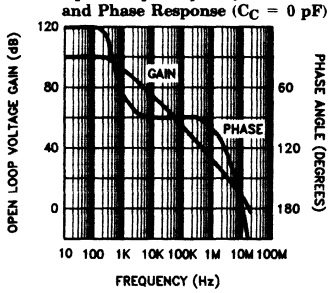
Equivalent Input Noise Voltage vs Frequency



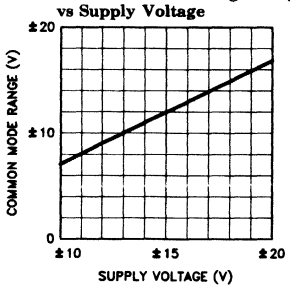
Normalized AC Parameters vs Temperature



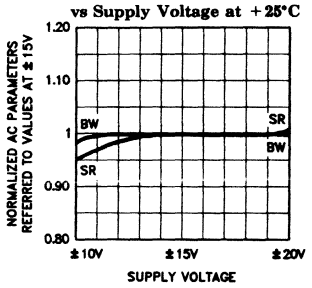
Open Loop Frequency and Phase Response (C_C = 0 pF)



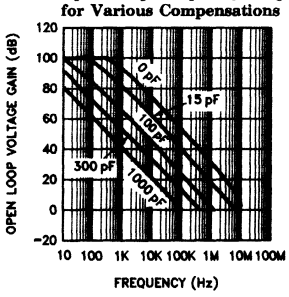
Common-Mode Voltage Range vs Supply Voltage



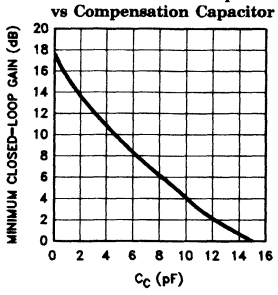
Normalized AC Parameters vs Supply Voltage at +25°C



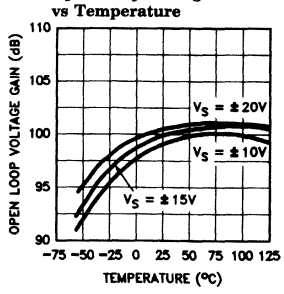
Open Loop Frequency Response for Various Compensations



Minimum Closed-Loop Gain vs Compensation Capacitor (C_C)



Open-Loop Voltage Gain vs Temperature



2400-2

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EHA2500 Series
High Slew Rate Operational Amplifier

Features
- High slew rate—100 V/μs
- Fast settling—200 ns
- Wide power bandwidth
- High input impedance
- Low offset current—25 nA
- Compensated versions available

Applications
- Data acquisition systems
- R.F. amplifiers
- Video amplifiers
- Signal generators
- Pulse amplification
- High speed sample and holds

General Description
Elantec's EHA2500 Series of monolithic high slew rate amplifiers is designed and optimized for high slew rates and wide bandwidths. Three different types are offered. The EHA250X series is unity gain stable and low cost. The EHA251X series has twice the bandwidth and slew rate of the EHA250X series and is also unity gain stable. For the best AC performance choose the EHA252X series which has the highest slew rate −120 V/μs—and the widest bandwidths available. The EHA252X series is stable with closed loop gains as low as three.

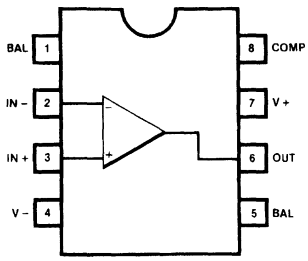
These devices are fabricated using Elantec's DInamic Dielectrically Isolated process that has excellent PNPs and NPNs that allow higher bandwidths than standard junction isolated process.

Elantec's high speed amplifiers are widely used in military, video and medical applications. They are especially suited for high speed video amplifiers, pulse detectors, and wide bandwidth filters.

Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

EHA3-, EHA7-



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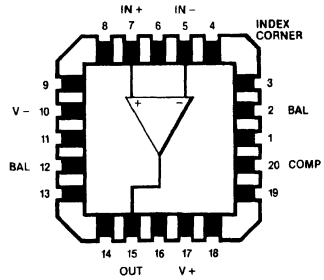
EHA4-



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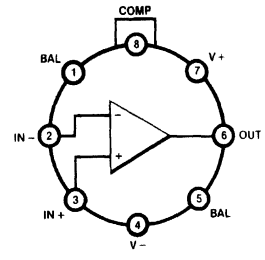
EHA2-



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Top Views

EHA2500 Series
High Slew Rate Operational Amplifier

Selection Guide

Part Number	Temp	V_{OS} (Max) mV	I_{BIAS} (Max) nA	I_{OS} (Max) nA	G_{BW} (Typ) MHz	PBW (Min) kHz	S_R (Min) V/μs	t_{SET} (Typ) μs	PSRR, CMRR (Min) dB	R_{IN} (Min) MΩ	Minimum Stable Gain
EHA2500	M	5	200	25	12	350	25	0.33	80	25	1
EHA2502	M	8	250	50	12	300	20	0.33	74	20	1
EHA2505	C	8	250	50	12	300	20	0.33	74	20	1
EHA2510	M	8	200	25	12	750	50	0.25	80	50	1
EHA2512	M	10	250	50	12	600	40	0.25	74	40	1
EHA2515	C	10	250	50	12	600	40	0.25	74	40	1
EHA2520	M	8	200	25	20	1500	100	0.20	80	50	3
EHA2522	M	10	250	50	20	1200	80	0.20	74	40	3
EHA2525	C	10	250	50	20	1200	80	0.20	74	40	3

Ordering Information

Dice (Note 1) (EHA0-)	14-Pin DIP Ceramic (EHA1-)	TO-99 Metal Can (EHA2-)	8-Pin DIP Plastic (EHA3-)	LCC 20-Pin (EHA4-)	8-Pin DIP CerDIP (EHA7-)
EHA0-2500-6		EHA2-2500/883B EHA2-2500-2			EHA7-2500/883B EHA7-2500-2
EHA0-2502-6		EHA2-2502/883B EHA2-2502-2			EHA7-2502/883B EHA7-2502-2
EHA0-2505-6		EHA2-2505-5	EHA3-2505-5		EHA7-2505-5
EHA0-2510-6		EHA2-2510/883B EHA2-2510-2			EHA7-2510/883B EHA7-2510-2
EHA0-2512-6		EHA2-2512/883B EHA2-2512-2			EHA7-2512/883B EHA7-2512-2
EHA0-2515-6		EHA2-2515-5	EHA3-2515-5		EHA7-2515-5
EHA0-2520-6	(Note 2)	EHA2-2520/883B EHA2-2520-2		EHA4-2520/883B	EHA7-2520/883B EHA7-2520-2
EHA0-2522-6		EHA2-2522/883B EHA2-2522-2			EHA7-2522/883B EHA7-2522-2
EHA0-2525-6		EHA2-2525-5	EHA3-2525-5		EHA7-2525-5

Note 1: Dice are available in waffle packs. Consult factory for more information.
Note 2: Consult factory for special packaging or temperature range requirements.

PREFIX		
EHA2–	TO-99 Metal Can	MDP0004
EHA3–	8-Pin Plastic DIP	MDP0031
EHA4–	Leadless Chip Carrier (LCC)	MDP0007
EHA7–	8-Pin CerDIP	MDP0010
EHA0–	Dice	

SUFFIX	
–1	0°C to +200°C
–2	–55°C to +125°C
–3	
–4	–25°C to +85°C
–5	0°C to +75°C
–6	100% 25°C Probe (Dice Only)
–7	
/883B	See Elantec's "Military Processing—Monolithic Products".
–9	

EHA2500 Series
High Slew Rate Operational Amplifier

Important Note:
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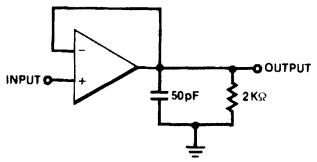
Test Level	*Test Procedure*
I	*100% production tested and QA sample tested per QA test plan QCX0002.*
II	*100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.*
III	*QA sample tested per QA test plan QCX0002.*
IV	*Parameter is guaranteed (but not tested) by Design and Characterization Data.*
V	*Parameter is typical value at T_A = 25°C for information purposes only.*

AC Test Circuits

EHA250X and EHA251X



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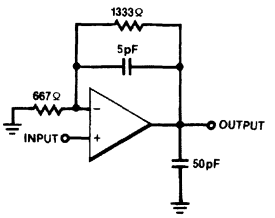
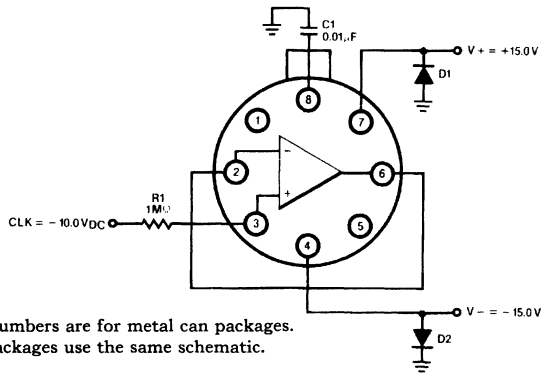
EHA252X



2500-5

Burn-In Circuit



Pin numbers are for metal can packages.
All packages use the same schematic.

2500-6

Top View

EHA2500/2502/2505
High Slew Rate Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage	±20V	T_A	Operating Temperature Range	
V_{IN}	Differential Input Voltage	±15V		EHA2500/02	−55°C to +125°C
P_D	Maximum Power Dissipation	See Curves		EHA2505	0°C to +75°C
I_{OP}	Peak Output Current	50 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified

Parameter	Description	Test Conditions	EHA2500				EHA2502				EHA2505				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_A = 25°C		2	5	I		4	8	I		4	8	I	mV
					8	I			10	I			10	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			20		V		20		V		20		V	µV/°C
I_B	Bias Current (Note 1)	T_A = 25°C		100	200	I		125	250	I		125	250	I	nA
					400	I			500	I			500	III	nA
I_{OS}	Offset Current	T_A = 25°C		10	25	I		20	50	I		20	50	I	nA
					50	I			100	I			100	III	nA
R_{IN}	Input Resistance	T_A = 25°C	25	50		IV	20	50		IV	20	50		IV	MΩ
V_{CMR}	Common-Mode Range		±10			I	±10			I	±10			II	V
CMRR	Common-Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	90		I	74	90		I	74	90		II	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	74	90		I	74	90		II	dB

EHA2500/2502/2505
High Slew Rate Operational Amplifier

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\ k\Omega$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	EHA2500				EHA2502				EHA2505				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
A_{VOL}	Large Signal Voltage Gain (Note 4)	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	20	30		I	15	25		I	15	25		I	V/mV
		$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$	15			I	10			I	10			III	V/mV
V_{OUT}	Output Voltage Swing	$R_L = 2\ k\Omega$	±10	±20		I	±10	±12		I	±10	±12		II	V
I_{OUT}	Output Current	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±20		I	±10	±20		I	±10	±20		I	mA
		$V_{OUT} = \pm 10V$	±7.5			I	±7.5			I	±7.5			III	mA
I_{CC}	Supply Current (Note 5)	$T_A = 25°C$		4	6	I		4	6	I		4	6	I	mA
					6.5	I			7	I			7	III	mA

AC Electrical Characteristics

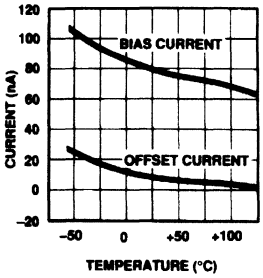
$V_S = \pm 15V$, $A_V = 1$, $R_S = 50\Omega$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$, $V_{OUT} = \pm 200\ mV$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (See AC test circuit)

Parameter	Description	Test Conditions	EHA2500				EHA2502				EHA2505				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r, t_f	Rise and Fall Times	$T_A = 25°C$		25	50	I		25	50	I		25	50	I	ns
					60	I			60	I			60	III	ns
SR	Slew Rate	$V_{OUT} = \pm 5V$, $T_A = 25°C$	±25	±30		I	±20	±30		I	±20	±30		I	V/μs
		$V_{OUT} = \pm 5V$	±20			I	±15			I	±15			III	V/μs
GBW	Gain Bandwidth Products	$A_V \ge 10$, $T_A = 25°C$		12		V		12		V		12		V	MHz
FPBW	Full Power Bandwidth (Note 6)	$V_{OUT} = \pm 10V$, $T_A = 25°C$	350	500		IV	300	500		IV	300	500		IV	kHz
O.S.	Overshoot	$T_A = 25°C$		25	40	I		25	50	I		25	50	I	%
					50	I			60	I			60	III	%
t_s	Settling Time to 0.1%	$V_{OUT} = \pm 5V$, $T_A = 25°C$		0.33		V		0.33		V		0.33		V	μs

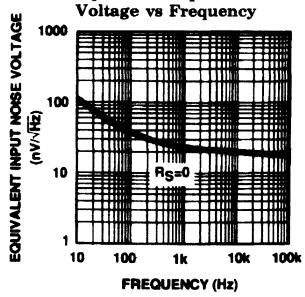
Note 1: Both input currents, I_{B+}, and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: PSRR+, V_{S+} = +10V to +20V with V_{S-} = −15V. For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL+}, V_{OUT} = 0V to +10V and for A_{VOL-}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply currents, I_{CC+}, and I_{CC-}, are tested.
Note 6: The Full Power Bandwidth is guaranteed by testing slew rate, FPBW = $SR/(2\pi V_P)$.

Typical Performance Curves

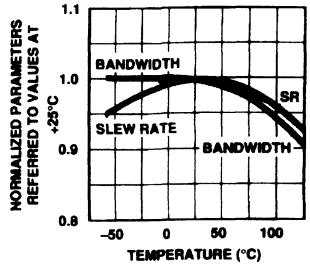
Input Bias and Offset Current vs Temperature



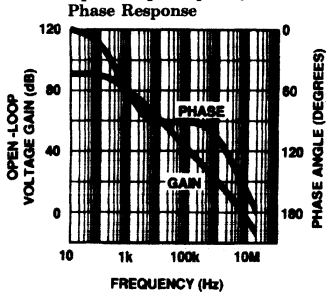
Equivalent Input Noise Voltage vs Frequency



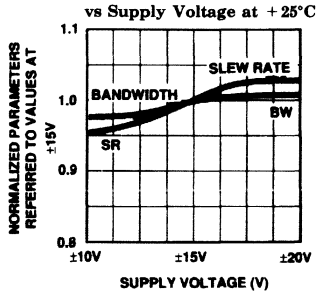
Normalized AC Parameters vs Temperature



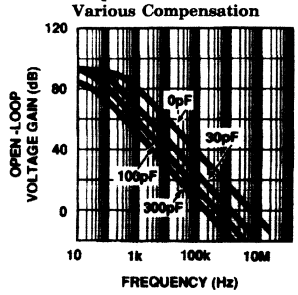
Open-Loop Frequency and Phase Response



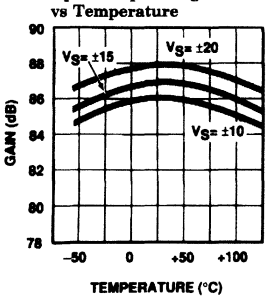
Normalized AC Parameters vs Supply Voltage at +25°C



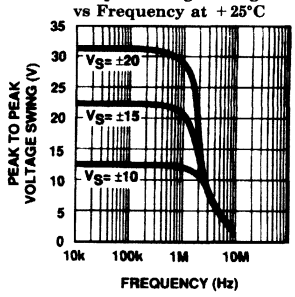
Open-Loop Frequency Response For Various Compensation



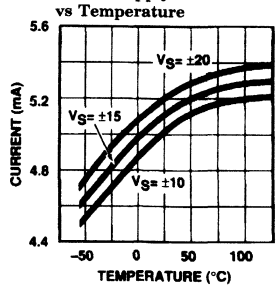
Open-Loop Voltage Gain vs Temperature



Output Voltage Swing vs Frequency at +25°C



Power Supply Current vs Temperature



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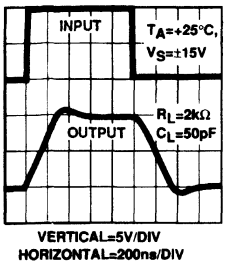
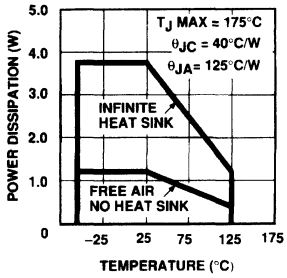
EHA2500/2502/2505
High Slew Rate Operational Amplifier

Typical Performance Curves — Contd.

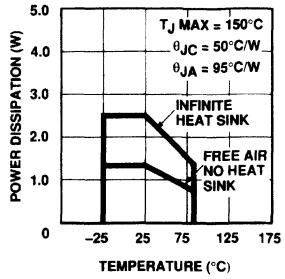
Voltage Follower
Pulse Response



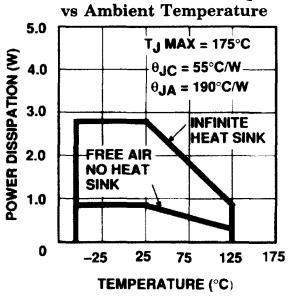
8-Lead CerDIP Maximum
Power Dissipation
vs Ambient Temperature



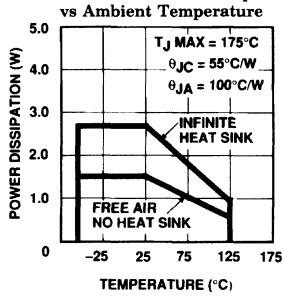
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



8-Lead TO-99 Metal Can
Maximum Power Dissipation
vs Ambient Temperature



20-Pad LCC
Maximum Power Dissipation
vs Ambient Temperature



2500–8

Absolute Maximum Ratings

V_S	Supply Voltage	±20V	T_A	Operating Temperature Range	
V_{IN}	Differential Input Voltage	±15V		EHA2510/12	−55°C to +125°C
P_D	Maximum Power Dissipation	See Curves		EHA2515	0°C to +75°C
I_{OP}	Peak Output Current	50 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified

Parameter	Description	Test Conditions	EHA2510				EHA2512				EHA2515				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_A = 25°C		4	8	I		5	10	I		5	10	I	mV
					10	I			14	I			14	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			20		V		25		V		30		V	µV/°C
I_B	Bias Current (Note 1)	T_A = 25°C		100	200	I		125	250	I		125	250	I	nA
					400	I			500	I			500	III	nA
I_{OS}	Offset Current	T_A = 25°C		10	25	I		20	50	I		20	50	I	nA
					50	I			100	I			100	III	nA
R_{IN}	Input Resistance	T_A = 25°C	50	100		IV	40	100		IV	40	100		IV	MΩ
V_{CMR}	Common-Mode Range		±10			I	±10			I	±10			II	V
CMRR	Common-Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	90		I	74	90		I	74	90		II	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	74	90		I	74	90		II	dB

EHA2510/2512/2515
High Slew Rate Operational Amplifier

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\ k\Omega$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	EHA2510				EHA2512				EHA2515				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
A_{VOL}	Large Signal Voltage Gain (Note 4)	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	10	15		I	7.5	15		I	7.5	15		I	V/mV
		$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$	7.5			I	5			I	5			III	V/mV
V_{OUT}	Output Voltage Swing	$R_L = 2\ k\Omega$	±10	±12		I	±10	±12		I	±10	±12		II	V
I_{OUT}	Output Current	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±20		I	±10	±20		I	±10	±20		I	mA
		$V_{OUT} = \pm 10V$	±7.5			I	±7.5			I	±7.5			III	mA
I_{CC}	Supply Current (Note 5)	$T_A = 25°C$		4	6	I		4	6	I		4	6	I	mA
					6.5	I			7	I			7	III	mA

AC Electrical Characteristics

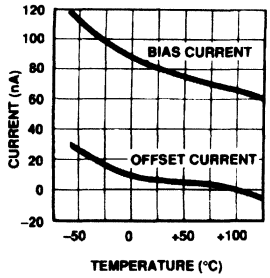
$V_S = \pm 15V$, $A_V = 1$, $R_S = 50\Omega$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$, $V_{OUT} = \pm 200\ mV$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (See AC test circuit)

Parameter	Description	Test Conditions	EHA2510				EHA2512				EHA2515				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r, t_f	Rise and Fall Times	$T_A = 25°C$		25	50	I		25	50	I		25	50	I	ns
					60	I			60	I			60	III	ns
SR	Slew Rate	$V_{OUT} = \pm 5V$, $T_A = 25°C$	±50	±65		I	±40	±60		I	±40	±60		I	V/μs
		$V_{OUT} = \pm 5V$	±45			I	±35			I	±35			III	V/μs
GBW	Gain Bandwidth Products	$A_V \geq 10$, $T_A = 25°C$		12		V		12		V		12		V	MHz
FPBW	Full Power Bandwidth (Note 6)	$V_{OUT} = \pm 10V$, $T_A = 25°C$	750	1000		IV	600	1000		IV	600	1000		IV	kHz
O.S.	Overshoot	$T_A = 25°C$		25	40	I		25	50	I		25	50	I	%
					50	I			60	I			60	III	%
t_s	Settling Time to 0.1%	$V_{OUT} = \pm 5V$		0.25		V		0.25		V		0.25		V	μs

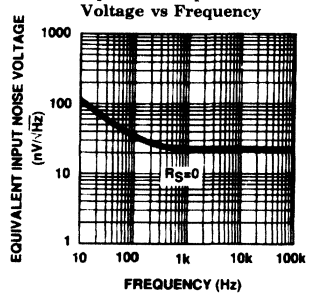
Note 1: Both input currents, I_{B+}, and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: PSRR+, V_{S+} = +10V to +20V with V_{S-} = −15V. For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL+}, V_{OUT} = 0V to +10V and for A_{VOL-}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply currents, I_{CC+}, and I_{CC-}, are tested.
Note 6: The Full Power Bandwidth is guaranteed by testing slew rate, FPBW = $SR/(2\pi V_P)$.

Typical Performance Curves

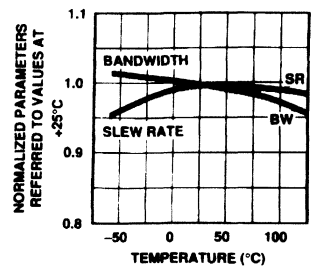
Input Bias and Offset Current vs Temperature



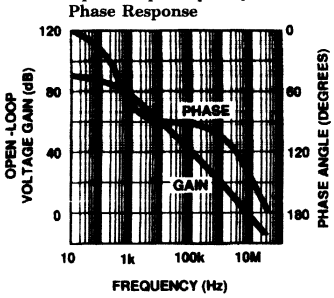
Equivalent Input Noise Voltage vs Frequency



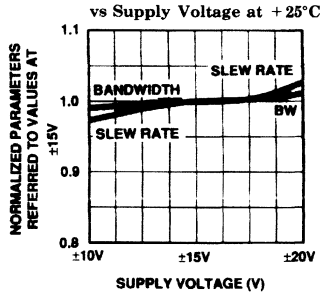
Normalized AC Parameters vs Temperature



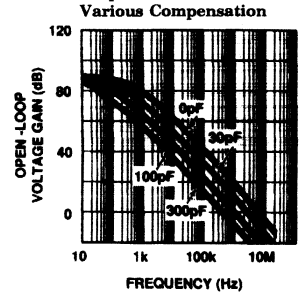
Open-Loop Frequency and Phase Response



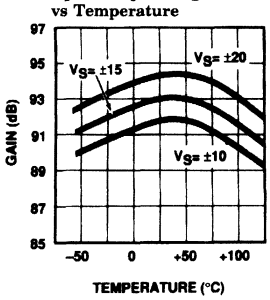
Normalized AC Parameters vs Supply Voltage at +25°C



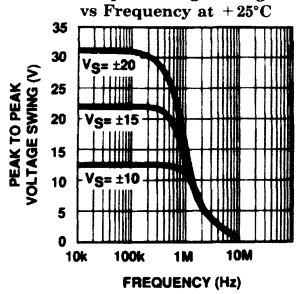
Open-Loop Frequency Response For Various Compensation



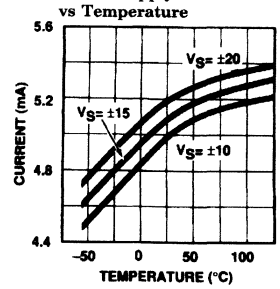
Open-Loop Voltage Gain vs Temperature



Output Voltage Swing vs Frequency at +25°C



Power Supply Current vs Temperature

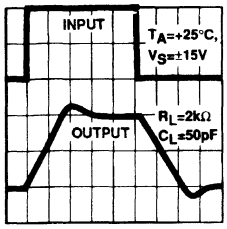


2500-9

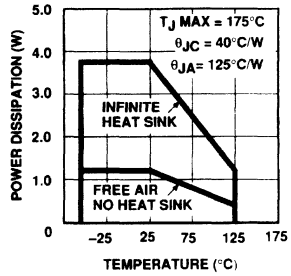
EHA2510/2512/2515
High Slew Rate Operational Amplifier

Typical Performance Curves — Contd.

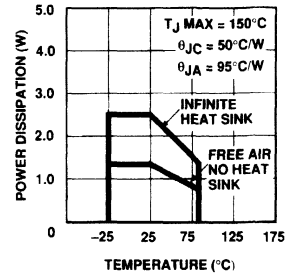
Voltage Follower
Pulse Response



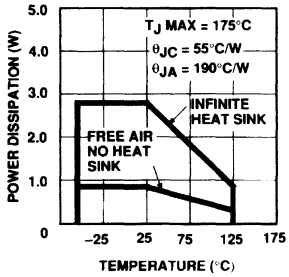
8-Lead CerDIP Maximum
Power Dissipation
vs Ambient Temperature



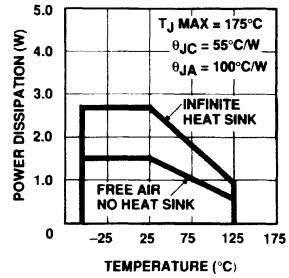
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



8-Lead TO-99 Metal Can
Maximum Power Dissipation
vs Ambient Temperature



20-Pad LCC
Maximum Power Dissipation
vs Ambient Temperature



2500-10

EHA2520/2522/2525
High Slew Rate Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage	±20V	T_A	Operating Temperature Range	
V_{IN}	Differential Input Voltage	±15V		EHA2520/22	−55°C to +125°C
P_D	Maximum Power Dissipation	See Curves		EHA2525	0°C to +75°C
I_{OUT}	Peak Output Current	50 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified

Parameter	Description	Test Conditions	EHA2520				EHA2522				EHA2525				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_A = 25°C		4	8	I		5	10	I		5	10	I	mV
					10	I			14	I			14	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			20		V		25		V		30		V	µV/°C
I_B	Bias Current (Note 1)	T_A = 25°C		100	200	I		125	250	I		125	250	I	nA
					400	I			500	I			500	III	nA
I_{OS}	Offset Current	T_A = 25°C		10	25	I		20	50	I		20	50	I	nA
					50	I			100	I			100	III	nA
R_{IN}	Input Resistance	T_A = 25°C	50	100		IV	40	100		IV	40	100		IV	MΩ
V_{CMR}	Common-Mode Range		±10			I	±10			I	±10			II	V
CMRR	Common-Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	90		I	74	90		I	74	90		II	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	74	90		I	74	90		II	dB

EHA2520/2522/2525
High Slew Rate Operational Amplifier

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\ k\Omega$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	EHA2520				EHA2522				EHA2525				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
A_{VOL}	Large Signal Voltage Gain (Note 4)	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	10	15		I	7.5	15		I	7.5	15		I	V/mV
		$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$	7.5			I	5			I	5			III	V/mV
V_{OUT}	Output Voltage Swing	$R_L = 2\ k\Omega$	±10	±12		I	±10	±12		I	±10	±12		II	V
I_{OUT}	Output Current	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±20		I	±10	±20		I	±10	±20		I	mA
		$V_{OUT} = \pm 10V$	±7.5			I	±7.5			I	±7.5			III	mA
I_{CC}	Supply Current (Note 5)	$T_A = 25°C$		4	6	I		4	6	I		4	6	I	mA
					6.5	I			7	I			7	III	mA

AC Electrical Characteristics

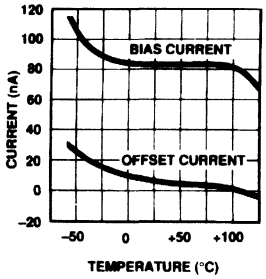
$V_S = \pm 15V$, $A_V = 3$, $R_S = 50\Omega$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$, $V_{OUT} = \pm 200\ mV$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (See AC test circuit)

Parameter	Description	Test Conditions	EHA2520				EHA2522				EHA2525				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r, t_f	Rise and Fall Times	$T_A = 25°C$		25	50	I		25	50	I		25	50	I	ns
					55	I			60	I			60	III	ns
SR	Slew Rate	$V_{OUT} = \pm 5V$, $T_A = 25°C$	±100	±120		I	±80	±120		I	±80	±120		I	V/μs
		$V_{OUT} = \pm 5V$	±84			I	±60			I	±60			III	V/μs
GBW	Gain Bandwidth Products	$A_V \ge 10$, $T_A = 25°C$	10	20		IV	10	20		IV	10	20		IV	MHz
FPBW	Full Power Bandwidth (Note 6)	$V_{OUT} = \pm 10V$, $T_A = 25°C$	1500	2000		IV	1200	1600		IV	1200	1600		IV	kHz
O.S.	Overshoot	$T_A = 25°C$		25	40	I		25	50	I		25	50	I	%
					45	I			60	I			60	III	%
t_s	Settling Time to 0.1%	$V_{OUT} = \pm 5V$, $T_A = 25°C$		0.20		V		0.20		V		0.20		V	μs

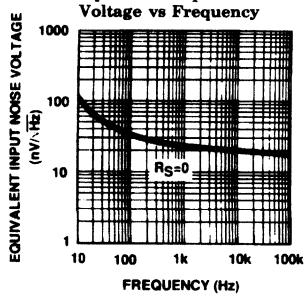
Note 1: Both input currents, I_{B+}, and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: PSRR+, V_{S+} = +10V to +20V with V_{S-} = −15V. For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For $A_{VOL}+$, V_{OUT} = 0V to +10V and for $A_{VOL}-$, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply currents, $I_{CC}+$, and $I_{CC}-$, are tested.
Note 6: The Full Power Bandwidth is guaranteed by testing slew rate, FPBW = $SR/(2\pi V_P)$.

Typical Performance Curves

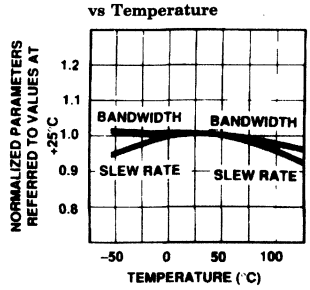
Input Bias and Offset Current vs Temperature



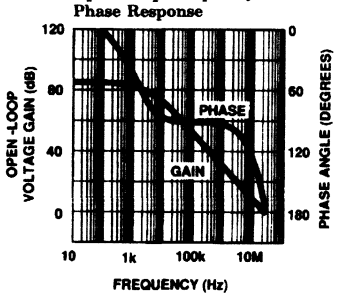
Equivalent Input Noise Voltage vs Frequency



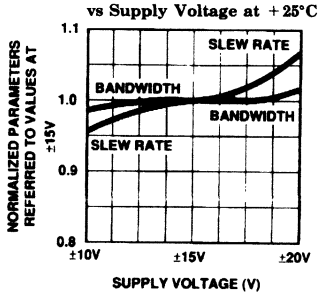
Normalized AC Parameters vs Temperature



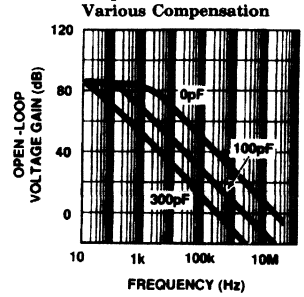
Open-Loop Frequency and Phase Response



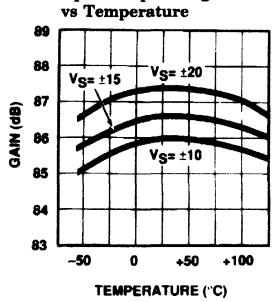
Normalized AC Parameters vs Supply Voltage at +25°C



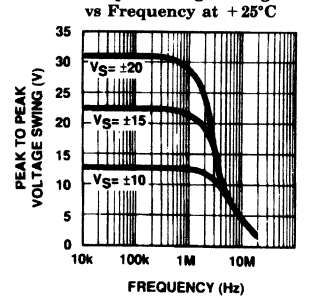
Open-Loop Frequency Response For Various Compensation



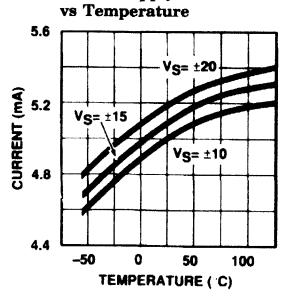
Open-Loop Voltage Gain vs Temperature



Output Voltage Swing vs Frequency at +25°C



Power Supply Current vs Temperature



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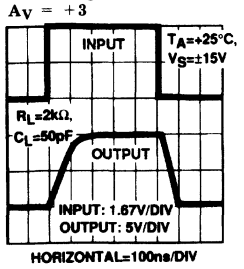
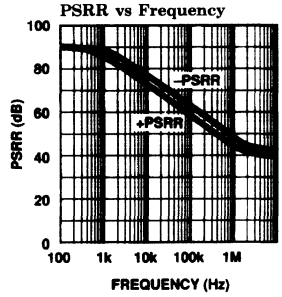
EHA2520/2522/2525
High Slew Rate Operational Amplifier

Typical Performance Curves — Contd.

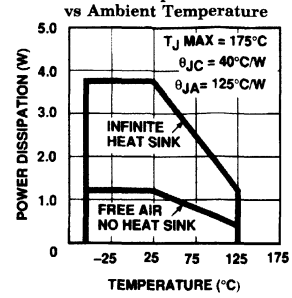
Pulse Response,
$A_V = +3$



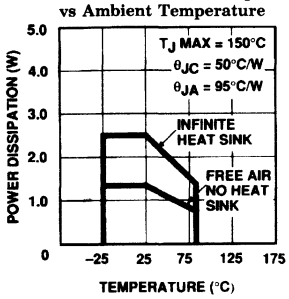
PSRR vs Frequency



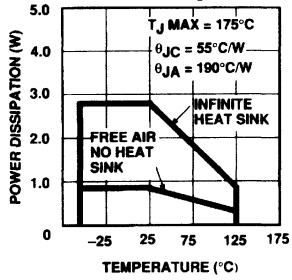
8-Lead CerDIP Maximum
Power Dissipation
vs Ambient Temperature



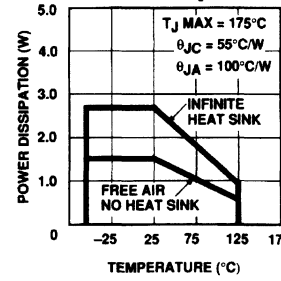
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



8-Lead TO-99 Metal Can
Maximum Power Dissipation
vs Ambient Temperature



20-Pad LCC
Maximum Power Dissipation
vs Ambient Temperature



2500-12

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EHA2600 Series

Wideband, High Impedance Operational Amplifier

Features

- High slew rates
- High input impedance—500 MΩ
- Low input bias currents—1 nA
- Low input offset current—1 nA
- High gain—> 100 dB
- Output short circuit protected
- Output clamp
- Low input offset voltage—500 μV

Applications

- Video amplifiers
- Precision comparators
- Pulse amplifiers
- DAC buffers
- High-speed sample and holds

General Description

Elantec's EHA2600 Series of high performance op amps is designed to offer designers high-speed amplifiers without sacrificing DC characteristics. These products are fabricated using Elantec's Complementary Bipolar processes.

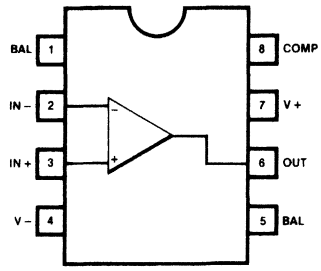
Two different versions are offered. The EHA260X series which is internally compensated and unity gain stable, and the EHA262X series that is optimized for slew rate and bandwidth.

These devices are used in a wide variety of applications including video signal conditioning, instrumentation, and data acquisition systems. For any application that requires high-speed AC and good DC performance to accurately process signals, the EHA2600 series provides excellent performance with over a 100 dB of gain, 1 nA of bias current and gain bandwidths to 100 MHz.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

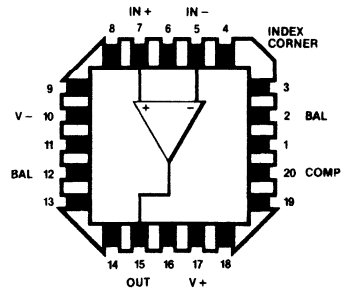
Connection Diagrams

EHA3-, EHA7-



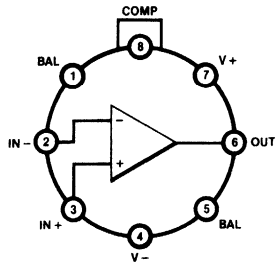
2600-1

EHA4-



2600-2

EHA2-



2600-3

Top Views

Note: Non-designated pins are no connects and are not electrically connected internally.

EHA2600 Series
Wideband, High Impedance Operational Amplifier

Selection Guide

Part Number	Temp	V_{OS} (Max) mV	I_{BIAS} (Max) nA	I_{OS} (Max) nA	G_{BW} (Typ) MHz	PBW (Min) kHz	S_R (Min) V/μs	t_{SET} (Typ) μs	PSRR, CMRR (Min) dB	R_{IN} (Min) MΩ	Minimum Stable Gain
EHA2600	M	4	10	10	12	50	4	1.5	80	100	1
EHA2602	M	5	25	25	12	50	4	1.5	74	40	1
EHA2605	C	5	25	25	12	50	4	1.5	74	40	1
EHA2620	M	4	15	15	100	400	25	—	80	65	5
EHA2622	M	5	25	25	100	320	20	—	74	40	5
EHA2625	C	5	25	25	100	320	20	—	74	40	5

Ordering Information

Dice (Note 1) (EHA0-)	14-Pin DIP Ceramic (EHA1-)	TO-99 Metal Can (EHA2-)	8-Pin DIP Plastic (EHA3-)	LCC 20-Pin (EHA4-)	8-Pin DIP CerDIP (EHA7-)
EHA0-2600-6		EHA2-2600/883B EHA2-2600-2 EHA2-2600-1 (Note 3)			EHA7-2600/883B EHA7-2600-2
EHA0-2602-6		EHA2-2602/883B EHA2-2602-2			EHA7-2602/883B EHA7-2602-2
EHA0-2605-6		EHA2-2605-5	EHA3-2605-5		EHA7-2605-5
EHA0-2620-6	(Note 2) (Note 2)	EHA2-2620/883B EHA2-2620-2 EHA2-2620-1 (Note 3)		EHA4-2620/883B	EHA7-2620/883B EHA7-2620-2
EHA0-2622-6	(Note 2) (Note 2)	EHA2-2622/883B EHA2-2622-2			EHA7-2622/883B EHA7-2622-2
EHA0-2625-6	(Note 2)	EHA2-2625-5	EHA3-2625-5		EHA7-2625-5

Note 1: Dice are available in waffle packs. Consult factory for more information.
Note 2: Consult factory for special packaging or temperature range requirements.
Note 3: Contact factory for minimum quantity and availability.

PREFIX	
EHA2–	TO-99 Metal Can MDP0004
EHA3–	8-Pin Plastic DIP MDP0031
EHA4–	Leadless Chip Carrier (LCC)..MDP0007
EHA7–	8-Pin CerDIP.....MDP0010
EHA0–	Dice

SUFFIX	
–1	0°C to +200°C
–2	–55°C to +125°C
–3	
–4	–25°C to +85°C
–5	0°C to +75°C
–6	100% 25°C Probe (Dice Only)
–7	
/883B	See Elantec's "Military Processing—Monolithic Products".
–9	

EHA2600/2602/2605
Wideband, High Impedance Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage	±22.5V	T_A	Operating Temperature Range	
V_{IN}	Differential Input Voltage	±12V		EHA2600/02	−55°C to +125°C
P_D	Maximum Power Dissipation	See Curves		EHA2605	0°C to +75°C
I_{OP}	Peak Output Current	Short Circuit Protected	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $C_L \leq 10$ pF, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified

Parameter	Description	Test Conditions	EHA2600				EHA2602				EHA2605				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_A = 25°C		0.5	4	I		3	5	I		3	5	I	mV
				2	6	I			7	I			7	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			5		V		5		V		5		V	µV/°C
I_B	Bias Current (Note 1)	T_A = 25°C		1	10	I		15	25	I		15	25	I	nA
				10	50	I			60	I			40	III	nA
I_{OS}	Offset Current	T_A = 25°C		1	10	I		5	25	I		5	25	I	nA
				5	50	I			60	I			40	III	nA
R_{IN}	Input Resistance	T_A = 25°C	100	500		IV	40	300		IV	40	300		IV	MΩ
V_{CMR}	Common-Mode Range		±11			IV	±11			IV	±11			IV	V
CMRR	Common-Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	100		I	74	100		I	74	100		II	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	74	90		I	74	90		II	dB
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_O = ±10V, T_A = 25°C	100	150		I	80	150		I	80	150		I	kV/V
		R_L = 2 kΩ, V_O = ±10V	70			I	60			I	70			III	kV/V
V_{OUT}	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	±10	±12		I	±10	±12		II	V

EHA2600/2602/2605
Wideband, High Impedance Operational Amplifier

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $C_L \leq$ 10 pF, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	EHA2600				EHA2602				EHA2605				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
I_{OUT}	Output Current	V_{OUT} = ±10V, T_A = 25°C	±15	±22		I	±10	±18		I	±10	±18		I	mA
		V_{OUT} = ±10V	±7.5			I	±7.5			I	±7.5			III	mA
I_{CC}	Supply Current (Note 5)	T_A = 25°C		3	3.7	I		3	4	I		3	4	I	mA

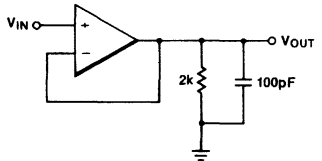
AC Electrical Characteristics

V_S = ±15V, R_L = 2 kΩ, C_L = 100 pF, V_{OUT} = ±200 mV, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (See AC test circuit)

Parameter	Description	Test Conditions	EHA2600				EHA2602				EHA2605				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r, t_f	Rise and Fall Times	T_A = 25°C		30	60	I		30	60	I		30	60	I	ns
					70	I			70	I			70	III	ns
SR	Slew Rate	V_{OUT} = ±5V, T_A = 25°C	±4	±7		I	±4	±7		I	±4	±7		I	V/μs
BW	Unity Gain Bandwidth (Note 6)	V_{OUT} < 90 mV, T_A = 25°C		12		V		12		V		12		V	MHz
FPBW	Full Power Bandwidth (Note 6)	V_{OUT} = ±10V, T_A = 25°C	50	75		IV	50	75		IV	50	75		IV	kHz
O.S.	Overshoot	T_A = 25°C		25	40	I		25	40	I		25	40	I	%
					50	I			50	I			50	III	%
t_s	Settling Time to 0.1%	V_{OUT} = ±5V, T_A = 25°C		1.5		V		1.5		V		1.5		V	μs

Note 1: Both input currents, I_{B+}, and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: PSRR+, V_{S+} = +10V to +20V with V_{S-} = −15V. For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For $A_{VOL}+$, V_{OUT} = 0V to +10V and for $A_{VOL}-$, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply currents, $I_{CC}+$, and $I_{CC}-$, are tested.
Note 6: The Full Power Bandwidth is guaranteed by testing slew rate, FPBW = SR/(2π V_P).

EHA260X A.C. Test Circuit



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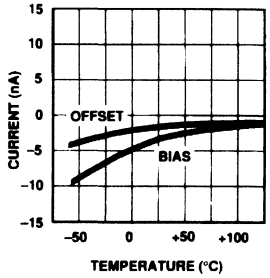
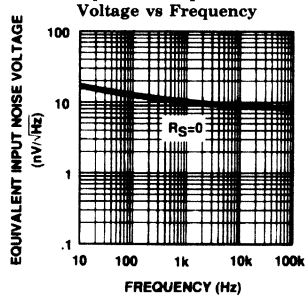
Typical Performance Curves

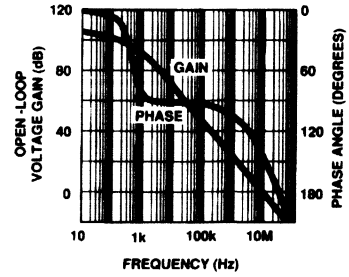
Input Bias Current and Offset Current as a Function of Temperature



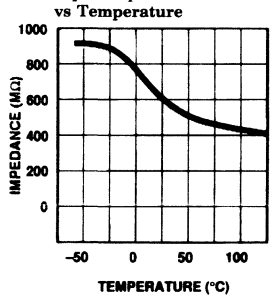
Equivalent Input Noise Voltage vs Frequency



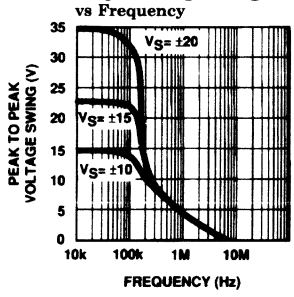
Open-Loop Frequency and Phase Response



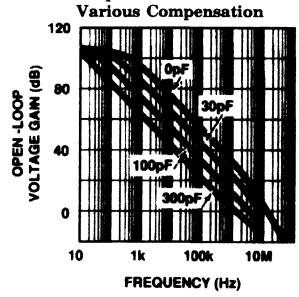
Input Impedance vs Temperature



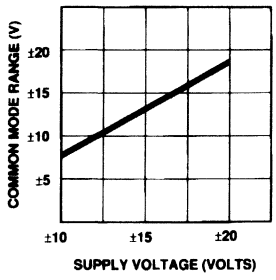
Output Voltage Swing vs Frequency



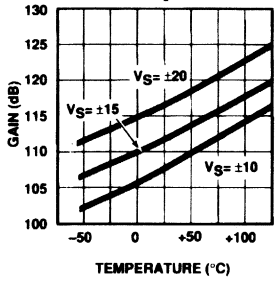
Open-Loop Frequency Response For Various Compensation



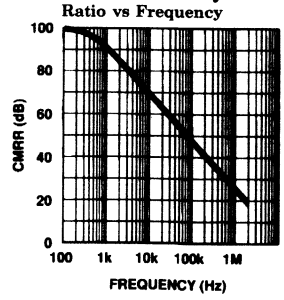
Common Mode Voltage Range as a Function of Supply Voltage



Open-Loop Voltage Gain vs Temperature



Common Mode Rejection Ratio vs Frequency



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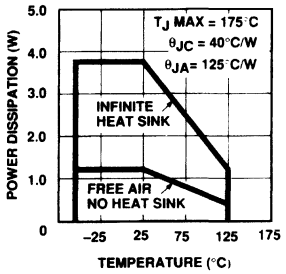
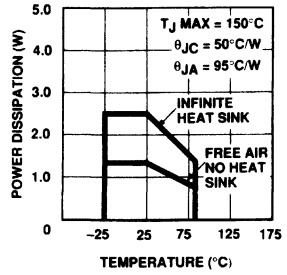
EHA2600/2602/2605
Wideband, High Impedance Operational Amplifier

Typical Performance Curves — Contd.

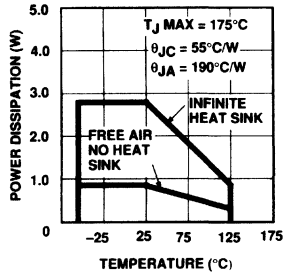
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



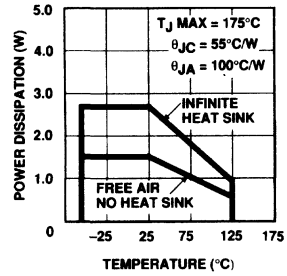
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



2600-6

EHA2620/2622/2625
Wideband, High Impedance Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage	±22.5V	T_A	Operating Temperature Range	
V_{IN}	Differential Input Voltage	±12.0V		EHA2620/22	−55°C to +125°C
P_D	Maximum Power Dissipation	See Curves		EHA2625	0°C to +75°C
I_{OP}	Peak Output Current	Short Circuit Protected	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified

Parameter	Description	Test Conditions	EHA2620				EHA2622				EHA2625				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_A = 25°C		0.5	4	I		3	5	I		3	5	I	mV
				2	6	I			7	I			7	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			5		V		5		V		5		V	µV/°C
I_B	Bias Current (Note 1)	T_A = 25°C		1	15	I		15	25	I		15	25	I	nA
				10	50	I			60	I			40	III	nA
I_{OS}	Offset Current	T_A = 25°C		1	15	I		5	25	I		5	25	I	nA
				5	50	I			60	I			40	III	nA
R_{IN}	Input Resistance	T_A = 25°C	65	500		IV	40	300		IV	40	300		IV	MΩ
V_{CMR}	Common-Mode Range		±11.0			IV	±11.0			IV	±11.0			IV	V
CMRR	Common-Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	100		I	74	100		I	74	100		II	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	74	90		I	74	90		II	dB

EHA2620/2622/2625
Wideband, High Impedance Operational Amplifier

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	EHA2620				EHA2622				EHA2625				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_O = ±10V, T_A = 25°C	100	150		I	80	150		I	80	150		I	kV/V
		R_L = 2 kΩ, V_O = ±10V	70			I	60			I	70			III	kV/V
V_O	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	±10	±12		I	±10	±12		II	V
I_{OUT}	Output Current	V_{OUT} = ±10V, T_A = 25°C	±15	±22		I	±10	±18		I	±10	±18		I	mA
		V_{OUT} = ±10V	±7.5			I	±7.5			I	±7.5			III	mA
I_{CC}	Supply Current (Note 5)	T_A = 25°C		3	3.7	I		3	4	I		3	4	I	mA

AC Electrical Characteristics

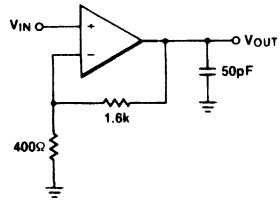
V_S = ±15V, R_S = 50Ω, R_L = 2 kΩ, C_L = 50 pF, V_{OUT} = ±200 mV, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified
(See AC test circuit)

Parameter	Description	Test Conditions	EHA2620				EHA2622				EHA2625				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r, t_f	Rise and Fall Times	A_V = 5V, T_A = 25°C		17	45	I		17	45	I		30	45	I	ns
		A_V = 5V			60	I			70	I			70	III	ns
SR	Slew Rate	V_{OUT} = ±5V, A_V = 5V, T_A = 25°C	±25	±35		I	±20	±35		I	±20	±35		I	V/μs
GBW	Gain Bandwidth Product	$V_O \le$ 90 mV, A_V = 100V T_A = 25°C		100		V		100		V		100		V	MHz
FPBW	Full Power Bandwidth (Note 6)	V_{OUT} = ±10V, T_A = 25°C	400	600		IV	320	600		IV	320	600		IV	kHz
O.S.	Overshoot	T_A = 25°C			60	I			60	I			60	I	%
					70	I			70	I			70	III	%

Note 1: Both input currents, I_{B+}, and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: PSRR+, V_{S+} = +10V to +20V with V_{S-} = −15V. For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For $A_{VOL}+$, V_{OUT} = 0V to +10V and for $A_{VOL}-$, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply currents, I_{CC+}, and I_{CC-} are tested.
Note 6: The Full Power Bandwidth is guaranteed by testing slew rate, FPBW = SR/(2π V_P).

AC Electrical Characteristics — Contd.

EH262X AC Test Circuit



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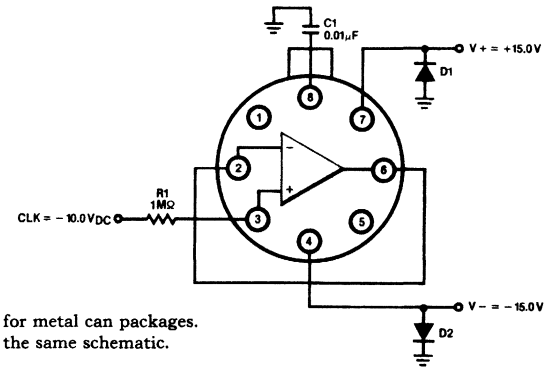
Burn-In Circuit



Pin numbers are for metal can packages.
All packages use the same schematic.

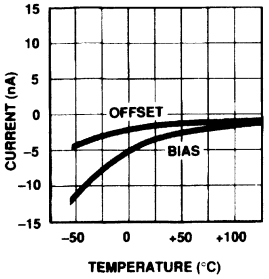
2600-8

Top View

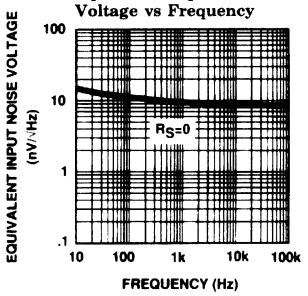
EHA2620/2622/2625
Wideband, High Impedance Operational Amplifier

Typical Performance Curves

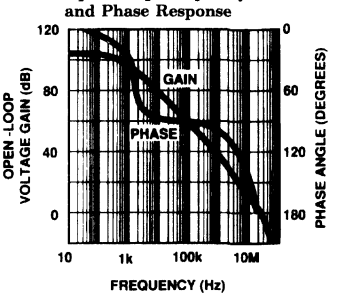
Input Bias Current and Offset Current as a Function of Temperature



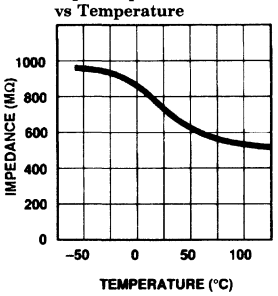
Equivalent Input Noise Voltage vs Frequency



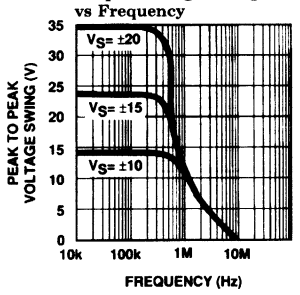
Open-Loop Frequency and Phase Response



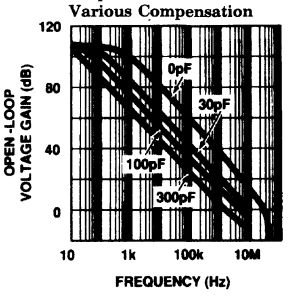
Input Impedance vs Temperature



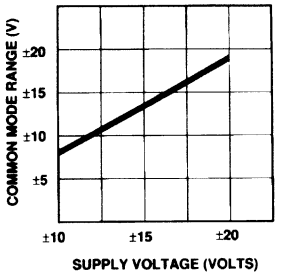
Output Voltage Swing vs Frequency



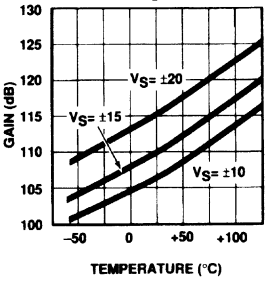
Open-Loop Frequency Response For Various Compensation



Common Mode Voltage Range as a Function of Supply Voltage



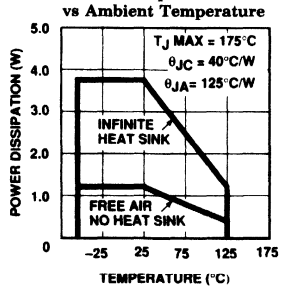
Open-Loop Voltage Gain vs Temperature



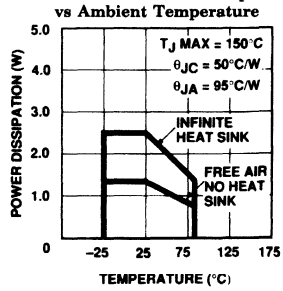
2600-9

Typical Performance Curves — Contd.

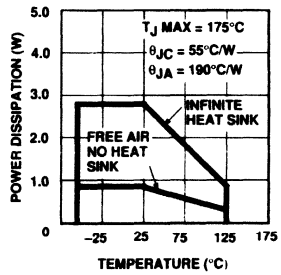
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



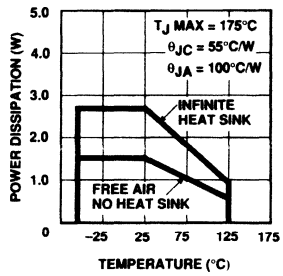
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



2600-10

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EHA5190/EHA5195

Wideband, Fast Settling Operational Amplifier

Features

- Very high slew rate—200 V/μs
- Wide gain-bandwidth—150 MHz
- Power bandwidth—6.5 MHz
- Fast settling—70 ns
- Low offset voltage—0.5 mV
- Input voltage noise—6 nV/$\sqrt{\text{Hz}}$
- Monolithic bipolar construction
- MIL-STD-883 Rev. C compliant
- Exact replacement for HA5190/5195

Applications

- Fast, precise D/A converters
- High speed sample-hold circuits
- Pulse and video amplifiers
- Wideband amplifiers
- Replace costly hybrid

Ordering Information

Part No.	Temp. Range	Package	Outline #
EHA1-5190-2	−55°C to +125°C	14-Pin CerDIP	MDP0014
EHA1-5190/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EHA2-5190-2	−55°C to +125°C	12-Pin TO-8	MDP0002
EHA2-5190/883B	−55°C to +125°C	12-Pin TO-8	MDP0002
EHA4-5190/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EHA1-5195-5	0°C to +75°C	14-Pin CerDIP	MDP0014
EHA2-5195-5	0°C to +75°C	12-Pin TO-8	MDP0002

General Description

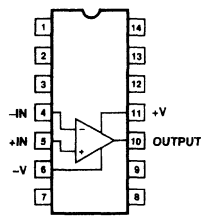
The Elantec EHA5190/EHA5195 are monolithic operational amplifiers featuring a combination of speed, precision, and bandwidth. Employing monolithic Complementary Bipolar construction, these devices are capable of delivering 200 V/μs slew rate with 70 ns settling times. These truly differential input operational amplifiers are designed to operate at gains ≥ 5 without the need for external compensation.

With a high Slew Rate and low settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample-hold circuits. 150 MHz gain-bandwidth product, 6.5 MHz power bandwidth, and 0.5 mV offset voltage all make the EHA5190/EHA5195 well suited for a variety of pulse and wideband video amplifier applications.

Elantec's EHA5190/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing Monolithic Products.*

Connection Diagrams

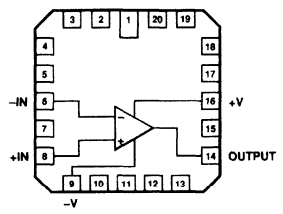
CerDIP Package



5190-1

Top View

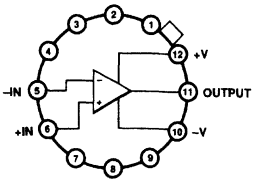
20-Lead LCC



5190-2

Top View

12-Lead TO-8



5190-3

Top View

Note: Case is tied to pin 10.

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EHA5190/EHA5195
Wideband, Fast Settling Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Operating Temperature Range	
Differential Input Voltage	6V	EHA5190	−55°C to +125°C
Output Current	50 mA (Peak)	EHA5195	0°C to +75°C
	30 mA (Continuous)	Operating Junction Temperature	
Internal Power Dissipation	See Curves	CerDIP, Ceramic LCC, TO-8	175°C
		Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 200Ω; unless otherwise specified

Parameter	Description	Temp	EHA5190				EHA5195				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	25°C		0.5	5	I		0.5	6	I	mV
		Full			10	I			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V		20		V	µV/°C
I_B	Bias Current	25°C		5	15	I		5	15	I	µA
		Full			20	I			20	III	µA
I_{OS}	Offset Current	25°C		1	4	I		1	4	I	µA
		Full			6	I			6	III	µA
R_{IN}	Input Resistance	25°C		10		V		10		V	kΩ
C_{IN}	Input Capacitance	25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±5	±10		I	±5	±10		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		6		V		6		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain	25°C	15k	30k		I	10k	30k		I	V/V
	(Notes 1, 2)	Full	5k			I	5k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	74	90		I	74	90		II	dB
V_O	Output Voltage Swing (Note 1)	Full	±5	±8		I	±5	±8		II	V

EHA5190/EHA5195
Wideband, Fast Settling Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 200\Omega$; unless otherwise specified — Contd.

Parameter	Description	Temp	EHA5190				EHA5195				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
I_O	Output Current (Note 1)	Full	±25	±40		I	±25	±40		II	mA
R_O	Output Resistance	25°C		30		V		30		V	Ω
I_S	Supply Current	Full		13	28	I		13	28	II	mA
PSRR	Power Supply Rejection Ratio (Note 8)	Full	70	80		I	70	80		II	dB

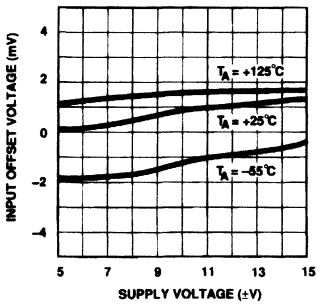
AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 200\Omega$; unless otherwise specified

Parameter	Description	Temp	EHA5190				EHA5195				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
GBW	Gain-Bandwidth Product (Notes 4, 5)	25°C		150		V		150		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 6)	25°C	5	6.5		I	5	6.5		I	MHz
t_r	Rise Time (Note 7)	25°C		7	18	IV		7	18	IV	ns
OS	Overshoot (Note 7)	25°C		25		V		25		V	%
SR	Slew Rate (Note 7)	25°C	160	200		I	160	200		I	V/μs
t_s	Settling Time (Notes 9, 10)										
	5V Step to 0.1%	25°C		50		V		50		V	ns
	5V Step to 0.05%	25°C		70		V		70		V	ns

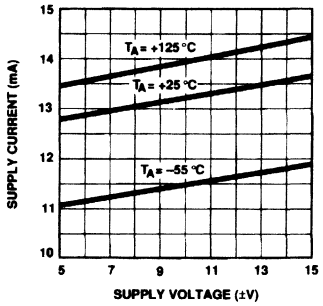
Note 1: $R_L = 200\Omega$, $C_L < 10$ pF, $V_O = \pm 5V$.
Note 2: $V_O = \pm 5V$.
Note 3: Two tests are performed. $V_{CM} = 0V$ to $-5V$ and $V_{CM} = 0V$ to $+5V$.
Note 4: $V_O = 90$ mV.
Note 5: $A_V = 10$.
Note 6: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi \text{ Vpeak}}$.
Note 7: Refer to Test Circuits section of data sheet.
Note 8: Two tests are performed. V+ = +15V, and V− is changed from −10V to −20V. V− = −15V and V+ is changed from +10V to +20V.
Note 9: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 10: $R_L = 1k$, $A_V = -5$.

Typical Performance Curves

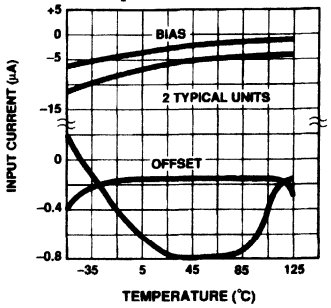
Input Offset Voltage vs Supply Voltage



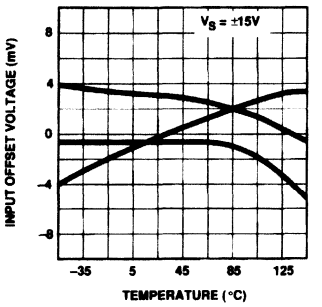
Supply Current vs Supply Voltage



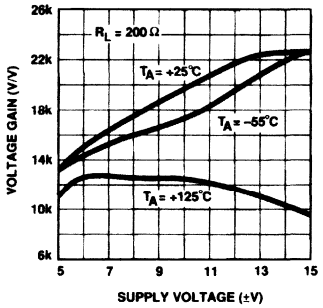
Input Currents vs Temperature



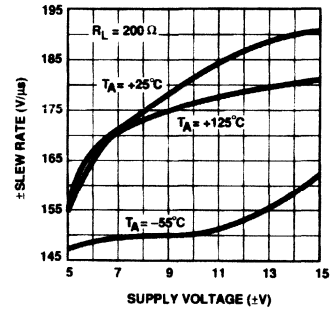
Input Offset Voltage vs Temperature (3 Typical units)



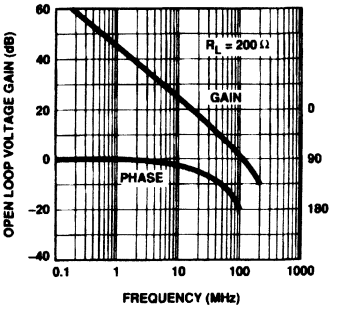
Voltage Gain vs Supply Voltage



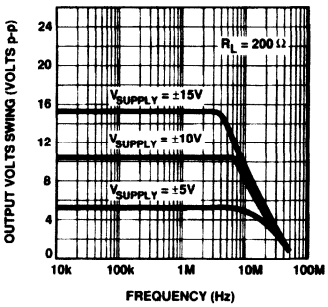
±Slew Rate vs Supply Voltage



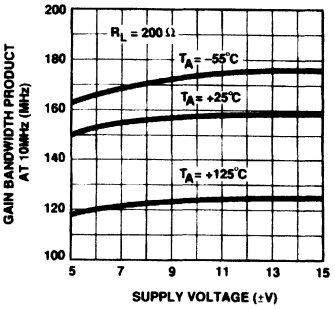
Open Loop Voltage Gain vs Frequency



Output Voltage Swing vs Frequency



Gain Bandwidth Product at 10 MHz vs Supply Voltage

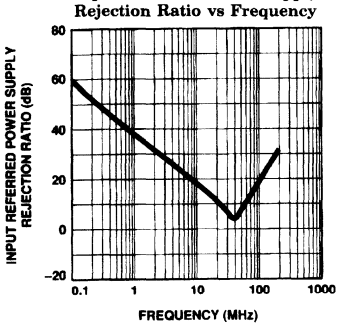


5190-4

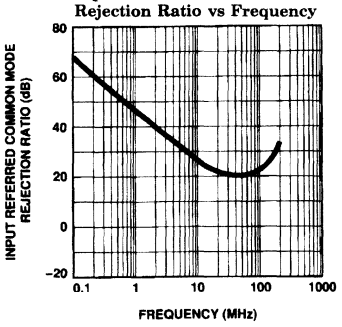
EHA5190/EHA5195
Wideband, Fast Settling Operational Amplifier

Typical Performance Curves — Contd.

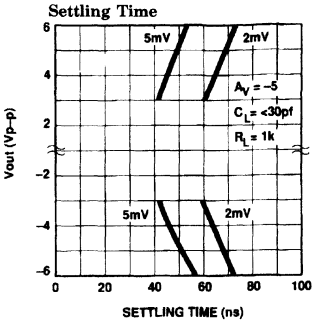
Input Referred Power Supply Rejection Ratio vs Frequency



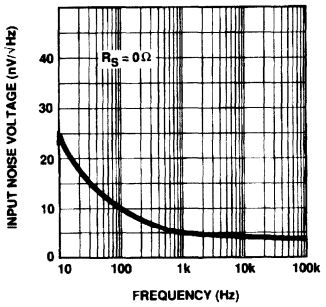
Input Referred Common Mode Rejection Ratio vs Frequency



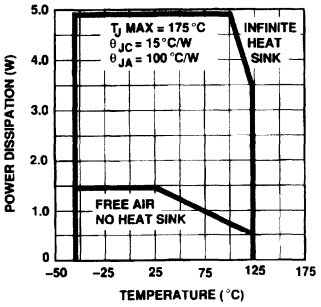
Settling Time



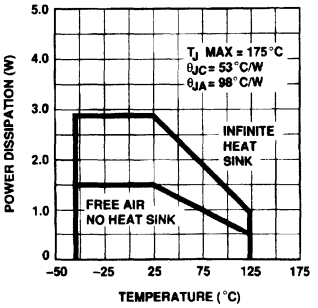
Input Noise Voltage vs Frequency



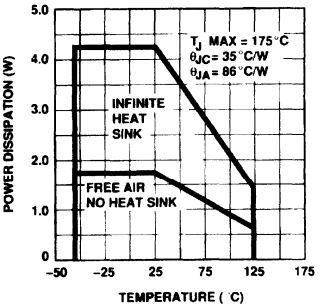
12-Lead TO-8 Maximum Power Dissipation vs Ambient Temperature



20-Lead LCC Maximum Power Dissipation vs Ambient Temperature



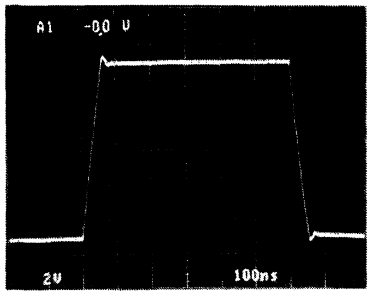
14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



5190-5

Typical Performance Curves — Contd.

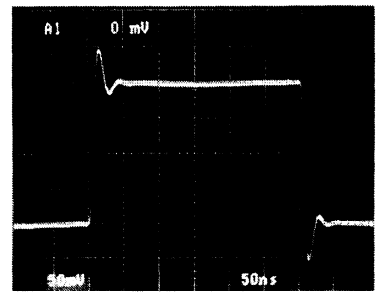
Large Signal Response



V_{IN} = ±1V
V_O = ±5V

5190-6

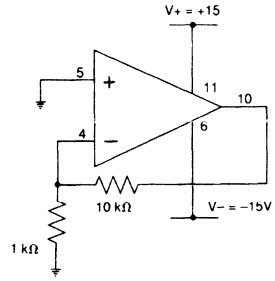
Small Signal Response



V_{IN} = ±20 mV
V_O = ±100 mV

5190-7

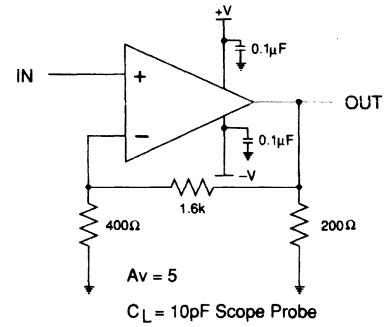
Burn-In Circuit



5190-8

Pin numbers are for 14-lead CerDIP. Burn-in circuit is identical for all package types.

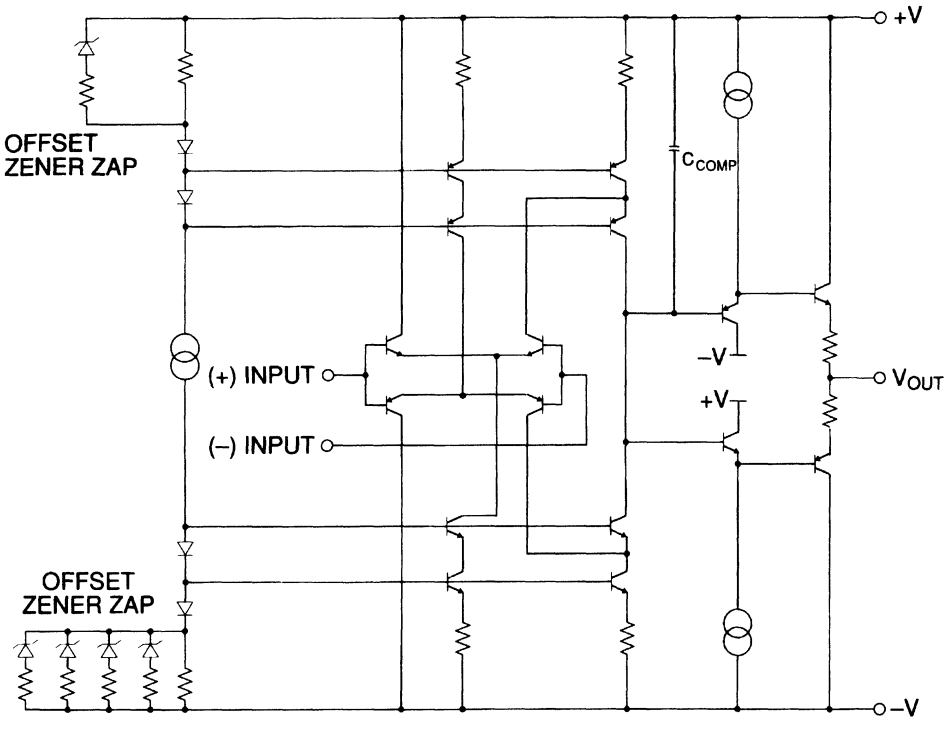
Test Circuit



5190-9

EHA5190/EHA5195
Wideband, Fast Settling Operational Amplifier

Schematic



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0032/ELH0032C
Fast Operational Amplifier

Features

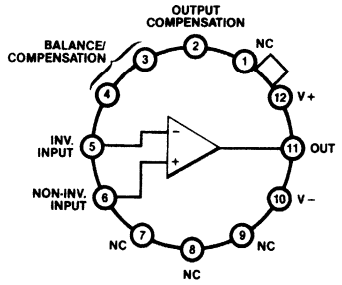
- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset nulls with single pot
- No compensation required for gains above 50
- Peak output current to 100 mA
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg. Outline #
ELH0032CG	−25°C to +85°C	TO-8 MDP0002
ELH0032G	−55°C to +125°C	TO-8 MDP0002
ELH0032G/883B	−55°C to +125°C	TO-8 MDP0002

8001301ZX is the DESC version of this device.

Connection Diagram



Top View

Case is electrically isolated.

Manufactured under U.S. Patent No. 4,746,877

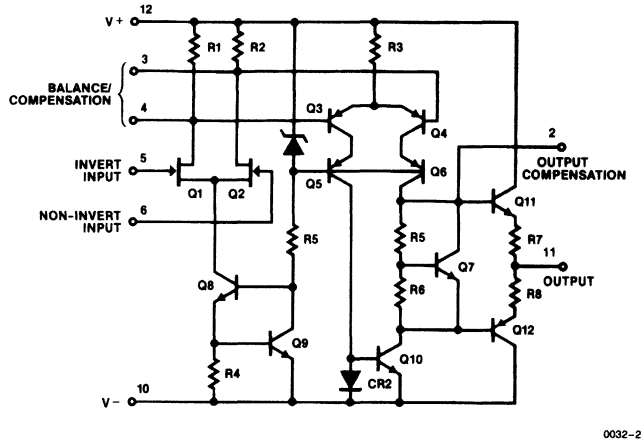
General Description

The ELH0032/ELH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability make the ELH0032/ELH0032C particularly suitable for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The ELH0032's wide bandwidth, high input impedance and high output drive capability make it an ideal choice for applications such as summing amplifiers in high-speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high-speed integrators and video amplifiers. The ELH0032 is guaranteed over the temperature range −55°C to +125°C and the ELH0032C is guaranteed from −25°C to +85°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Simplified Schematic



ELH0032/ELH0032C
Fast Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range:	
V_{IN}	Input Voltage	±15 V_S		ELH0032	−55°C to +125°C
	Differential Input Voltage	±30V or ±2 V_S		ELH0032C	−25°C to +85°C
P_D	Power Dissipation (Note 1)		T_J	Operating Junction Temperature	175°C
	T_A = 25°C 1.5W, derate 100°C/W to +125°C		T_{ST}	Storage Temperature	−65°C to +150°C
	T_C = 25°C 2.2W, derate 70°C/W to +125°C			Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, V_{IN} = 0V

Parameter	Description	Test Conditions	ELH0032				ELH0032C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage	T_J = 25°C (Note 2)		2	5	I		2	15	I	mV
					10	I			20	III	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift			25	150	I		25		V	µV/°C
I_{OS}	Input Offset Current	T_J = 25°C (Note 2)			25	I			50	I	pA
		T_A = 25°C (Note 3)			250	IV			500	IV	pA
		T_J = Max			25	I			5	III	nA
I_B	Input Bias Current	T_J = 25°C (Note 2)			100	I			500	I	pA
		T_A = 25°C (Note 3)			1	IV			5	IV	nA
		T_J = T_{MAX}			50	I			15	III	nA
V_{INCM}	Input Voltage Range		±10	±12		I	±10	±12		II	V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±10V	50	60		I	50	60		II	dB
A_{VOL}	Open-Loop Voltage Gain	V_O = ±10V, R_L = 1 kΩ, T_J = 25°C	48	60		I	48	60		I	dB
		V_O = ±10V, R_L = 1 kΩ	45			I	45			III	dB
		V_O = ±10V, f = 1 kHz, R_L = 1 kΩ, T_J = 25°C	60	70		I	60	70		I	dB
		V_O = ±10V, f = 1 kHz, R_L = 1 kΩ	57			I	57			III	dB

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$, $V_{IN} = 0V$ — Contd.

Parameter	Description	Test Conditions	ELH0032				ELH0032C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	$R_L = 1\ k\Omega$	± 10	± 13.5		I	± 10	± 13		II	V
I_S	Power Supply Current	$T_J = 25°C$, $I_O = 0$ mA		21	23	I		23	25	I	mA
		$T_A = 25°C$, $I_O = 0$ mA (Note 3)		18	20	IV		20	22	IV	mA
PSRR	Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq 15V$	50	60		I	50	60		II	dB
		$+5V \leq V_S(+) \leq +20V$, $V_S(-) = -15V$	50			I	50			II	dB
		$-5V \geq V_S(-) \geq -20V$, $V_S(+) = +15V$	50			I	50			II	dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$, $T_J = 25°C$

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
SR	Slew Rate	$A_V = +1$, $\Delta V_{IN} = 20V$	350	500		I	V/μs
t_S	Settling Time to 1% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$		100	500	IV	ns
t_S	Settling Time to 0.1% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$		300		V	ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$		8	20	I	ns
t_D	Small Signal Delay Time	$A_V = +1$, $\Delta V_{IN} = 1V$		10	25	I	ns

Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation.

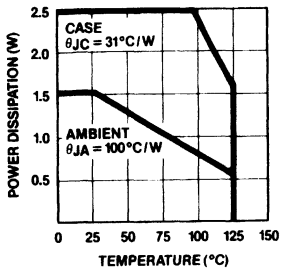
Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltage are $\pm 15V$, no-load operating junction temperature may rise 40°C–60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs temperature graph for expected values.

Note 3: Measured in still air 7 minutes after application of power.

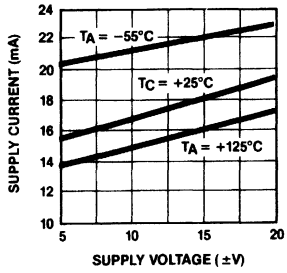
ELH0032/ELH0032C
Fast Operational Amplifier

Typical Performance Curves

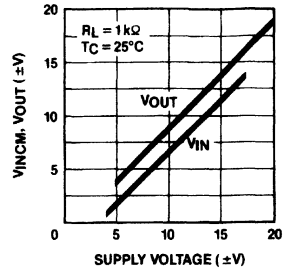
Maximum Power Dissipation



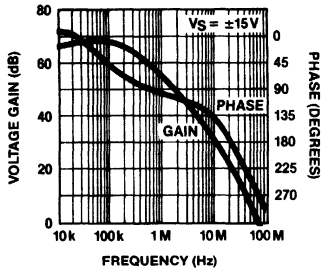
Supply Current vs Supply Voltage



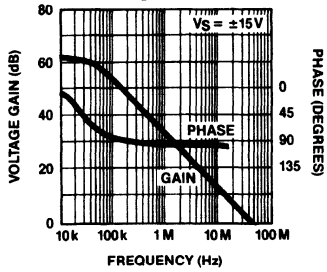
Input Voltage Range and Output Voltage vs Supply Voltage



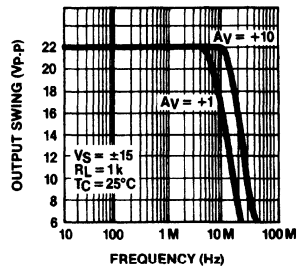
Bode Plot (Uncompensated)



Bode Plot (Unity Gain Compensation)



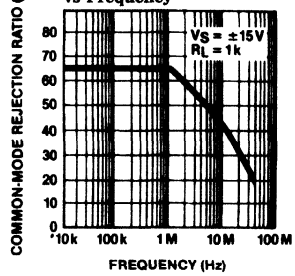
Large Signal Frequency Response



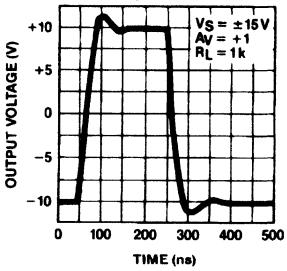
0032-3

Typical Performance Curves — Contd.

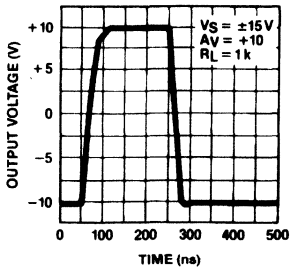
Common Mode Rejection Ratio vs Frequency



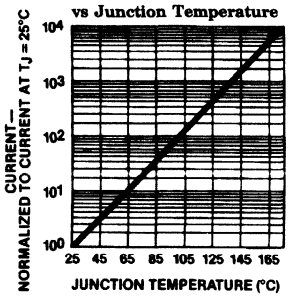
Large Signal Pulse Response



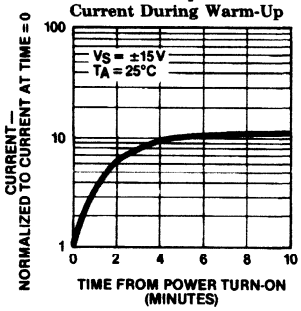
Large Signal Pulse Response



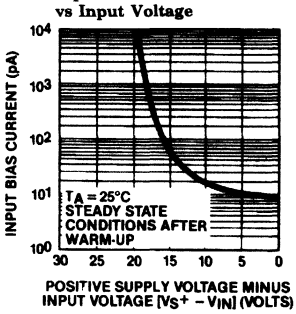
Normalized Input Bias and Offset Current vs Junction Temperature



Normalized Input Bias Current During Warm-Up

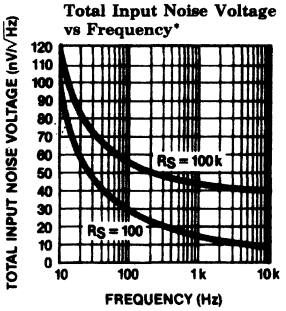


Input Bias Current vs Input Voltage



0032-4

Total Input Noise Voltage vs Frequency*

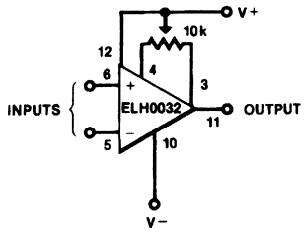


0032-5

*Noise voltage includes contribution from source resistance.

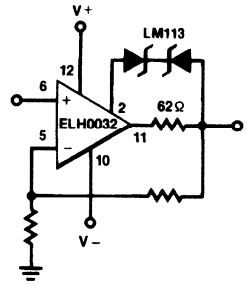
Auxiliary Circuits

Offset Null



0032-6

Output Short Circuit Protection

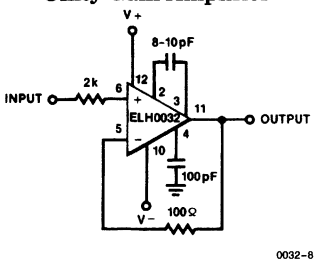


0032-7

ELH0032/ELH0032C
Fast Operational Amplifier

Typical Applications

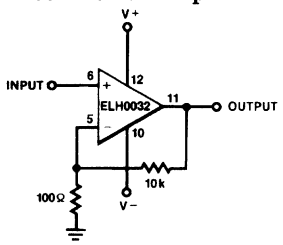
Unity Gain Amplifier



0032-8

TYP $BW_{3\ dB}$ = 45 MHz

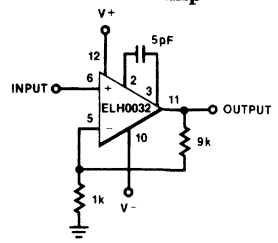
100X Buffer Amplifier



0032-9

TYP $BW_{3\ dB}$ = 10 MHz

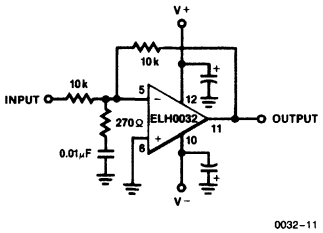
10X Buffer Amplifier



0032-10

TYP $BW_{3\ dB}$ = 5 MHz

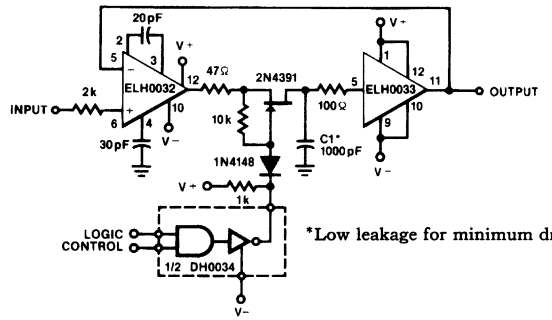
Non-Compensated Unity Gain Inverter



0032-11

TYP $BW_{3\ dB}$ = 70 MHz

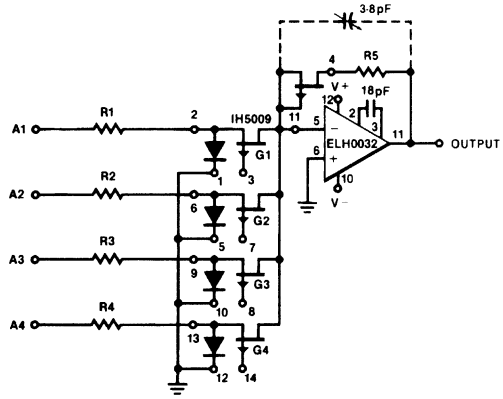
High-Speed Sample and Hold



*Low leakage for minimum drift

0032-12

High-Speed Current Mode MUX



0032-13

Applications Information

Power Supply Decoupling

The ELH0032/ELH0032C, like most high-speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power, thus raising the FET junction temperature 40°C–60°C above the free-air ambient temperature when supplies are $\pm$15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at the time will be indicative of normal operating currents. An additional rise will occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalance-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value, depending on FET geometry and doping levels. This effect will be noted as the input voltage of the ELH0032 is taken below ground potential when the supplies are $\pm$15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the ELH0032/ELH0032C is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

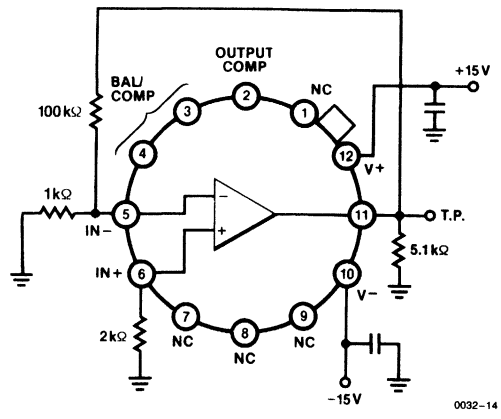
In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a 1 pF.

Heatsinking

While the ELH0032/ELH0032C is specified for operation without any explicit heatsink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

Burn-In Circuit

(Functional Diagram)



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2006/EL2006A
High Gain Fast FET Input Op Amp

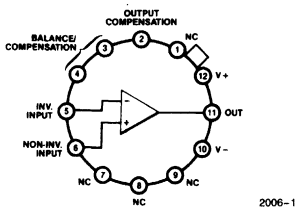
Features

- 90 dB open loop gain
- 450 V/μs slew rate
- 40 MHz bandwidth
- No thermal tail
- 3 mV max input offset voltage
- Offset nulls with single pot
- No compensation required for gains above 50
- Peak output current to 200 mA
- Pin compatible with LH0032
- 80 dB common mode rejection

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2006CG	−25°C to +85°C	TO-8	MDP0002
EL2006G	−55°C to +125°C	TO-8	MDP0002
EL2006G/883B	−55°C to +125°C	TO-8	MDP0002
EL2006ACG	−25°C to +85°C	TO-8	MDP0002
EL2006AG	−55°C to +125°C	TO-8	MDP0002
EL2006AG/883G	−55°C to +125°C	TO-8	MDP0002
EL2006L	−55°C to +125°C	52-Pad LCC	MDP0013
EL2006L/883B	−55°C to +125°C	52-Pad LCC	MDP0013

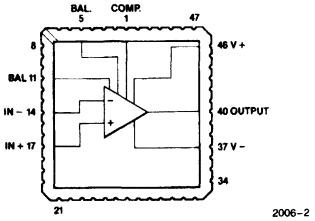
Connection Diagrams



2006-1

Top View

L Package



2006-2

Top View

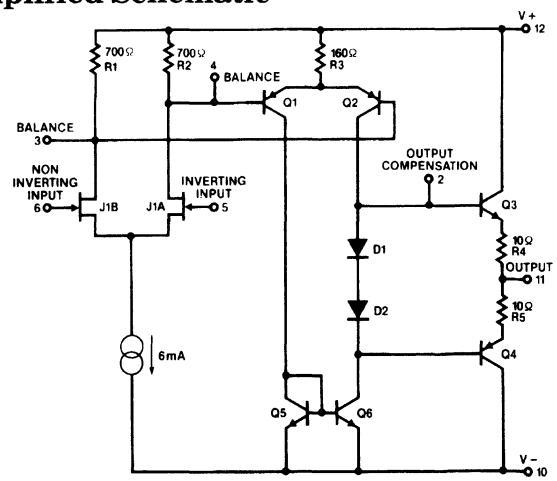
General Description

The EL2006/EL2006A are high slew rate, wide bandwidth, high input impedance, high gain and fully differential input operational amplifiers. They exhibit excellent open loop gain characteristics making them suitable for a broad range of high speed signal processing applications. These patented devices have open loop gains in excess of 86 dB making the EL2006/EL2006A ideal choices for current mode video bandwidth digital to analog converters of 10 bits or higher resolution. The EL2006's FET input structure, high slew rate, and high output drive capability allow use in applications such as buffers for flash converter inputs. In general, the EL2006/EL2006A allow the user to take relatively high closed loop gains without compromising gain accuracy or bandwidth.

The EL2006/EL2006A are pin compatible with the popular industry standard ELH0032/ELH0032A offering comparable bandwidth and slew rate, while offering significant improvements in open loop gain, common mode rejection and power supply rejection.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883 Class B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



2006-3

Manufactured under U.S. Patent No. 4,746,877

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	±15V		EL2006, EL2006A	−55°C to +125°C
	Differential Input Voltage	30V		EL2006C, EL2006AC	−25°C to +85°C
I_{OUT}	Peak Output Current (Note 1)	±200 mA	T_J	Operating Junction Temperature	175°C
P_D	Power Dissipation		T_{ST}	Storage Temperature	−65°C to +150°C
	T_A = 25°C 1.5W, derate 100°C/W to +125°C			Lead Temperature	
	T_C = 25°C 2.2W, derate 70°C/W to +125°C			(Soldering 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} < T_A < T_{MAX}$

Parameter	Description	Test Conditions	EL2006				EL2006C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_J = 25°C			5	I			5	I	mV
					10	I			10	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			15		V		15		V	µV/°C
I_B	Bias Current	T_J = 25°C			100	I			500	I	pA
				1	10	I		1	10	III	nA
I_{OS}	Offset Current	T_J = 25°C			25	I			50	I	pA
				0.2	2.5	I		0.2	2.5	III	nA
V_{CM}	Common Mode Range		±10			I	±10			II	V
CMRR	Common Mode Rejection Ratio	ΔV_{IN} = ±10V	70	80		I	70	80		II	dB
PSRR	Power Supply Rejection Ratio	±5V ≤ V_S ≤ ±15V	70	88		I	70	88		II	dB
A_{VOL}	Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10V, T_J = 25°C	86	90		I	80	90		I	dB
		R_L = 1 kΩ, V_{OUT} = ±10V	80			I	74			III	dB
V_O	Output Voltage Swing	R_L = 1 kΩ	±12			I	±12			II	V
I_{OUT}	Output Current	V_{OUT} = ±10V, T_J = 25°C, (Note 1)	±100			I	±100			I	mA
I_{CC}	Supply Current			20	23	I		20	23	II	mA

EL2006/EL2006A
High Gain Fast FET Input Op Amp

DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $T_{MIN} < T_A < T_{MAX}$ (Note: These tests are in addition to those listed above.)

Parameter	Description	Test Conditions	EL2006A				EL2006AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	$T_J = 25°C$			3	I			3	I	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			15	25	I		15	25	I	$\mu V/°C$
A_{VOL}	Large Signal Voltage Gain	$T_J = 25°C$, $R_L = 1\ k\Omega$, $V_{OUT} = \pm 10V$	86	90		I	86	90		II	dB
		$R_L = 1\ k\Omega$, $V_{OUT} = \pm 10V$	80			I	80			III	dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$, $T_J = 25°C$ (See AC Test Circuits)

Parameter	Description	Test Conditions	EL2006, EL2006A				EL2006C, EL2006AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r	Rise Time	$A_V = 10V$, $V_{OUT} = 1\ V_{P-P}$		18		V		18		V	ns
		$A_V = 1V$, $V_{OUT} = 1\ V_{P-P}$		12	15	I		12	15	I	ns
SR	Slew Rate (Note 2)	$A_V = 1V$, $V_{OUT} = 20\ V_{P-P}$	350	450		I	350	450		I	$V/\mu s$
t_s	Settling Time to 1.0%	$A_V = -1V$, $V_{OUT} = 10\ V_{P-P}$		90		V		90		V	ns
t_s	Settling Time to 0.1%	$A_V = -1V$, $V_{OUT} = 10\ V_{P-P}$		160		V		160		V	ns
t_s	Settling Time to 0.01%	$A_V = -1V$, $V_{OUT} = 10\ V_{P-P}$		250		V		250		V	ns
GBW	Gain Bandwidth Product	$A_V \geq 20V$		500		V		500		V	MHz
	Pull Power Bandwidth (Note 3)	$V_{OUT} = \pm 10V$	5.5	7		I	5.5	7		I	MHz
	Unity Gain Bandwidth	$C_A = 8\ pF$, $C_B = 100\ pF$		40		V		40		V	MHz
e_N	Noise Voltage	1 kHz to 1 MHz		20		V		20		V	$nV/\sqrt{Hz}$
t_D	Small Signal Delay	$A_V = 1V$		13	15	I		13	15	I	ns
C_{IN}	Input Capacitance			2		V		2		V	pF

Note 1: $T_J = 25°C$, duty cycle < 1%, pulse width < 10 μs.
Note 2: Slew rate is measured at the 25% and 75% points.
Note 3: The Full Power bandwidth is guaranteed by testing slew rate.

EL2006 Recommended Compensation

(See Figure 1)

A_{VOL}	C_A	C_B	R_{S+}	R_{S-}	R_F
+1	5–8 pF	100 pF	2k	Open Circuit	100
−1 to +5	5 pF	68 pF	0	< 1k	1k
±10	5 pF	10 pF	< 1k	1k	> 10k
> ±20	3 pF	10 pF	< 1k	1k	> 20k

Note: Use a small capacitor of about 1 pF in parallel with R_F to compensate for stray input capacitance.

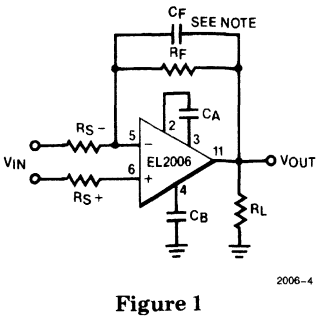
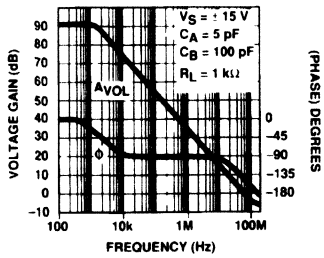


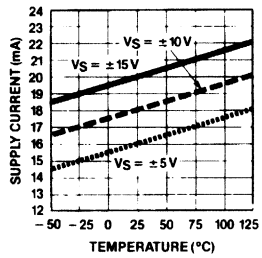
Figure 1

Typical Performance Curves

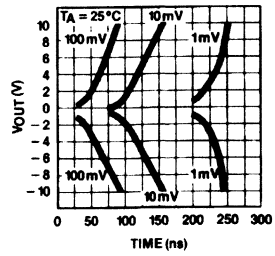
Bode Plot, Unity Gain Compensation



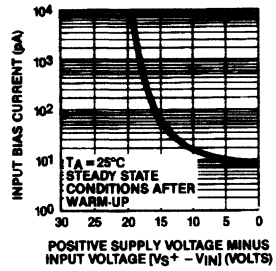
Supply Current vs Temperature



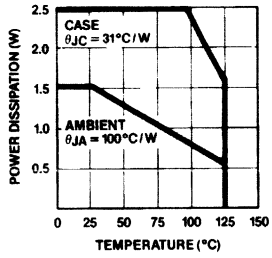
Inverting Gain of −1 Settling Time



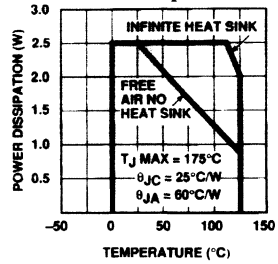
Input Bias Currents as a Function of Input Voltage



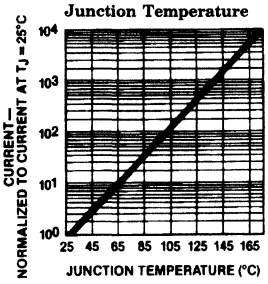
TO-8 Maximum Power Dissipation



52-Pad LCC Maximum Power Dissipation vs Ambient Temperature



Normalized Input Bias and Offset Current vs Junction Temperature



2006-5

Applications Information

General

The EL2006 was designed to overcome the gain and stability limitations of prior high speed FET input operational amplifiers like the LH0032. Open loop gain is typically 90 dB allowing gain setting to 12-bit accuracy. This new design also eliminates "thermal tail", which is the tendency for the gain to diminish at very low frequencies to DC due to thermal feedback. The EL2006 is also easier to stabilize than earlier designs, thanks to an Elantec proprietary internal compensation technique which eliminates the "second stage bump." The EL2006 open loop gain

EL2006/EL2006A
High Gain Fast FET Input Op Amp

Applications Information — Contd.

characteristic is well behaved well beyond the unity gain frequency so that spurious ringing or oscillation in the 100 MHZ–200 MHz region is avoided. Finally, we have provided temperature compensation so that gain and stability are relatively constant over temperature.

These improvements are provided in a configuration which is plug compatible with LH0032 and similar products so that designers can easily upgrade their system performance without extensive re-design. In most cases, the EL2006 can be used to replace LH0032 with no change in external compensation.

Video DAC Amplifiers

A typical application for the EL2006 is to provide gain for video signals. In the example shown, the EL2006 provides a gain of 2 with settling time around 35 ns to 10 mV.

Power Supply Decoupling

The EL2006/EL2006A, like most high-speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power, thus raising the FET junction temperature 40°C–60°C above the free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at the time will be indicative of normal operating currents. An additional rise will occur as power is delivered to a load due to additional internal power dissipation.

Power Dissipation

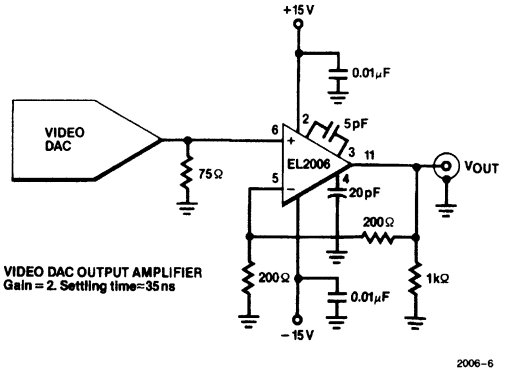
There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value, depending on FET geometry and doping levels. This effect will be noted as the input voltage of the EL2006 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the EL2006/EL2006A is typically 2 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a 1 pF.



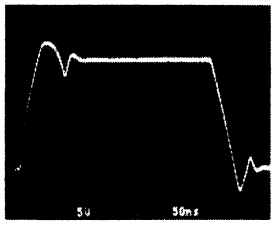
VIDEO DAC OUTPUT AMPLIFIER
Gain = 2. Settling time=35ns

Applications Information — Contd.

Heatsinking

While the EL2006/EL2006A are specified for operation without any explicit heatsink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

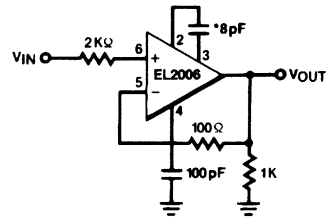
Voltage Follower (A_V = +1)
Large Signal Pulse Response



2006-12

V_S = ±15V, V_{IN} = +10V to −10V and −10V to +10V

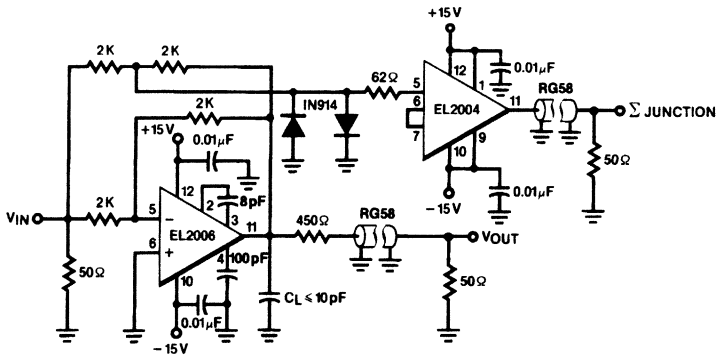
Large Signal Pulse Response Test Circuit



*INCLUDES STRAYS

2006-7

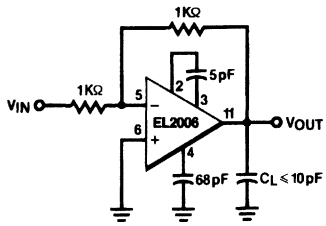
EL2006 Settling Time Test Circuit



RL = 2KΩ // 2KΩ // 500Ω ≈ 333Ω

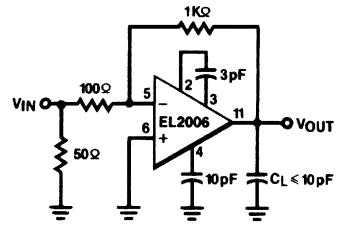
2006-8

Inverting Unity Gain



2006-9

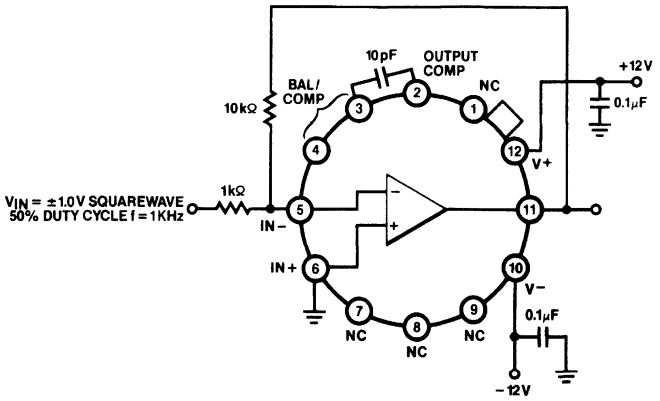
Inverting Gain of 10



2006-10

EL2006/EL2006A
High Gain Fast FET Input Op Amp

Burn-In Circuit



2006-11

Pin Numbers are for TO-8 package. LCC uses the same schematic.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2020/EL2020C
50 MHz Current Feedback Amplifier

Features

- Slew rate 500 V/μs
- ±33 mA output current
- Drives ±2.4V into 75Ω
- Differential phase <0.1°
- Differential gain <0.1%
- V supply ±5V to ±18V
- Output short circuit protected
- Uses current mode feedback
- 1% settling time of 50 ns for 10V step
- Low cost
- 9 mA supply current
- 8-pin mini-dip

Applications

- Video gain block
- Residue amplifier
- Radar systems
- Current to voltage converter
- Coax cable driver with gain of 2

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2020CN	0°C to +75°C	P-DIP	MDP0031
EL2020CJ	0°C to +75°C	CerDIP	MDP0010
EL2020J	−55°C to +125°C	CerDIP	MDP0010
EL2020J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2020CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2020L	−55°C to +125°C	20-Pad LCC	MDP0007
EL2020L/883B	−55°C to +125°C	20-Pad LCC	MDP0007

General Description

The EL2020 is a fast settling, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain then a conventional voltage feedback operational amplifier.

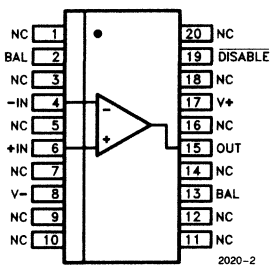
The EL2020 will drive two double terminated 75Ω coax cables to video levels with low distortion. Since it is a closed loop device, the EL2020 provides better gain accuracy and lower distortion than an open loop buffer. The device includes output short circuit protection, and input offset adjust capability.

The bandwidth and slew rate of the EL2020 are relatively independent of the closed loop gain taken. The 50 MHz bandwidth at unity gain only reduces to 30 MHz at a gain of 10. The EL2020 may be used in most applications where a conventional op amp is used, with a big improvement in speed power product.

Elantec products and facilities comply with MIL-I-45208A, MIL-STD-883 Rev C and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

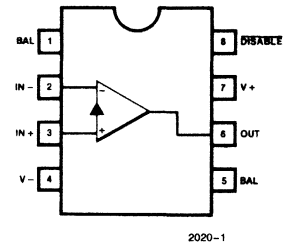
Connection Diagrams

SOL



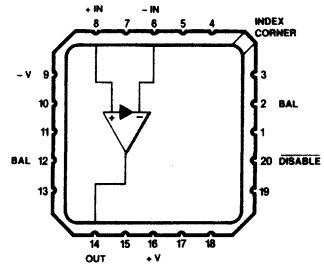
2020-2

DIP



2020-1

LCC



2020-3

EL2020/EL2020C
50 MHz Current Feedback Amplifier

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage	±18V or 36V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	±15V or V_S		EL2020	−55°C to +125°C
ΔV_{IN}	Differential Input Voltage	±10V		EL2020C	0°C to +75°C
I_{IN}	Input Current (Pins 2 or 3)	±10 mA	T_J	Operating Junction Temperature	
I_{INS}	Input Current (Pins 1, 5, or 8)	±5 mA		LCC, CerDIP Package	175°C
P_D	Maximum Power Dissipation			Plastic Package	150°C
	(See Curves)	1.25W	T_{ST}	Storage Temperature	−65°C to +150°C
I_{OP}	Peak Output Current	Short Circuit Protected		Lead Temperature (Soldering, 5 seconds)	300°C
	Output Short Circuit Duration (Note 2)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop Characteristics V_S = ±15V

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2020	EL2020C	
V_{OS} (Note 1)	Input Offset Voltage	25°C	−10	3	+10	I	I	mV
		T_{MIN}, T_{MAX}	−15		+15	I	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			−30		V	V	µV/°C
CMRR (Note 3)	Common Mode Rejection Ratio	ALL	50	60		I	II	dB
PSRR (Note 4)	Power Supply Rejection Ratio	25°C	65	75		I	I	dB
		T_{MIN}, T_{MAX}	60			I	III	dB
$+I_{IN}$	Non-inverting Input Current	25°C, T_{MAX}	−15	5	+15	I	II	µA
		T_{MIN}	−25		+25	I	III	µA
$+R_{IN}$	Non-Inverting Input Resistance	ALL	1	5		I	II	MΩ
+IPSR (Note 4)	Non-Inverting Input Current Power Supply Rejection	25°C, T_{MAX}		0.05	0.5	I	II	µA/V
		T_{MIN}			1.0	I	III	µA/V
$-I_{IN}$ (Note 1)	−Input Current	25°C, T_{MAX}	−40	10	+40	I	II	µA
		T_{MIN}	−50		+50	I	III	µA

Open Loop Characteristics $V_S = \pm 15V$ — Contd.

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2020	EL2020C	
−ICMR (Note 3)	−Input Current Common Mode Rejection	25°C, T_{MAX}		0.5	2.0	I	II	μA/V
		T_{MIN}			4.0	I	III	μA/V
−IPSR (Note 4)	−Input Current Power Supply Rejection	25°C, T_{MAX}		0.05	0.5	I	II	μA/V
		T_{MIN}			1.0	I	III	μA/V
R_{ol}	Transimpedence ($\Delta V_{OUT}/\Delta(-I_{IN})$) $R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25°C, T_{MAX}	300	1000		I	II	V/mA
		T_{MIN}	50			I	III	V/mA
A_{VOL1}	Open Loop DC Voltage Gain $R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25°C, T_{MAX}	70	80		I	II	dB
		T_{MIN}	60			I	III	dB
A_{VOL2}	Open Loop DC Voltage Gain $R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25°C, T_{MAX}	60	70		I	II	dB
		T_{MIN}	55			I	III	dB
V_O	Output Voltage Swing $R_L = 400\Omega$	25°C, T_{MAX}	±12	±13		I	II	V
		T_{MIN}	±11			I	III	V
I_{OUT}	Output Current $R_L = 400\Omega$	25°C, T_{MAX}	±30	±32.5		I	II	mA
		T_{MIN}	±27.5			I	III	mA
I_s	Quiescent Supply Current	25°C		9	12	I	I	mA
		T_{MIN}, T_{MAX}			15	I	III	mA
$I_{s\,off}$	Supply Current, Disabled, $V_8 = 0V$	ALL		5.5	7.5	I	II	mA
I_{logic}	Pin 8 Current, Pin 8 = 0V	ALL		1.1	1.5	I	II	mA
I_D	Min Pin 8 Current to Disable	ALL		120	250	I	II	μA
I_e	Max Pin 8 Current to Enable	ALL			30	I	II	μA

EL2020/EL2020C
50 MHz Current Feedback Amplifier

AC Closed Loop Characteristics EL2020/EL2020C $V_S = \pm 15V, T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
	Closed Loop Gain of 1 V/V (0 dB), $R_F = 1\ k\Omega$					
SR1	Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, test at $V_O = \pm 5V$	300	500		I	V/μs
FPBW1	Full Power Bandwidth (Note 5)	4.77	7.95		I	MHz
t_r1	Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		6		V	ns
t_f1	Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		6		V	ns
t_p1	Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% Points		8		V	ns
	Closed Loop Gain of 1 V/V (0 dB), $R_F = 820\Omega$					
BW	−3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100$ mV		50		V	MHz
t_s	1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		50		V	ns
t_s	0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		90		V	ns
	Closed Loop Gain of 10 V/V (20 dB), $R_F = 1\ k\Omega$, $R_G = 111\Omega$					
SR10	Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, Test at $V_O = \pm 5V$	300	500		I	V/μs
FPBW10	Full Power Bandwidth (Note 5)	4.77	7.95		I	MHz
t_r10	Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		25		V	ns
t_f10	Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		25		V	ns
t_p10	Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% points		12		V	ns
	Closed Loop Gain of 10 V/V (20 dB), $R_F = 680\Omega$, $R_G = 76\Omega$					
BW	−3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100$ mV		30		V	MHz
t_s	1% Settling Time, $R_l = 400\ \Omega$, $V_O = 10V$		55		V	ns
t_s	0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		280		V	ns

Note 1: The offset voltage and inverting input current can be adjusted with an external 10 kΩ pot between pins 1 and 5 with the wiper connected to V_{CC} (Pin 7) to make the output offset voltage zero.

Note 2: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

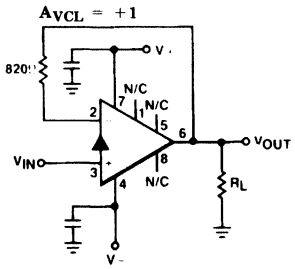
Note 3: $V_{CM} = \pm 10V$.

Note 4: $\pm 4.5V \leq V_S \leq \pm 18V$.

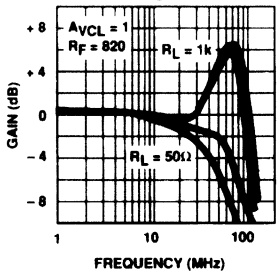
Note 5: Full Power Bandwidth is guaranteed based on Slew Rate measurement. $FPBW = SR/2\pi V_{peak}$.

Typical Performance Curves Non-Inverting Gain of One

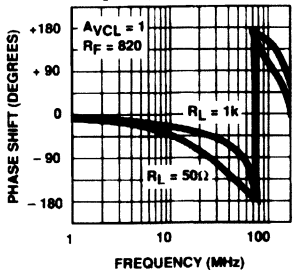
A_{VCL} = +1



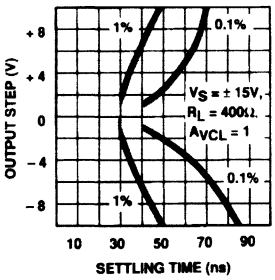
Gain vs Frequency



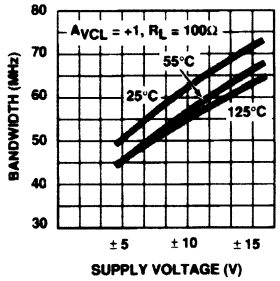
Phase Shift vs Frequency



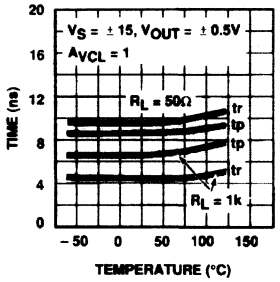
Settling Time vs Output Swing



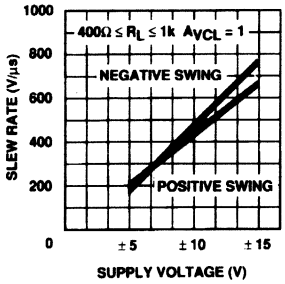
−3 dB Bandwidth vs Supply Voltage



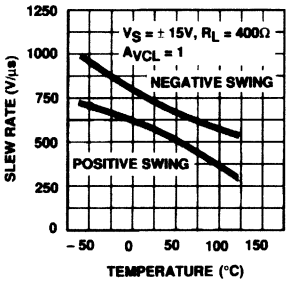
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



Slew Rate vs Temperature



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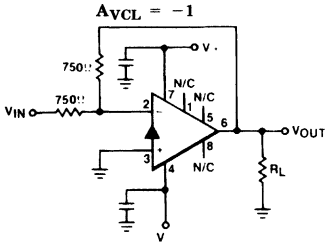
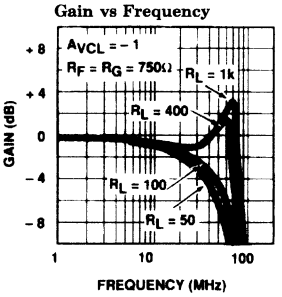
EL2020/EL2020C
50 MHz Current Feedback Amplifier

Typical Performance Curves — Contd. Inverting Gain of One

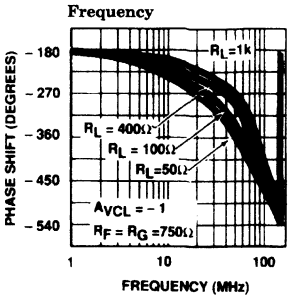
$A_{VCL} = -1$



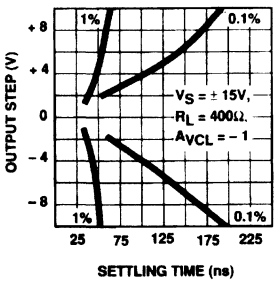
Gain vs Frequency



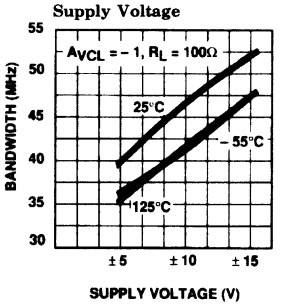
Phase Shift vs Frequency



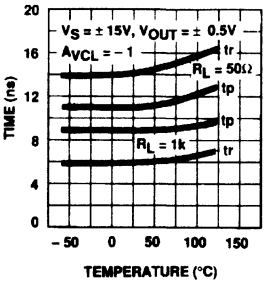
Settling Time vs Output Swing



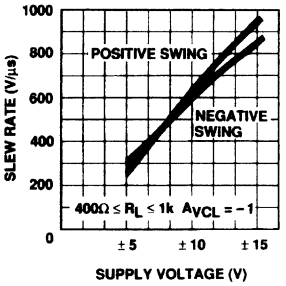
−3 dB Bandwidth vs Supply Voltage



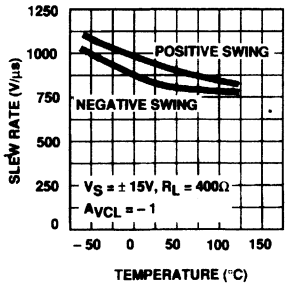
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



Slew Rate vs Temperature



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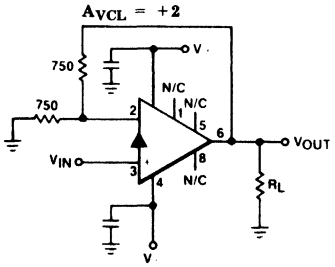
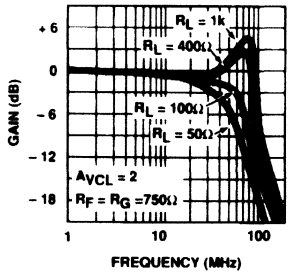
Typical Performance Curves — Contd. Non-Inverting Gain of Two

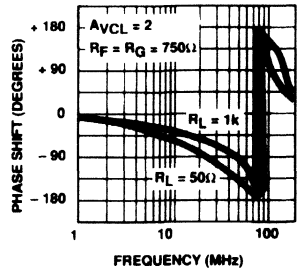
A_{VCL} = +2



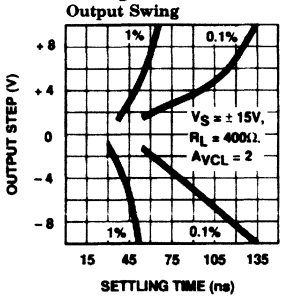
Gain vs Frequency



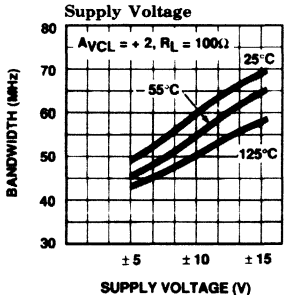
Phase Shift vs Frequency



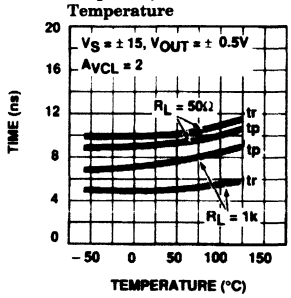
Settling Time vs Output Swing



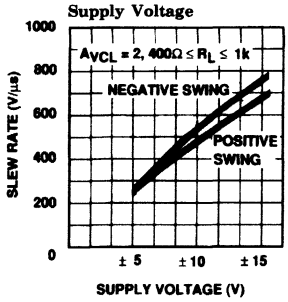
−3 dB Bandwidth vs Supply Voltage



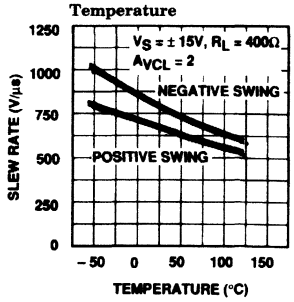
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



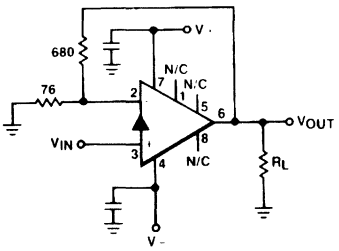
Slew Rate vs Temperature



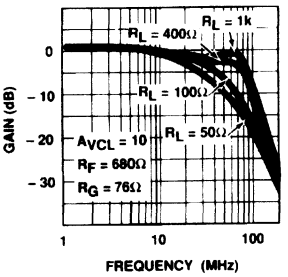
2020-6

Typical Performance Curves — Contd. Non-Inverting Gain of Ten

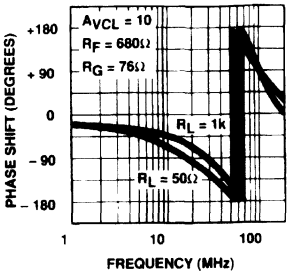
A_{VCL} = +10



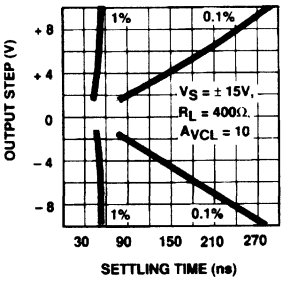
Gain vs Frequency



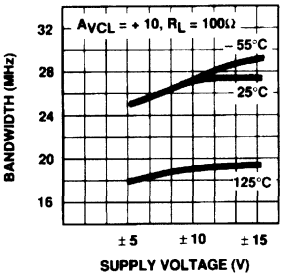
Phase Shift vs Frequency



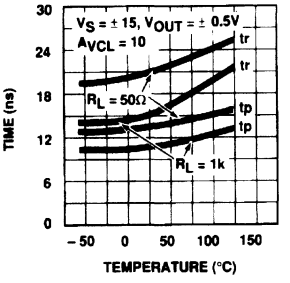
Settling Time vs Output Swing



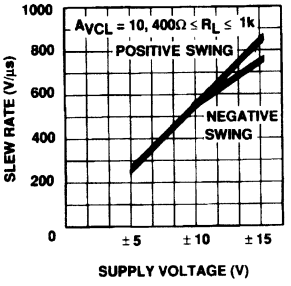
-3 dB Bandwidth vs Supply Voltage



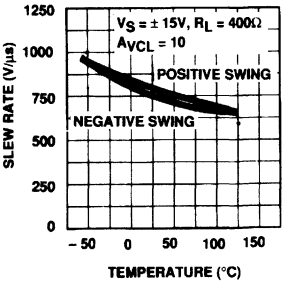
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



Slew Rate vs Temperature



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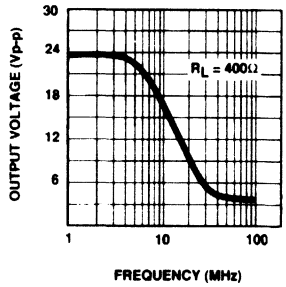
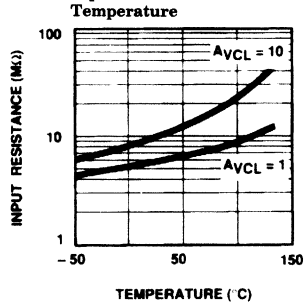
Typical Performance Curves — Contd.

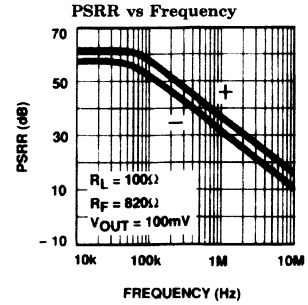
Maximum Undistorted Output Voltage vs Frequency



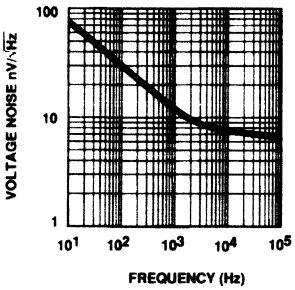
Input Resistance vs Temperature



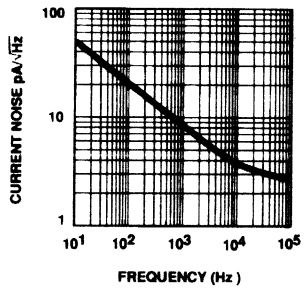
PSRR vs Frequency



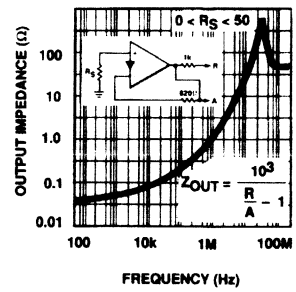
Voltage Noise vs Frequency



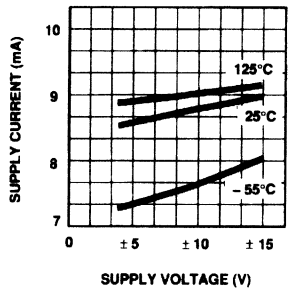
Current Noise vs Frequency



Output Impedance vs Frequency



Supply Current vs Supply Voltage



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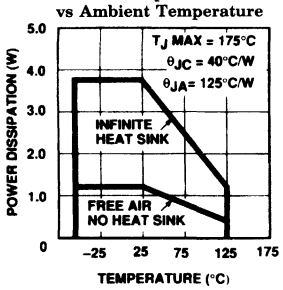
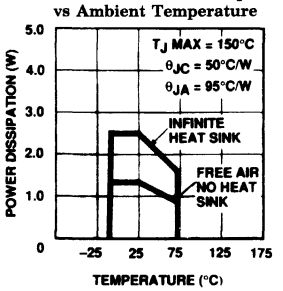
EL2020/EL2020C
50 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

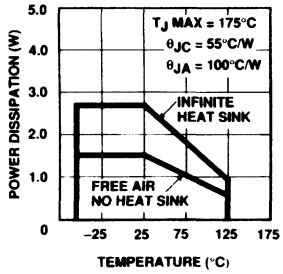
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



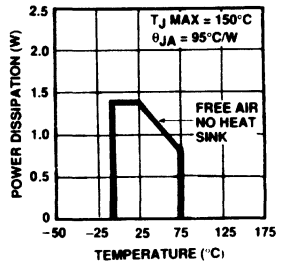
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2020-9

Application Information

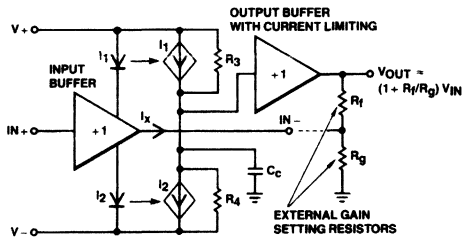
Theory of Operation

The EL2020 has a unity gain buffer similar to the EL2003 from the non-inverting input to the inverting input. The error signal of the EL2020 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is the transresistance (R_{OL}) of the EL2020 [$V_{OUT} = R_{OL} * I_{INV}$]. Since R_{OL} is very large ($\approx 10^6$), the current flowing into the inverting input in the steady state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first order approximation for circuit analysis, namely that...

1. The voltage across the inputs $\approx$ 0 and
2. The current into the inputs is $\approx$ 0

Simplified Block Diagram of EL2020



2020-10

Resistor Value Selection and Optimization

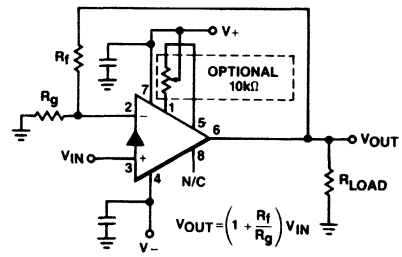
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2020. A nominal value for the feedback resistor is 1 kΩ, which is the value used for production testing. This value guarantees stability. For a given gain, the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth will be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed loop transfer function which results from stray capacitance between the inverting input and ground.

Power Supplies

The EL2020 may be operated with single or split power supplies as low as ±3V (6V total) to as high as ±18V (36V total). The slew rate degrades significantly for supply voltages less than ±5V (10V total), but the bandwidth only changes 25% for supplies from ±3V to ±18V. It is not necessary to use equal value split power supplies, i.e., −5V and +12V would be excellent for 0V to 1V video signals. Bypass capacitors from each supply pin to a ground plane are recommended. The EL2020 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate supply ringing and the errors it might cause, a 4.7 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rate and longer settling times.

Non-Inverting Amplifier



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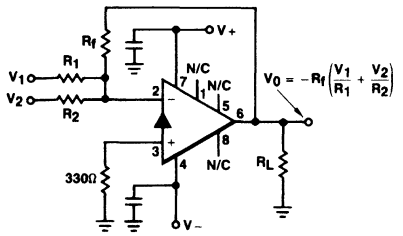
EL2020 Typical Non-Inverting Amplifier Characteristics

A_V	R_F	R_G	Bandwidth	10V Settling Time	
				1%	0.1%
+1	820Ω	None	50 MHz	50 ns	90 ns
+2	750Ω	750Ω	50 MHz	50 ns	100 ns
+5	680Ω	170Ω	50 MHz	50 ns	200 ns
+10	680Ω	76Ω	30 MHz	55 ns	280 ns

EL2020/EL2020C
50 MHz Current Feedback Amplifier

Application Information — Contd.

Summing Amplifier



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EL2020 Typical Inverting Amplifier Characteristics

A_V	R_F	R_1, R_2	Bandwidth	10V Settling Time	
				1%	0.1%
−1	750Ω	750Ω	40 MHz	50 ns	130 ns
−2	750Ω	375Ω	40 MHz	55 ns	160 ns
−5	680Ω	130Ω	40 MHz	55 ns	160 ns
−10	680Ω	68Ω	30 MHz	70 ns	170 ns

Input Range

The non-inverting input to the EL2020 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit.

The input charactersitics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that Schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2020 is fairly tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources may cause oscillations; a 1 kΩ resistor in series with the input lead will usually eliminate problems without sacrificing too much speed.

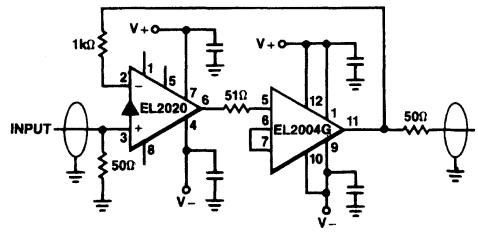
Current Limit

The EL2020 has internal current limits that protect the output transistors. The current limit goes down with junction temperature rise. At a junction temperature of +175°C the current limits are at about 50 mA. If the EL2020 output is shorted to ground when operating on ±15V supplies, the power dissipation could be as great as 1.1W. A heat sink is required in order for the EL2020 to survive an indefinite short. Recovery time to come out of current limit is about 50 ns.

Using the 2020 with Output Buffers

When more output current is required, a wideband buffer amplifier can be included in the feedback loop of the EL2020. With the EL2003 the subsystem overshoots about 10% due to the phase lag of the EL2003. With the EL2004 in the loop, the overshoot is less than 2%. For even more output current, several buffers can be paralleled.

EL2020 Buffered with an EL2004



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Capacitive Loads

The EL2020 is like most high speed feedback amplifiers in that it does not like capacitive loads between 50 pF and 1000 pF. The output resistance works with the capacitive load to form a second non-dominate pole in the loop. This results in excessive peaking and overshoot and can lead to oscillations. Standard resistive isolation techniques used with other op amps work well to isolate capacitive loads from the EL2020.

Application Information — Contd.

Offset Adjust

To calculate the amplifier system offset voltage from input to output we use the equation:

Output Offset Voltage = V_{OS} (R_F/R_G+1) ± I_{BIAS} (R_F)

The EL2020 output offset can be nulled by using a 10 kΩ potentiometer from pins 1 to 5 with the slider tied to pin 7 ($+V_{CC}$). This adjusts both the offset voltage and the inverting input bias current. The typical adjustment range is ±80 mV at the output.

Compensation

The EL2020 is internally compensated to work with external feedback resistors for optimum bandwidth over a wide range of closed loop gain. The part is designed for a nominal 1 kΩ of feedback resistance, although it is possible to get more bandwidth by decreasing the feedback resistance.

The EL2020 becomes *less* stable by adding capacitance in parallel with the feedback resistor, so feedback capacitance is not recommended.

The EL2020 is also sensitive to stray capacitance from the inverting input to ground, so the board should be laid out to keep the physical size of this node small, with ground plane kept away from this node.

Active Filters

The EL2020's low phase lag at high frequencies makes it an excellent choice for high performance active filters. The filter response more closely approaches the theoritical response than with conventional op amps due to the EL2020's smaller propagation delay. Because the internal compensation of the EL2020 depends on resistive feedback, the EL2020 should be set up as a gain block.

Driving Cables

The EL2020 was designed with driving coaxial cables in mind. With 30 mA of output drive and low output impedance, driving one to three 75Ω double terminated coax cables with one EL2020 is practical. Since it is easy to set up a gain of +2, the double matched method is the best way to drive coax cables, because the impedance match on both ends of the cable will suppress reflections. For a discussion on some of the other ways to drive cables, see the section on driving cables in the EL2003 data sheet.

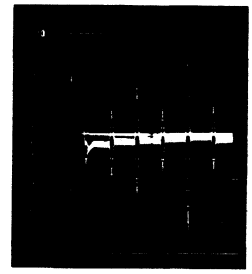
Video Performance Characteristics

The EL2020 makes an excellent gain block for video systems, both RS-170 (NTSC) and faster. It is capable of driving 3 double terminated 75Ω cables with distortion levels acceptable to broadcasters. A common video application is to drive a 75Ω double terminated coax with a gain of 2.

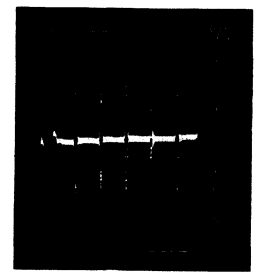
To measure the video performance of the EL2020 in the non-inverting gain of 2 configuration, 5 identical gain-of-two circuits were cascaded (with a divide by two 75Ω attenuator between each stage) to increase the errors.

The results, shown in the photos, indicate the entire system of 5 gain-of-two stages has a differential gain of 0.5% and a differential phase of 0.5°. This implies each device has a differential gain/phase of 0.1% and 0.1°, but these are too small to measure on single devices.

Differential Phase of 5 Cascaded Gain-Of-Two Stages



Differential Gain of 5 Cascaded Gain-Of-Two Stages



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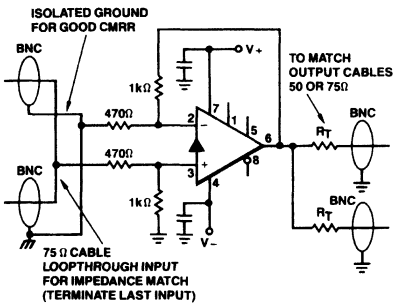
EL2020/EL2020C
50 MHz Current Feedback Amplifier

Application Information — Contd.

Video Distribution Amplifier

The distribution amplifier shown below features a difference input to reject common mode signals on the 75Ω coax cable input. Common mode rejection is often necessary to help to eliminate 60 Hz noise found in production environments.

Video Distribution Amplifier with Difference Input



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EL2020 Disable/Enable Operation

The EL2020 has an enable/disable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to pin 7, V_{CC}. When more than 250 μA is pulled from pin 8, the EL2020 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is halved. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (~1.1 mA) if pin 8 is grounded.

To draw current out of pin 8 an "open collector output" logic gate or a discrete NPN transistor can be used. This logic interface method has the advantage of level shifting the logic signal from 5V supplies to whatever supply the EL2020 is operating on without any additional components.

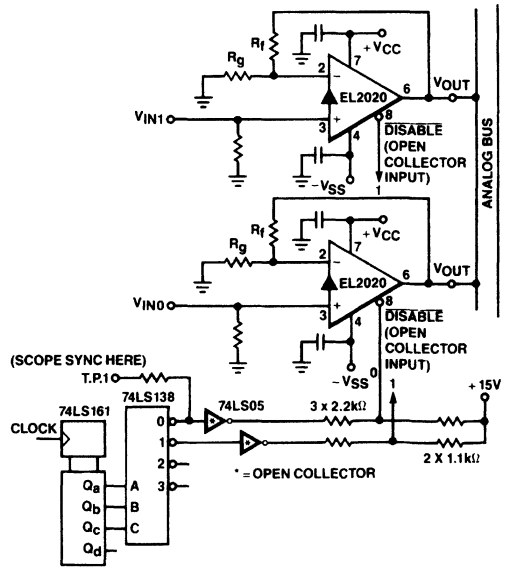
Using the EL2020 as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown.

When the EL2020 is disabled, the DC output impedance is very high, over 10 kΩ. However there is also an output capacitance that is non-linear. For signals of less than 5V peak to peak, the output capacitance looks like a simple 15 pF capacitor. However, for larger signals the output capacitance becomes much larger and non-linear.

The example multiplexer will switch between amplifiers in 5 μs for signals of less than ±2V on the outputs. For full output signals of 20V peak to peak, the selection time becomes 25 μs. The disabled outputs also present a capacitive load and therefore only three amplifiers can have their outputs shorted together. However an unlimited number can sum together if a small resistor (25Ω) is inserted in series with each output to isolate it from the "bus". There will be a small gain loss due to the resistors of course.

Using the EL2020 as a Multiplexer



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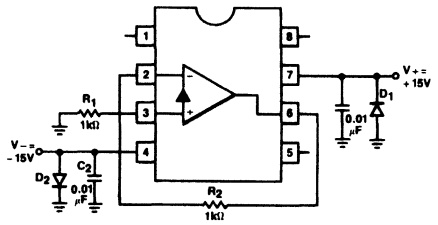
Burn-In Circuit



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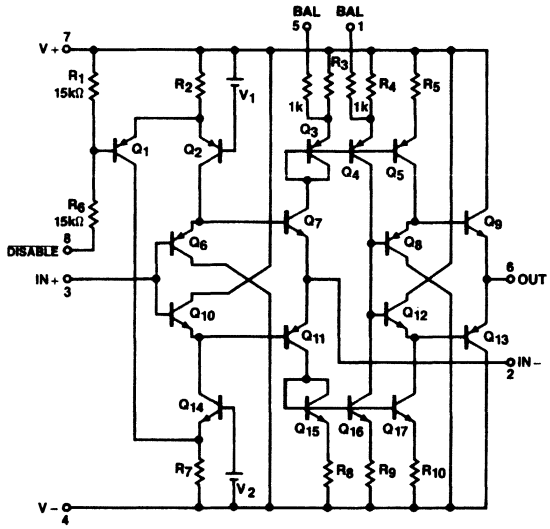
Pin numbers are for DIP Packages.
All Packages Use the Same Schematic.

Equivalent Circuit



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elantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2022/EL2022C
165 MHz Current Feedback Amplifier

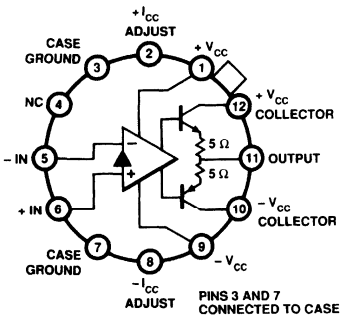
Features
- 165 MHz closed loop −3 dB bandwidth
- Slew rate of ±1900 V/μs
- Internal compensation for all gains
- ±100 mA output current
- 0.1% settling time is 22 ns for 2.5V volt step
- Small TO-8 package
- Vsupply ±5V to ±15V
- 18 mA supply current
- Pin Compatible with CLC231

Applications
- Video gain block
- Driving A/D converters
- Residue amplifier
- Radar systems
- DAC current to voltage converter
- Coax cable driver with gain of 2

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2022CG	−25°C to +85°C	12-Lead TO-8	MDP0019
EL2022G	−55°C to +125°C	12-Lead TO-8	MDP0019
EL2022G/883B	−55°C to +125°C	12-Lead TO-8	MDP0019

Connection Diagram



2022-1

Top View

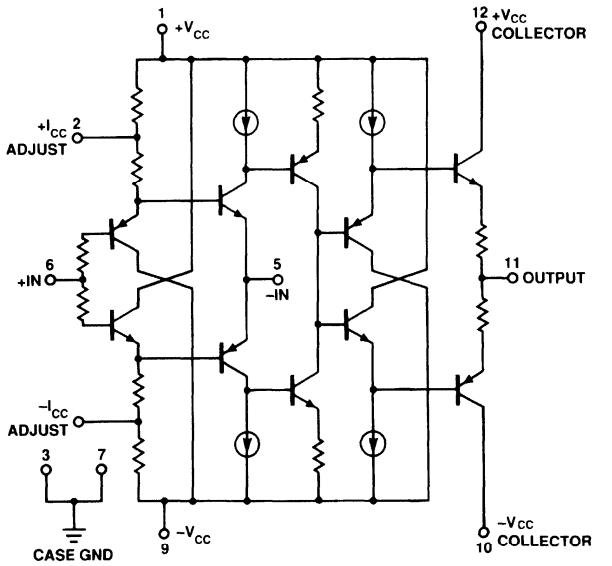
General Description

The EL2022 Amplifier is designed to drive low impedance loads at frequencies up to 165 MHz. The EL2022 is a fast settling, wide bandwidth amplifier optimized for gains between −5 and +5. This amplifier uses current mode feedback to achieve more bandwidth at a given gain than conventional voltage feedback operational amplifiers.

The EL2022 will drive five double terminated 75Ω coax cables to video levels with low distortion. It is a closed loop amplifier and provides better gain accuracy than is possible with open loop buffers. The EL2022 may be used in most applications where a conventional op amp is used, with a significant improvement in speed power product.

Elantec facilities comply with MIL-STD-1772A, MIL-I-45208 and other applicable quality specifications. For information on Elantec's military processing, see QRA-3, Elantec's 883B Program for Hybrid Integrated Circuits.

Simplified Schematic



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EL2022/EL2022C
165 MHz Current Feedback Amplifier

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage	±20V
V_{IN}	Input Voltage	V_S − 3.5V
I_{OP}	Peak Output Current	±100 mA
P_D	Maximum Power Dissipation (See Curves)	1.5 Watts
T_A	Operating Temperature Range	
	EL2022	−55°C to +125°C
	EL2022C	−25°C to +85°C
T_J	Operating Junction Temperature	175°C
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V, A_V = +2, R_F = 250Ω, R_L = 100Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise specified

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2022	EL2022C	
V_{IO}	Input Offset Voltage	25°C		1.0	2.5	I	I	mV
		T_{Max}			4.5	I	III	mV
		T_{Min}			4.0	I	III	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient	T_{Min} to T_{Max}		10		V	V	µV/°C
$+I_{IB}$	Non-Inverting Input Bias Current	25°C		5	21	I	I	µA
		T_{Max}			31	I	III	µA
		T_{Min}			29	I	III	µA
$\Delta(+I_{IB})/\Delta T$	Non-Inverting Input Bias Current Temperature Coefficient	T_{Min} to T_{Max}		50		V	V	nA/°C
$-I_{IB}$	Inverting Input Bias Current	25°C		10	15	I	I	µA
		T_{Max}			35	I	III	µA
		T_{Min}			31	I	III	µA
$\Delta(-I_{IB})/\Delta T$	Inverting Input Bias Current Temperature Coefficient	T_{Min} to T_{Max}		125		V	V	nA/°C
PSRR	Power Supply Rejection Ratio, ±5V CHANGED TO ±15V		50	80		I	II	dB

EL2022/EL2022C
165 MHz Current Feedback Amplifier

DC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 250\Omega$, $R_L = 100\Omega$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise specified—Contd.

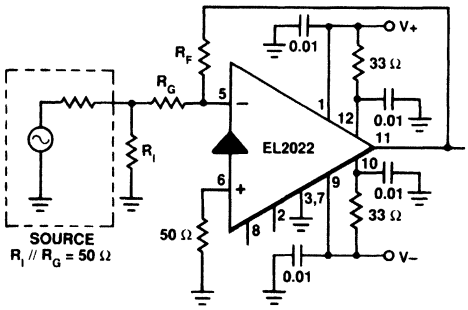
Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2022	EL2022C	
CMRR	Common Mode Rejection Ratio, $V_{CM} = \pm 5V$			46		V	V	dB
V_O	Output Voltage Swing No Load		±11	±12		I	II	V
I_{CC}	Supply Current			18	22	I	II	mA

AC Electrical Characteristics $V_S = \pm 15V$, $A_V = +2$, $R_F = 250\Omega$, $R_L = 100\Omega$

Parameter	Description	Output Voltage	Limits			Test Level		Units
			Min	Typ	Max	EL2022	EL2022C	
Time Domain Parameters								
t_r	Rise Time (Note 1)	−1V to +1V		2.1	2.75	I	III	ns
		−5V to +5V		4.3	5.5	I	III	ns
t_f	Fall Time (Note 1)	+1V to −1V		2.1	2.75	I	III	ns
		+5V to −5V		4.3	5.5	I	III	ns
OS	Overshoot	−2.5V to +2.5V		10	15	I	III	%
		+2.5V to −2.5V		10	15	I	III	%
SR	Slew Rate (Note 2)	−5V to +5V	1500	1900		I	III	V/µs
		+5V to −5V	1500	1900		I	III	V/µs
Frequency Domain Parameters								
BW	−3 dB Bandwidth	0.63 V_{pp}		165		V	V	MHz
G_p	Gain Peaking	0.63 V_{pp}		0.1		V	V	dB
G_r	Gain Rolloff, 100 MHz	0.63 V_{pp}		0.4		V	V	dB
R_{IN}	Non-Inverting Input Resistance			400		V	V	kΩ
C_{IN}	Non-Inverting Input Capacitance			1.3		V	V	pF
R_o	Output Resistance at 100 MHz			5		V	V	Ω
L_o	Output Inductance at 100 MHz			37		V	V	nH

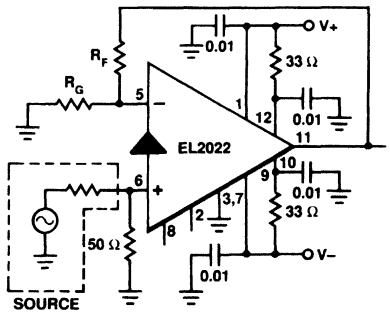
Note 1: Rise and fall times are measured between 10% and 90%.
Note 2: Slew rate measured between +2.5V and −2.5V.

Inverting Test Circuit



2022-3

Non-Inverting Test Circuit



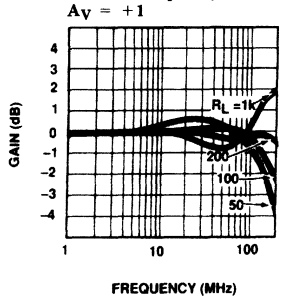
2022-4

Component Selection Chart

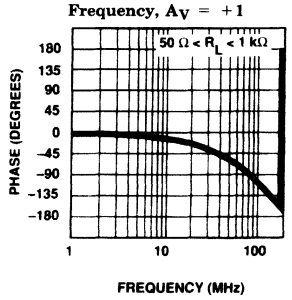
A_V	Circuit	R_F	R_G
−1	Inverting	250Ω	250Ω
−5	Inverting	250Ω	50Ω
+1	Non-Inverting	250Ω	Open
+2	Non-Inverting	250Ω	250Ω
+5	Non-Inverting	250Ω	62.5Ω

Typical Performance Curves

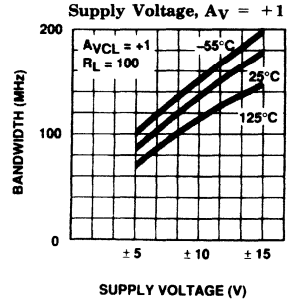
Gain vs Frequency, A_V = +1



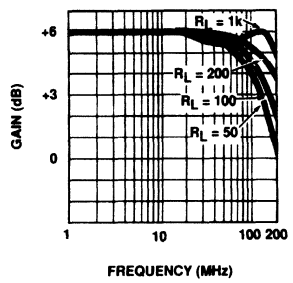
Phase Shift vs Frequency, A_V = +1



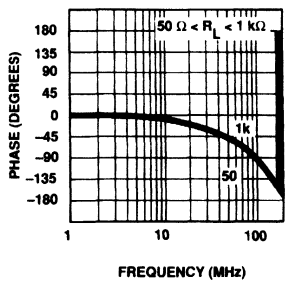
−3 dB Bandwidth vs Supply Voltage, A_V = +1



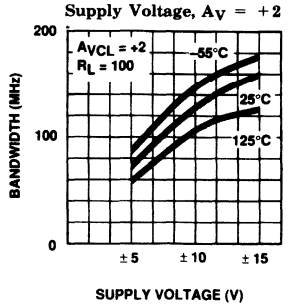
Gain vs Frequency, A_V = +2



Phase Shift vs Frequency, A_V = +2



−3 dB Bandwidth vs Supply Voltage, A_V = +2



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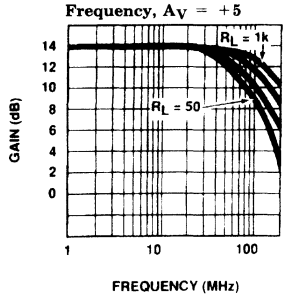
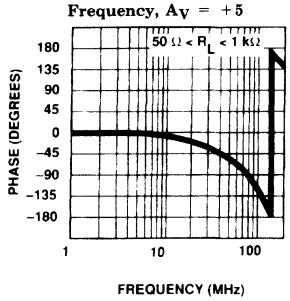
EL2022/EL2022C
165 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

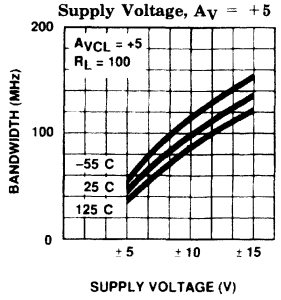
Gain vs Frequency, $A_V = +5$



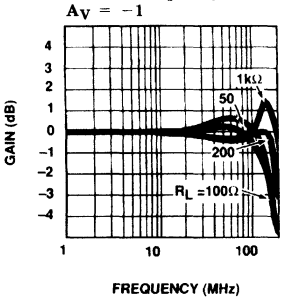
Phase Shift vs Frequency, $A_V = +5$



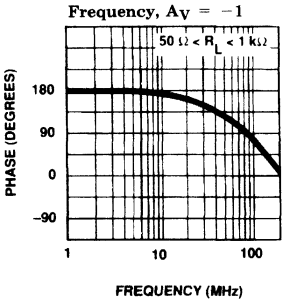
–3 dB Bandwidth vs Supply Voltage, $A_V = +5$



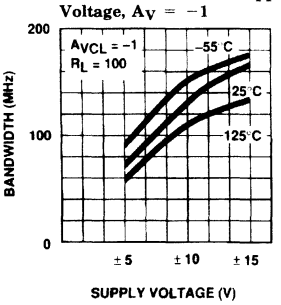
Gain vs Frequency, $A_V = -1$



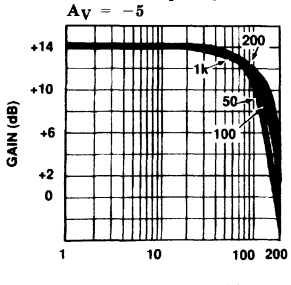
Phase Shift vs Frequency, $A_V = -1$



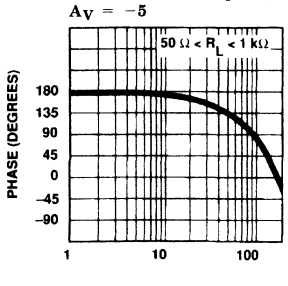
–3 dB Bandwidth vs Supply Voltage, $A_V = -1$



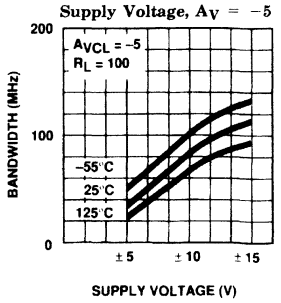
Gain vs Frequency, $A_V = -5$



Phase Shift vs Frequency, $A_V = -5$



–3 dB Bandwidth vs Supply Voltage, $A_V = -5$



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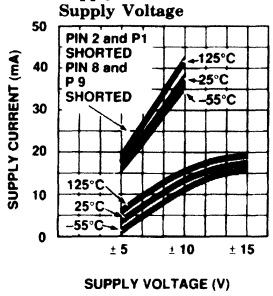
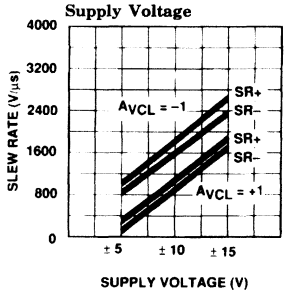
Typical Performance Curves — Contd.

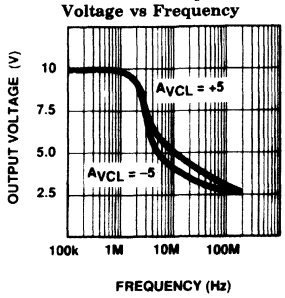
Supply Current vs Supply Voltage



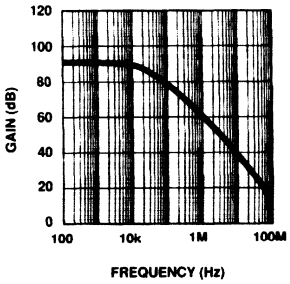
Slew Rate vs Supply Voltage



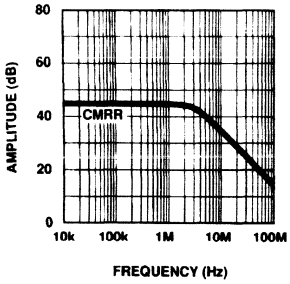
Undistorted Output Voltage vs Frequency



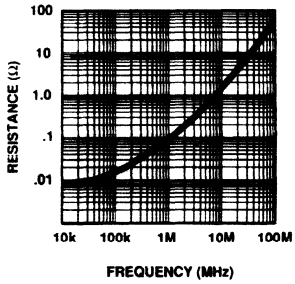
Open-Loop Voltage Gain vs Frequency



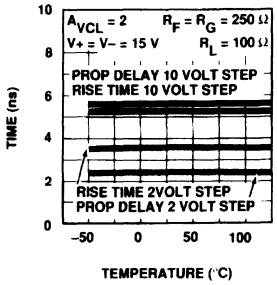
CMRR vs Frequency



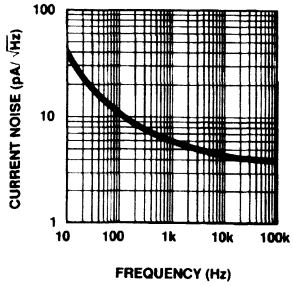
Closed Loop Output Impedance vs Frequency, A_V = +1



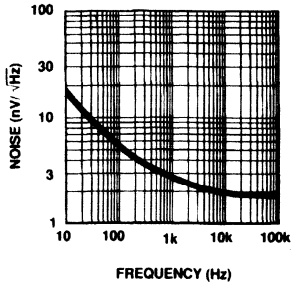
Prop Delay and Rise Time vs Supply Voltage



Current Noise



Voltage Noise



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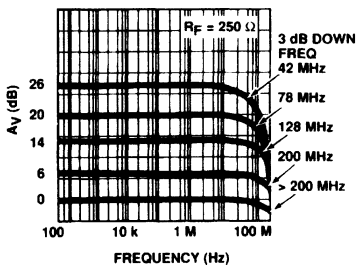
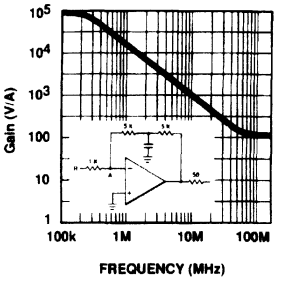
EL2022/EL2022C
165 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

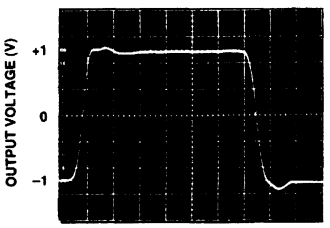
Frequency Response for Various Gains



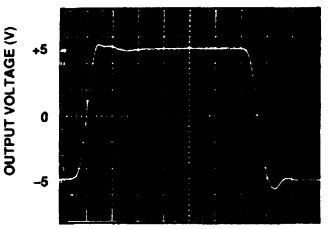
TRANS—Impedance



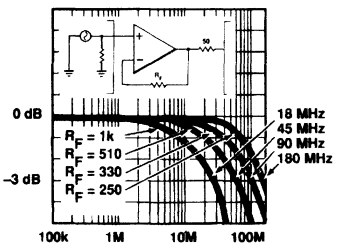
Small Signal Pulse Response



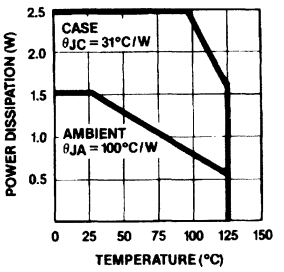
Large Signal Pulse Response



Frequency Response for Various Feedback Resistors Gain +1



Maximum Power Dissipation



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EL2022 Applications

EL2022 Basics

The EL2022 is a New Breed of Amplifier

It has a host of new features with which the user should be familiar. Among these are ...

1. It has a high impedance non-Inverting (+) input.
2. The impedance looking into the inverting input (−) open loop is low ($\approx$ 10Ω).
3. In steady state, the voltage at the (+) input follows the voltage at the (−) input.
4. The amplifier will try to put a voltage at the output that will force the current into the (−) input to be $\approx$ 0.
5. Therefore, the impedance looking into the inverting input is *increased* due to closing the loop around the amplifier.
6. The bandwidth of an amplifier subsystem built with the EL2022 is only mildly affected by the gain taken in the stage, provided the feedback resistor is held constant.
7. The bandwidth of an amplifier subsystem built with the EL2022 is strongly affected by the value of the feedback resistor used. The smaller the feedback resistor the more bandwidth, and vice versa. The optimum feedback resistor is 250Ω, with the device exhibiting peaking in the frequency domain if a smaller value is used.

The use of the EL2022 is similar to that of conventional op amps. We can still use the op amp assumptions as a first order approximation for circuit analysis, namely that ...

1. The voltage across the inputs $\approx$ 0 and
2. The current into the inputs is $\approx$ 0

Since the device is designed specifically for low gain applications, the best performance is obtained when the circuit is used at gains between ±5 and ±1. Performance is optimized for when a 250Ω feedback resistor is used.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than 0.25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not optimum.

During pc board layout, keep all traces short and direct. The body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of 0.01 to 0.1 μF (with short leads) should be less than 0.15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{CC} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in *Figures 1* and *2*. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase.

With proper layout, the EL2022 has excellent group delay characteristics. In a gain of +1, deviations from linear phase of less than ±1° have been observed over DC to 100 MHz.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junctions temperatures. Many styles of heat sinks are available for TO-8 packages; the Wakefield 215 and the Thermalloy 2240 are good examples. Some heat sinks are the radial fin type which cover the pc board and may

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165 MHz Current Feedback Amplifier

EL2022 Applications — Contd.

interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance.

For use of these heat sinks with conventional components, a 0.1″ high spacer can be inserted under the TO-8 package to allow sufficient clearance.

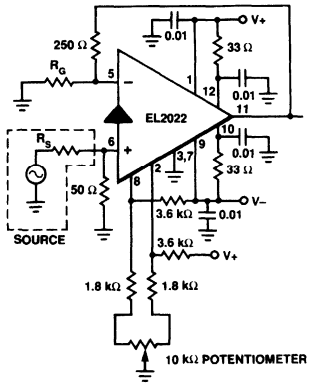
Low V_{CC} Operation: Supply Current Adjustment

The EL2022 is designed to operate on supplies as low as ±5V. In order to improve full bandwidth at reduced supply voltages, the supply current (I_{CC}) must be increased. The plot of supply current vs. V_{CC} shows the effect of shorting pins 1 and 2 and pins 8 and 9; this will increase both bandwidth and supply current. Care should be taken to not exceed the maximum junction temperatures; for this reason this technique should not be used with supplies exceeding ±10V. For intermediate values of V_{CC}, external resistors between pins 1 and 2 and pins 8 and 9 can be used.

Offset Voltage Adjustment

If trimming of the input offset voltage is desired, the circuit below can be used to adjust the V_{OS} approximately ±12 mV. If a narrower or broader adjustment range is desired, the 1.8 kΩ resistors can be scaled upward or downward respectively. Be aware that AC signals are present on pins 2 and 8 with this circuit.

Input Offset Adjust for the EL2022



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Power Supplies

The EL2022 may be operated with single or split power supplies as low as ±3V (6V total) to as high as ±20V (40V total). The slew rate degrades significantly for supply voltages less than ±5V (10V total).

When using power supplies of less than ±10V (20V total), pins 2 and 3 may be connected and pins 8 and 9 may be connected. This increases the supply current, bandwidth and slew rate. For power dissipation reasons this must not be done with supplies greater than 20V total. it is not necessary to use equal value split supplies, i.e., −5V and +12V would be fine for 0 to 2V output signals. Bypass capacitors from each supply pin to a ground plane are recommended. The EL2022 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate supply ringing and the errors it might cause, a 4.7 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rate and longer settling times.

Input Range

The non-inverting input to the EL2022 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However, if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that Schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2022 has good input-output isolation and is fairly tolerant of variations in source impedances. Capacitive sources cause no problems at

EL2022 Applications — Contd.

all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources can cause oscillations; a 100Ω resistor in series with the non-inverting input lead will usually eliminate problems without sacrificing too much speed. An unterminated cable or other resonant source can also cause oscillations. Again, an isolating resistor will eliminate the problem.

Feedback Resistor Selection

Nominally 250Ω, the value of the resistor has a strong effect on the dynamics of the amplifier.

Typical Non-Inverting Amplifier Characteristics

A_V	R_F	R_G	R_I	Bandwidth	Z_{IN}
+1	250Ω	None	100Ω	180 MHz	400 kΩ
+2	250Ω	250Ω	100Ω	165 MHz	400 kΩ
+5	250Ω	62.5Ω	100Ω	130 MHz	400 kΩ

Typical Inverting Amplifier Characteristics

A_V	R_F	R_G	R_I	Bandwidth
−1	250Ω	250Ω	100Ω	165 MHz
−2	250Ω	125Ω	100Ω	150 MHz
−5	250Ω	50Ω	100Ω	110 MHz

Mount the body of the feedback resistor near pin 5, to minimize capacitance on this node. Non-inductive resistors must be used. Do not use any feedback capacitance, instability may result.

For minimum settling time, minimize any stray capacitance from pin 5 to the output or to ground.

Current Limit

The EL2022 has the ability to have external current limits to protect the output transistors. This current limit is implemented with resistors in series with pins 12 and 10, the collectors of the output emitter followers. Bypassing of pins 12 and 10 is required. The short circuit current is given by $I_{SC} = V_{CC} - 0.6\ V/R_{SC}$. In order to limit the output current to 100 mA with ±15 supplies in the case of the output being shorted to ground, 150Ω 1 Watt resistors should be used here. This will also limit output swing into a heavy load.

Compensation

The EL2022 is compensated primarily with its feedback resistor and an internal capacitor from the gain node. The part is designed for a nominal 250Ω of feedback resistance, although it is possible to get more bandwidth by decreasing the feedback resistance.

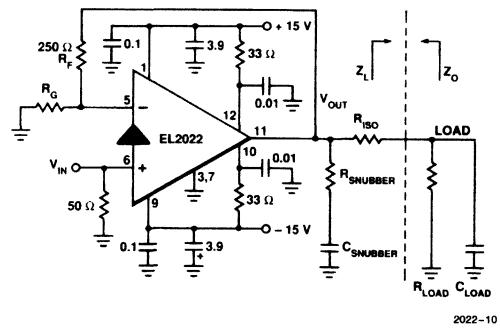
The EL2022 becomes **less** stable by adding capacitance in parallel with the feedback resistor, so feedback capacitance is not recommended.

The EL2022 is also sensitive to stray capacitance from the inverting input to ground, so the board should be laid out to keep the physical size of this node small.

Capacitive Loads

The EL2022 is stable driving most capacitive loads. However, when driving a pure capacitive load of less than a thousand picofarads the frequency response may have several dB of peaking and the squarewave response may ring for several hundred nanoseconds. To reduce these effects, and their associated peaking in the frequency domain, the circuit below should be used.

Driving Reactive Loads



The output stage of the EL2022 looks inductive at high frequencies, and the snubber components have two benefits. First, they de-Q the output stage by adding a real load at high frequency, and second, they provide an upper limit to the impedance from which the load is being driven from.

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165 MHz Current Feedback Amplifier

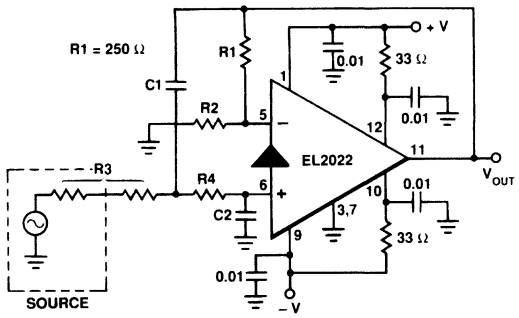
EL2022 Applications — Contd.

The isolation resistor has similar benefits. A value of R_{ISO} of 5Ω will not affect bandwidth or drive capability much, yet it will improve small and large signal response significantly with reactive loads. For a thorough discussion on reducing the effects of load capacitance and selecting optimal component values, see the section on driving capacitive loads in the EL2003 datasheet.

EL2022 Active Filters

The EL2022's low phase lag at high frequencies makes it an excellent choice for high performance active filters, and the filter response more closely approaches the theoretical response than with conventional op amps, due to the EL2022's shorter propagation delay. As long as you use it just as a gain block (called a +KRC realization) and don't put reactive components in the feedback path to the inverting input, it should work well.

2nd Order Low Pass Filter



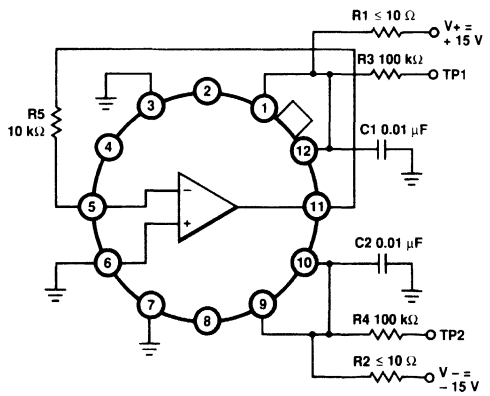
2022-11

Note that if R3 = R4 = R and C1 = C2 = C then $F_{cutoff} = 2\pi$ (1/RC) AND Q = 1/(3− (1+ (R1/R2)).

The EL2022 as a Coaxial Cable Driver

The EL2022 makes an excellent gain block for wide bandwidth systems. It is capable of driving more than 3 double terminated 75Ω cables with low distortion and very wide bandwidth. The most common application here may be the gain of 2 driving 50Ω or 75Ω double terminated coax. The EL2022 was designed with driving coaxial cables in mind. The 100 mA of output drive and its low output impedance allows it to drive two or three 75Ω double terminated coax cables with one EL2022, and still keep the speed and distortion specifications that professional video requires. The double matched method is the best way to drive coax cables, because the impedance match on both ends of the cable will suppress reflections. For a discussion on some of the other ways to drive cables, see the section on driving cables in the EL2003 datasheet.

Burn-In Circuit



2022-12

EL2028/EL2028C

0.01% 200 ns Unity Gain Stable Operational Amplifier

Features

- Settling time for 10V swings to 0.1% of 90 ns; to 0.01% of 200 ns
- Unity gain bandwidth—50 Mhz
- High slew rate—700 V/μs
- Large power bandwidth—5 MHz
- Large open loop gain—100 dB
- Low input offset voltage—1 mV
- Low input bias current—250 nA
- Inputs tolerant of overload
- Uses standard ±5V to ±15V supplies
- Output tolerant of load capacitance
- MIL-STD-883 Rev. C Compliant

Applications

- 12-bit DAC output amplifiers
- Fast-settling instrumentation amplifiers
- Driving 12-bit A/D converters
- Radar systems
- Replacement of costly hybrids

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2028CJ	0°C to +75°C	CerDIP	MDP0014
EL2028CN	0°C to +75°C	P-DIP	MDP0012
EL2028J	−55°C to +125°C	CerDIP	MDP0014
EL2028J/883B	−55°C to +125°C	CerDIP	MDP0014

General Description

The EL2028 monolithic operational amplifier is designed for extremely fast and clean settling with millivolt accuracy. It settles to 0.01% from a 10V step in 200 ns but has no thermal tail nor input slew overload penalties. The EL2028 is a true operational amplifier with low bias currents and large voltage gain, and is compensated for unity gain feedback.

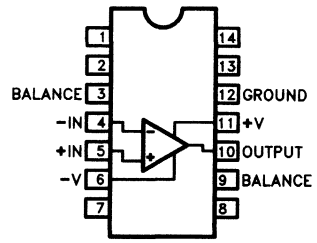
The inputs of the EL2028 are capable of 26V of differential overload without damage nor increased bias current. The input circuity does not exhibit slew aberrations even for signals beyond the output slew limit of 700 V/μs. The output is capable of large currents and is current-limited, and can drive as much as 100 pF stably. Even under capacitive loading the amplifier delivers a −3 dB bandwidth of 50 MHz.

The EL2028 can be used in circuits where current-feedback amplifiers were previously required for adequate speed, while offering at least a tenfold accuracy improvement.

Elantec's EL2028/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document QRA-2: *Elantec's Military processing-Monolithic Products.*

Connection Diagram

14-Pin DIP Package



Top View

EL2028/EL2028C

0.01% 200 ns Unity Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V
Voltage at GND Pin	V+ to V−
Voltage between −IN and +IN Pins	26V
Voltage at −IN or +IN Pins	V+ to V−
Output Current	50 mA (Peak) 30 mA (Continuous)
Current into +IN, −IN, GND, or Balance Pins	5 mA
Internal Power Dissipation	See Curves

Operating Ambient Temperature Range	
EL2028	−55°C to +125°C
EL2028C	0°C to +75°C
Operating Junction Temperature	
CerDIP	175°C
Plastic DIP	150°C
Lead Temperature (Soldering 5 seconds)	300°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 1k; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	EL2028 Test Level	EL2028C Test Level	Units
V_{OS}	Input Offset Voltage EL2028	25°C		0.25	2.0	I		mV
	EL2028C	25°C		0.25	1.0		I	mV
	EL2028	Full			3.0	I		mV
	EL2028C	Full			3.0		III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		3		V	V	µV/°C
I_B	Input Bias Current	25°C Full		250	500 800	I I	I III	nA nA
I_{OS}	Input Offset Current	25°C Full		120	250 350	I I	I III	nA nA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		10		V	V	MΩ
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		120		V	V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	V	pF
V_{CM}	Common-Mode Input Range	Full	±11	±12		I	II	V
E_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		10		V	V	nV/√hz
A_{VOL}	Large Signal Voltage Gain (V_O = ±10V)	25°C Full	45 20	80		I I	I III	V/mV V/mV
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	80	95		I	II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	80	95		I	II	dB
V_O	Output Voltage Swing	Full	±11	±12		I	II	V
I_O	Output Current (Note 3)	Full	±25	±50	±75	I	II	mA
I_S	Supply Current	Full		14	17	I	II	mA

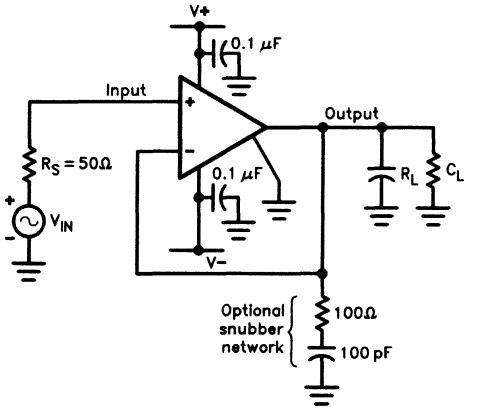
AC Electrical Characteristics

$V_S = \pm 15V$; $R_L = 1\ k\Omega$; $C_L = 25\ pF$; $T_A = 25°C$; Unless otherwise specified

Parameter	Description	Min	Typ	Max	EL2028 Test Level	EL2028C Test Level	Units
BW	Unity Gain −3 dB Bandwidth (Note 4)		50		V	V	MHz
GBW	Gain-Bandwidth Product (Note 4)		25		V	V	MHz
FPBW	Full-Power Bandwidth ($V_O = \pm 10V$)		5		V	V	MHz
SR	Slew Rate ($V_O = \pm 10V$)		700		V	V	V/μs
t_r	Rise Time (Notes 4, 5)		8		V	V	ns
O_S	Overshoot (Notes 4, 5)		10		V	V	%
t_s	Settling Time (Note 4) to 0.1% 10V Step to 0.01%		90 200		V V	V V	ns ns

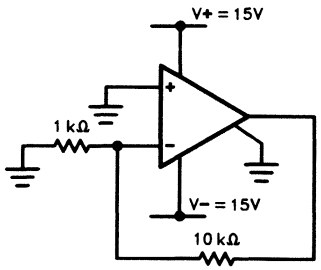
Note 1: Two tests are performed with $V_{CM} = 0V$ to $-11V$ and $V_{CM} = 0V$ to 11V.
Note 2: Two tests are performed with $V+ = 15V$, $V-$ changed from $-5V$ to $-15V$; $V- = -15V$, $V+$ changed from 5V to 15V.
Note 3: The inputs are overdriven by $\pm 15V$ and the output $R_L = 100\Omega$.
Note 4: A 100Ω + 100 pF snubber is used to load the output—see Applications section.
Note 5: V_{IN} = 100 mV peak-to-peak.

Test Circuit



2028-2

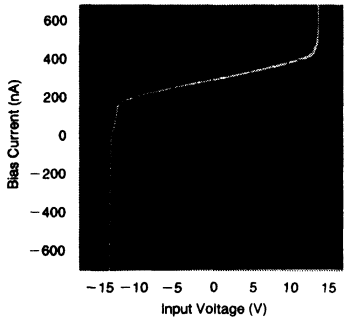
Burn-In Circuit



2028-3

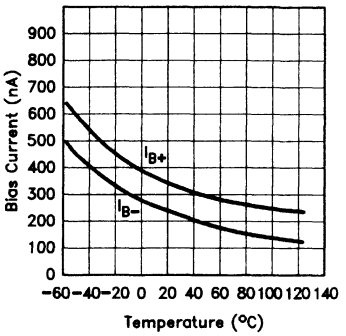
Typical Performance Curves

Input Bias Current vs Common-Mode Voltage



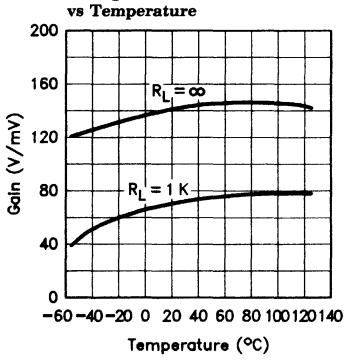
2028-4

Input Bias Current vs Temperature



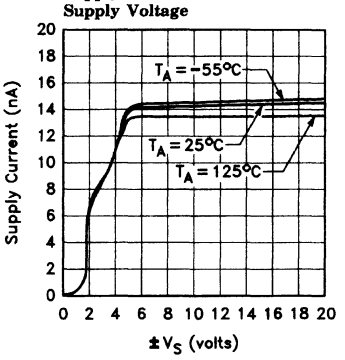
2028-5

Voltage Gain vs Temperature



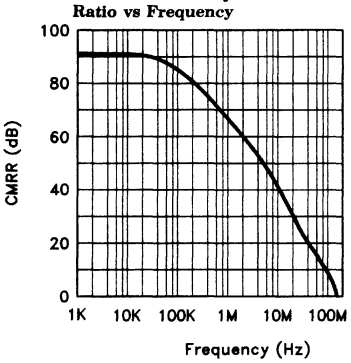
2028-6

Supply Current vs Supply Voltage



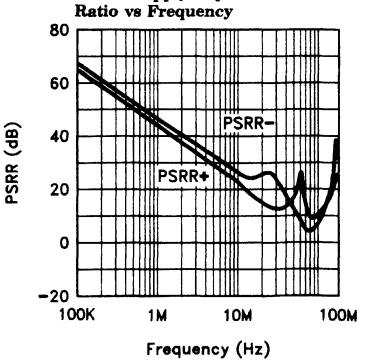
2028-7

Common-Mode Rejection Ratio vs Frequency



2028-8

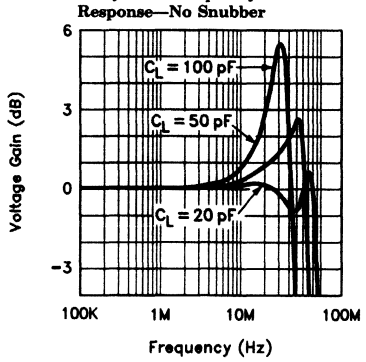
Power Supply Rejection Ratio vs Frequency



2028-9

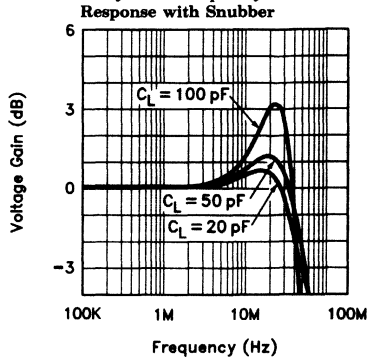
Typical Performance Curves — Contd.

Unity-Gain Frequency Response—No Snubber



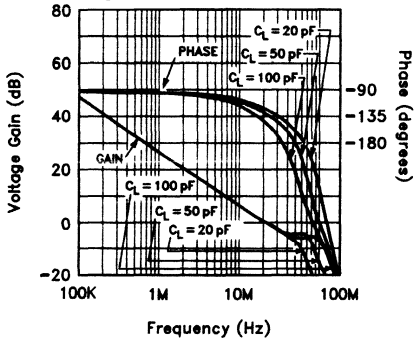
2028-10

Unity-Gain Frequency Response with Snubber



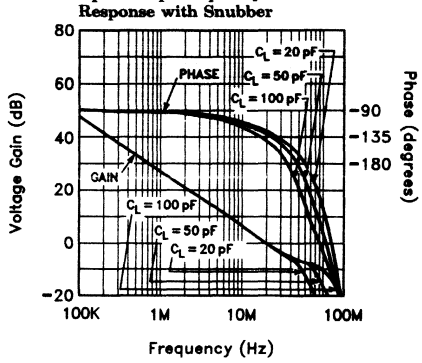
2028-11

Open-Loop Frequency Response—No Snubber



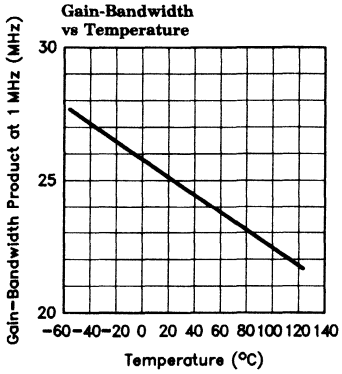
2028-12

Open-Loop Frequency Response with Snubber



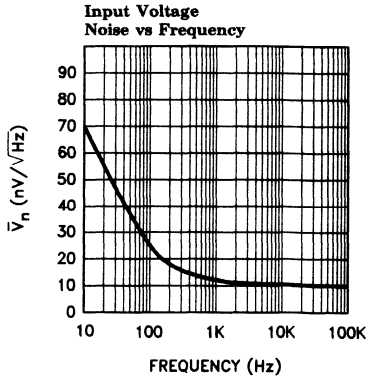
2028-13

Gain-Bandwidth vs Temperature



2028-14

Input Voltage Noise vs Frequency



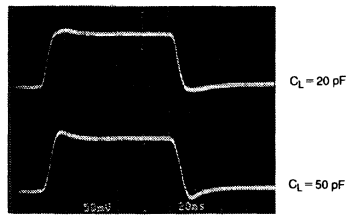
2028-15

Typical Performance Curves — Contd.

Small-Signal Pulse Response—No Snubber

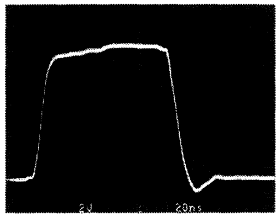
2028-16

Small-Signal Pulse Response— 100Ω + 100 pF Snubber



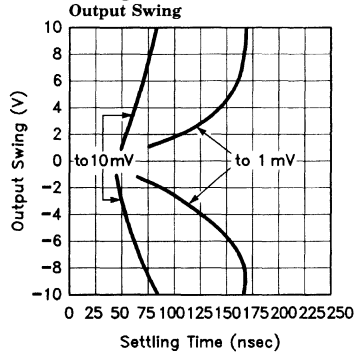
2028-17

Large-Signal Pulse Response—No Snubber



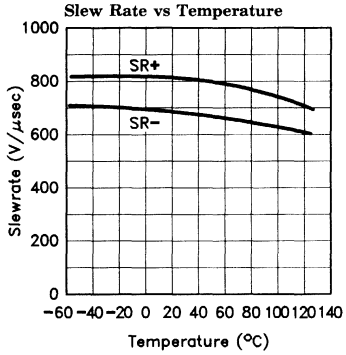
2028-18

Settling Time vs Output Swing



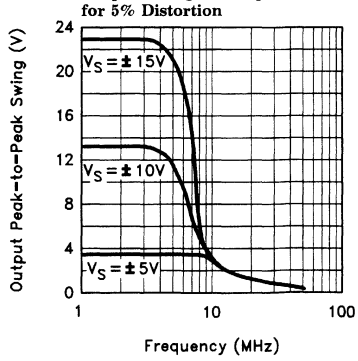
2028-19

Slew Rate vs Temperature



2028-20

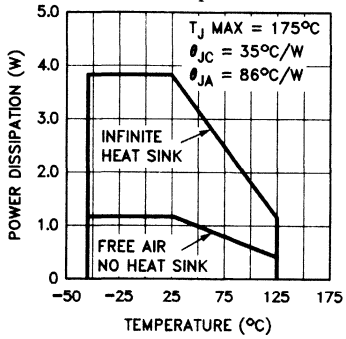
Output Swing vs Frequency for 5% Distortion



2028-21

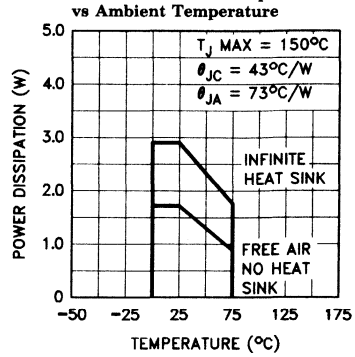
Typical Performance Curves — Contd.

14-Lead CerDIP
Maximum Power Dissipation
vs Ambient Temperature



2028-22

14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



2028-23

Applications Information

The EL2028 is a conventional high-accuracy operational amplifier with the speeds and bandwidths normally found only in current-feedback amplifiers. All the usual op amp configurations may be applied since the device is unity gain stable. The EL2028 will work well with a wide variety of loads and power supplies.

Power Supplies and Grounding

As with all high-frequency amplifiers, it is necessary to bypass the supply pins to ground close to the part. 0.01 μF capacitors of the ceramic type will suffice, although tantalum capacitors of any available value are perhaps the best choice. Tantalum capacitors have low series inductance yet are not high-Q in nature, helping to damp supply variations caused by load currents.

The EL2028 will work well from $\pm$5V supplies, with the input and output swings reduced to $\pm$1V over temperature, $\pm$2V nominally. At higher supplies, the part's dissipation must be maintained within package limits when the device and any load-related dissipations are calculated. Clip-on heatsinks are effective in reducing die temperature. Note that the device will warm approximately 36°C upon power-up: any accurate DC tests should either be done within 1 second or after 1 minute of turn-on at maximum supplies.

Although the part is current-limited at its output, that current can cause enough dissipation such that the maximum die temperature specification will be exceeded.

The EL2028 has a unique ground pin connection. The compensation capacitor returns to this pin rather than ground to aid in noise and settling characteristics. The input bias current compensation circuitry is also referred to this pin, so it cannot be connected to a voltage outside the input common-mode range.

Input Circuitry

The input appears as a high impedance even when the amplifier is overloaded. The input will not be damaged by transient nor continuous overloads, although an additional supply current of 2 mA per volt of overload will result. This should be considered in the device thermal calculations.

Like many other high-speed amplifiers, the input circuitry can resonate or even oscillate when driven by high-impedance inputs. The worst situation is when the device looks into an unterminated coaxial cable or a large inductance. Normal circuit interconnects cause no trouble. If the source impedance is difficult, a snubber similar to the output snubber can be added in parallel with the input.

Applications Information — Contd.

High values of feedback impedance can sacrifice loop stability. The main point is that the pole caused by any stray capacitance and the feedback network impedance should be several times greater than the EL2028's gain-bandwidth product divided by the noise gain of the feedback loop. If this condition cannot be met, the feedback resistor can have a small (1 pF–2 pF) capacitor in parallel to improve closed-loop phase margin.

Output Circuitry

The output circuitry was designed to deliver more current than the device can safely continuously output so that the transient currents caused by fast slews can be developed. For instance, a 50 pF load will draw 35 mA in response to a 700 V/μs output transient. The snubber network will draw similar currents, and it may not be useable if the amplifier is called upon to deliver large outputs continuously at high frequencies. In any event, the device is rated at 30 mA continuously.

The output circuit will resonate with capacitive loads if it is not damped. The output impedance of all amplifiers is approximately modeled as an inductor in series with a DC resistance. The equivalent component values for the EL2028 are 300 nH and 20Ω. To reduce the output stage resonance with capacitive loads, the snubber network can be added to de-Q the load. The EL2028 will comfortably drive 100 pF with the snubber values of 100 pF and 100Ω.

Offset Adjust

To effect input offset voltage adjustment, a 10k to 100k potentiometer is connected to the balance pins with the wiper connected to V−. $\pm$2.8 mV of adjustment is possible.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2029/EL2029C

0.01% 200 ns Op Amp—Gain of 5 Stable

Features

- Settling time for 10V swings to 0.1% of 100 ns; to 0.01% of 200 ns
- High slew rate—900 V/μs
- Large power bandwidth—5 MHz
- Large open loop gain—104 dB
- Low input offset voltage—500 μV
- Low input bias current—250 nA
- Inputs tolerant of overload
- Uses standard ±5V to ±15V supplies
- Output tolerant of load capacitance
- MIL-STD-883 Rev. C Compliant

Applications

- 12-bit DAC output amplifiers
- Fast-settling instrumentation amplifiers
- Driving 12-bit A/D converters
- Radar systems
- Replacement of costly hybrids

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2029CJ	0°C to +75°C	CerDIP	MDP0014
EL2029CN	0°C to +75°C	P-DIP	MDP0012
EL2029J	−55°C to +125°C	CerDIP	MDP0014
EL2029J/883B	−55°C to +125°C	CerDIP	MDP0014

General Description

The EL2029 monolithic operational amplifier is designed for extremely fast and clean settling with millivolt accuracy. It settles to 0.01% from a 10V step in 200 ns but has no thermal tail nor input slew overload penalities. The EL2029 is a true operational amplifier with low bias currents and large voltage gain, and is compensated for closed-loop gains of five or more.

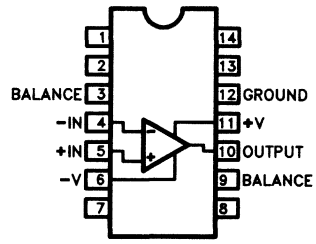
The inputs of the EL2029 are capable of 10V of differential overload without damage nor increased bias current. The amplifier does not exhibit slew aberrations even for signals beyond the output slew limit of 900 V/μs. The output is capable of large currents and is current-limited, and can drive as much as 100 pF stably.

The EL2029 can be used in circuits where current-feedback amplifiers were previously required for adequate speed, while offering at least a tenfold accuracy improvement.

Elantec's EL2029/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document QRA-2: *Elantec's Military processing-Monolithic Products.*

Connection Diagram

14-Pin DIP Package



2029-1

Top View

EL2029/EL2029C

0.01% 200 ns Op Amp—Gain of 5 Stable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V
Voltage at GND Pin	V+ to V−
Voltage between −IN and +IN Pins	10V
Voltage at −IN or +IN Pins	V+ to V−
Output Current	50 mA (Peak) 30 mA (Continuous)
Current into +IN, −IN, GND, or Balance Pins	5 mA
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	
EL2029	−55°C to +125°C
EL2029C	0°C to +75°C
Operating Junction Temperature	
CerDIP	175°C
Plastic DIP	150°C
Lead Temperature (Soldering 5 seconds)	300°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_F = 820Ω; R_G = 200Ω; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	EL2029 Test Level	EL2029C Test Level	Units
V_{OS}	Input Offset Voltage EL2029	25°C		0.15	1.0	I		mV
	EL2029C	25°C		0.15	0.5		I	mV
	EL2029	Full			1.5	I		mV
	EL2029C	Full			1.5		III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		3		V	V	µV/C
I_B	Input Bias Current	25°C		250	500	I	I	nA
		Full			800	I	III	nA
I_{OS}	Input Offset Current	25°C		120	250	I	I	nA
		Full			350	I	III	nA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		5		V	V	MΩ
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		120		V	V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	V	pF
V_{CM}	Common-Mode Input Range	Full	±11	±12		I	II	V
E_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		7		V	V	nV/$\sqrt{hz}$
A_{VOL}	Large Signal Voltage Gain	25°C	60	140		I	I	V/mV
	(V_O = ±10V)	Full	40			I	III	V/mV
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	80	95		I	II	dB

DC Electrical Characteristics

$V_S = \pm 15V$; $R_F = 820\Omega$; $R_G = 200\Omega$; $T_A = 25°C$ unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	EL2029 Test Level	EL2029C Test Level	Units
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	80	95		I	II	dB
V_O	Output Voltage Swing	Full	±11	±12		I	II	V
I_O	Output Current (Note 3)	Full	±25	±50	±75	I	II	mA
I_S	Supply Current	Full		14	17	I	II	mA

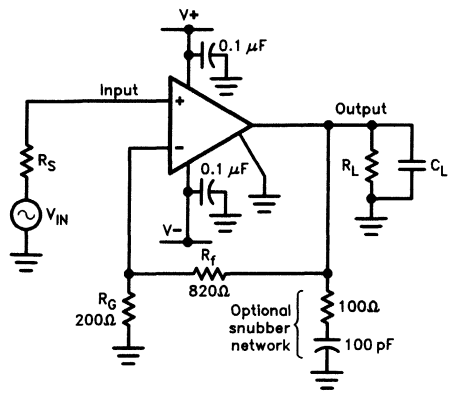
AC Electrical Characteristics

$V_S = \pm 15V$; $R_F = 820\Omega$; $R_G = 200\Omega$; $C_L = 25$ pF; $T_A = 25°C$ unless otherwise specified

Parameter	Description	Min	Typ	Max	EL2029 Test Level	EL2029C Test Level	Units
GBW	Gain-Bandwidth Product (Note 4)		100		V	V	MHz
FPBW	Full-Power Bandwidth ($V_O = \pm 10V$)		5		V	V	MHz
SR	Slew Rate ($V_O = \pm 10V$)		900		V	V	V/μs
tr	Rise Time (Notes 4, 5)		8		V	V	ns
OS	Overshoot (Notes 4, 5)		15		V	V	%
ts	Settling Time (Note 4) to 0.1% 10V Step to 0.01%		100 200		V V	V V	ns ns

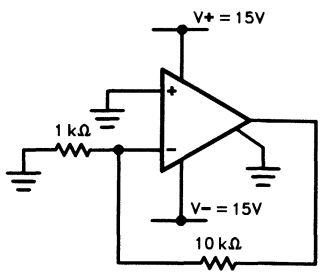
Note 1: Two tests are performed with $V_{CM} = 0V$ to $-11V$ and $V_{CM} = 0V$ to $11V$.
Note 2: Two tests are performed with $V+ = 15V$, $V-$ changed from $-5V$ to $-15V$; $V- = -15V$, $V+$ changed from 5V to 15V.
Note 3: The inputs are overdriven by $\pm 5V$ and the output $R_L = 100\Omega$.
Note 4: A 100Ω + 100 pF snubber is used to load the output—see Applications section.
Note 5: $V_{IN} = 100$ mV peak-to-peak.

Test Circuit



2029-2

Burn-In Circuit

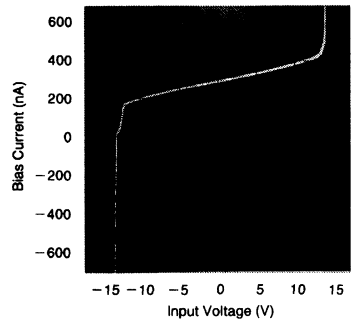


2029-3

EL2029/EL2029C
0.01% 200 ns Op Amp—Gain of 5 Stable

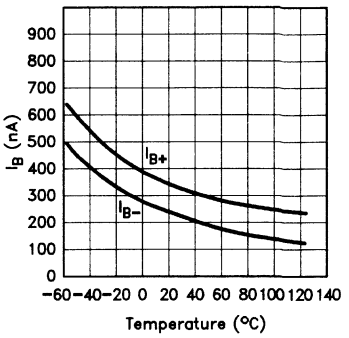
Typical Performance Curves

Input Bias Current vs Common-Mode Voltage



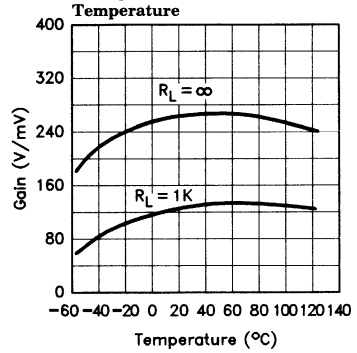
2029-4

Input Bias Current vs Temperature



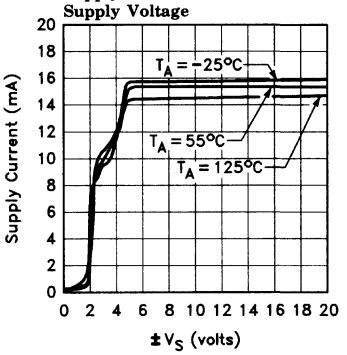
2029-5

Voltage Gain vs Temperature



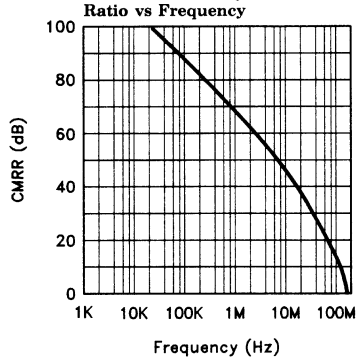
2029-6

Supply Current vs Supply Voltage



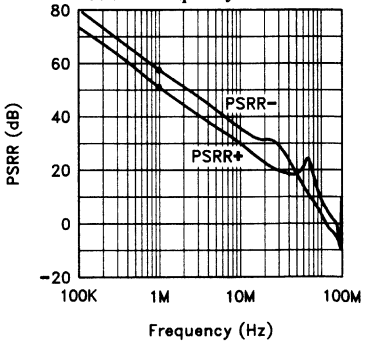
2029-7

Common-Mode Rejection Ratio vs Frequency



2029-8

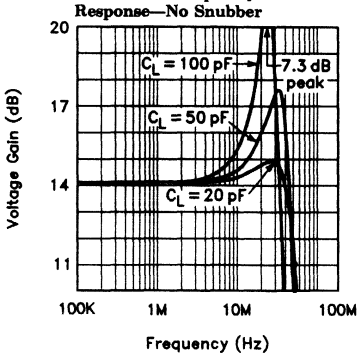
Power Supply Rejection Ratio vs Frequency



2029-9

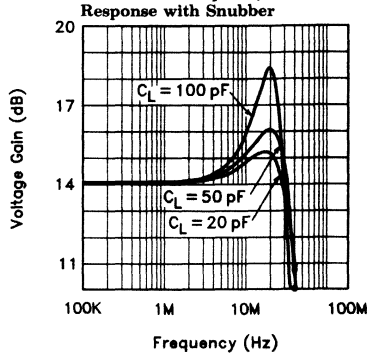
Typical Performance Curves — Contd.

Gain of +5 Frequency Response—No Snubber



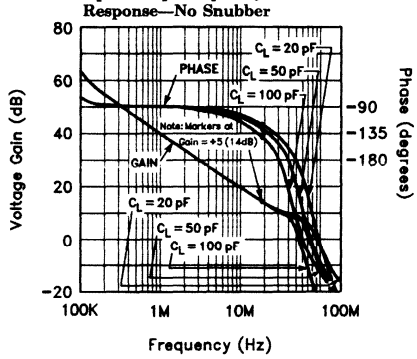
2029-10

Gain of +5 Frequency Response with Snubber



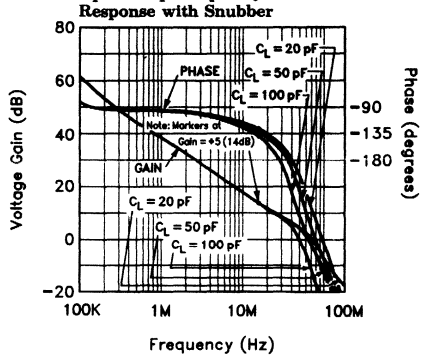
2029-11

Open-Loop Frequency Response—No Snubber



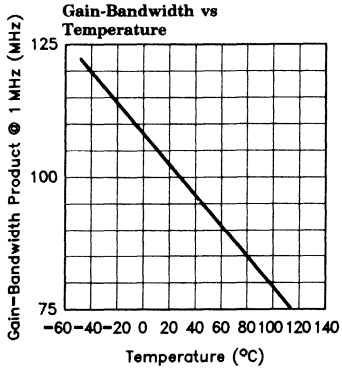
2029-12

Open-Loop Frequency Response with Snubber



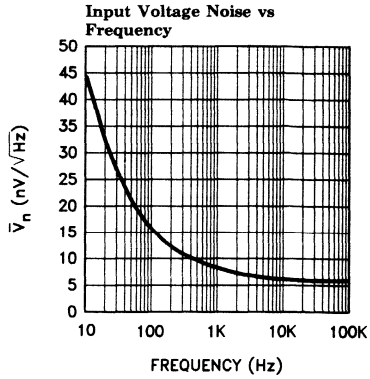
2029-13

Gain-Bandwidth vs Temperature



2029-14

Input Voltage Noise vs Frequency

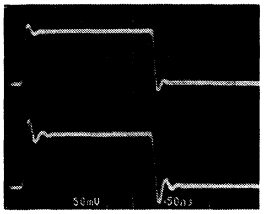


2029-15

EL2029/EL2029C
0.01% 200 ns Op Amp—Gain of 5 Stable

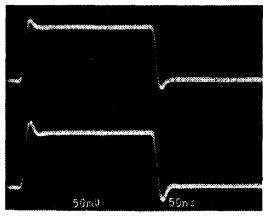
Typical Performance Curves — Contd.

Small-Signal Pulse Response—No Snubber



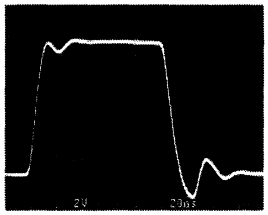
2029-16

Small-Signal Pulse Response—100Ω + 100 pF Snubber



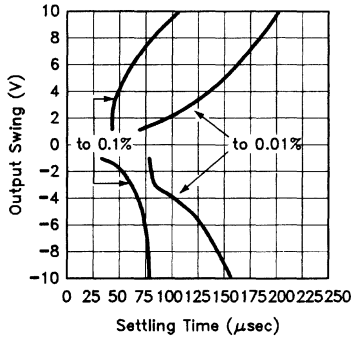
2029-17

Large-Signal Pulse Response—No Snubber



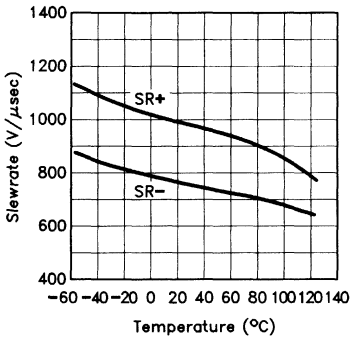
2029-18

Settling Time vs Output Swing



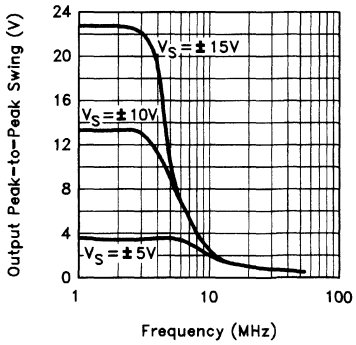
2029-19

Slew Rate vs Temperature



2029-20

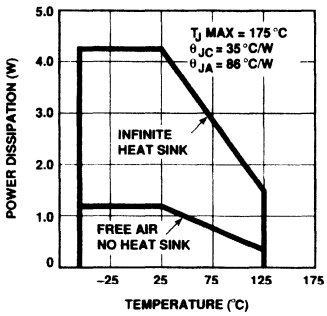
Output Swing vs Frequency for 5% Distortion



2029-21

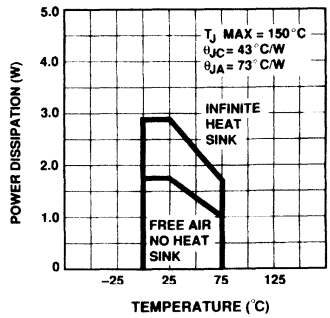
Typical Performance Curves — Contd.

14-Lead CerDIP
Maximum Power Dissipation
vs Ambient Temperature



2029-22

14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



2029-23

Applications Information

The EL2029 is a conventional high-accuracy operational amplifier with the speeds and bandwidths normally found only in current-feedback amplifiers. All the usual op amp configurations may be applied. The EL2029 will work well with a wide variety of loads and power supplies.

Power Supplies and Grounding

As with all high-frequency amplifiers, it is necessary to bypass the supply pins to ground close to the part. 0.01 μF capacitors of the ceramic type will suffice, although tantalum capacitors of any available value are perhaps the best choice. Tantalum capacitors have low series inductance yet are not high-Q in nature, helping to damp supply variations caused by load currents.

The EL2029 will work well from $\pm$5V supplies, with the input and output swings reduced to $\pm$1V over temperature, $\pm$2V nominally. At higher supplies, the part's dissipation must be maintained within package limits when the device and any load-related dissipations are calculated. Clip-on heatsinks are effective in reducing die temperature. Note that the device will warm approximately 36 degrees centigrade upon power-up: any accurate DC tests should either be done within 1 second or after 1 minute of turn-on at maximum supplies.

Although the part is current-limited at its output, that current can cause enough dissipation such that the maximum die temperature specification will be exceeded.

The EL2029 has a unique ground pin connection. The compensation capacitor returns to this pin rather than ground to aid in noise and settling characteristics. The input bias current compensation circuitry is also referred to this pin, so it cannot be connected to a voltage outside the input common-mode range.

Input Circuitry

The input appears as a high impedance even when the amplifier is overloaded. The input will not be damaged by transient nor continuous overloads, although an additional supply current of 4 mA per volt of overload will result. This should be considered in the device thermal calculations.

Like many other high-speed amplifiers, the input circuitry can resonate or even oscillate when driven by high-impedance inputs. The worst situation is when the device looks into an unterminated coaxial cable or a large inductance. Normal circuit interconnects cause no trouble. If the source impedance is difficult, a snubber similar to the output snubber can be added in parallel with the input.

High values of feedback impedance can sacrifice loop stability. The main point is that the pole caused by any stray capacitance and the feedback network impedance should be several times greater than the EL2029's gain-bandwidth product divided by the noise gain of the feedback loop. If this condition cannot be met, the feedback resistor can have a small (1–2 pF) capacitor in parallel to improve closed-loop phase margin.

Applications Information — Contd.

Output Circuitry

The output circuitry was designed to deliver more current than the device can safely continuously output so that the transient currents caused by fast slews can be developed. For instance, a 50 pF load will draw 45 mA in response to a 900 V/μs output transient. The snubber network will draw similar currents, and it may not be useable if the amplifier is called upon to deliver large outputs continuously at high frequencies. In any event, the device is rated at 30 mA continuously.

The output circuit will resonate with capacitive loads if it is not damped. The output impedance of all amplifiers is approximately modeled as an inductor in series with a DC resistance. The equivalent component values for the EL2029 are 300 nH and 20Ω. To reduce the output stage resonance with capacitive loads, the snubber network can be added to de-Q the load. The EL2029 will comfortably drive 100 pF with the snubber values of 100 pF and 100Ω.

Offset Adjust

To effect input offset voltage adjustment, a 10k to 100k potentiometer is connected to the balance pins with the wiper connected to V−. ±1.4 mV of adjustment is possible.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2030/EL2030C
120 MHz Current Feedback Amplifier

Features

- −3 dB bandwidth = 120 MHz, A_V = 1
- −3 dB bandwidth = 110 MHz, A_V = 2
- 0.01% differential gain and 0.01° differential phase (NTSC, PAL)
- 0.05% differential gain and 0.02° differential phase (HDTV)
- Slew rate 2000 V/μs
- 65 mA output current
- Drives ±10V into 200Ω load
- Characterized at ±5V and ±15V
- Low voltage noise
- Current mode feedback
- Settling time of 40 ns to 0.25% for a 10V step
- Output short circuit protected
- Low cost

Applications

- Video gain block
- Video distribution amplifier
- HDTV amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coax cable driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2030CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2030CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2030CJ	0°C to +75°C	14-Pin CerDIP	MDP0014
EL2030J	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2030J/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2030L	−55°C to +125°C	20-Pad LCC	MDP0007
EL2030L/883B	−55°C to +125°C	20-Pad LCC	MDP0007

General Description

The EL2030 is a very fast, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

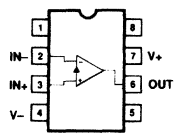
Due to its wide operating supply range (±15V) and extremely high slew rate of 2000 V/μs, the EL2030 drives ±10V into 200Ω at a frequency of 30 MHz, while achieving 110 MHz of small signal bandwidth or A_V = +2. This bandwidth is still 95 MHz for a gain of +10. On ±5V supplies the amplifier maintains a 90 MHz bandwidth for A_V = +2. When used as a unity gain buffer, the EL2030 has a 120 MHz bandwidth with the gain precision and low distortion of closed loop buffers.

The EL2030 features extremely low differential gain and phase, a low noise topology that reduces noise by a factor of 2 over competing amplifiers, and settling time of 40 ns to 0.25% for a 10V step. The output is short circuit protected. In addition, datasheet limits are guaranteed for ±15V and ±15V supplies.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: *Elantec's Military Processing, Monolithic Integrated Circuits.*

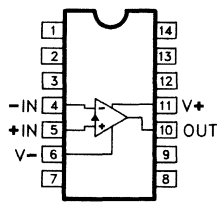
Connection Diagrams

Mini DIP



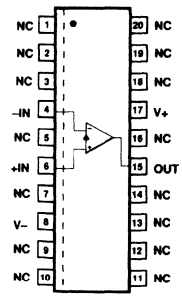
Top View

DIP



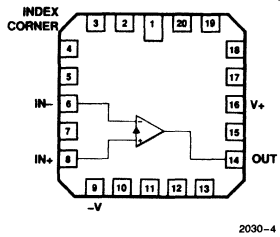
Top View

SOL



Top View

LCC



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

EL2030/EL2030C
120 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage	±15V or V_S		Ceramic Packages	175°C
ΔV_{IN}	Differential Input Voltage	±6V		Plastic Packages	150°C
P_D	Maximum Power Dissipation	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
I_{IN}	Input Current	±10 mA		Lead Temperature	
I_{OP}	Peak Output Current	Short Circuit Protected		DIP Package	300°C
	Output Short Circuit Duration	Continuous		(Soldering: <5 seconds—CN;	
	(Note 1)			<10 seconds—J)	
T_A	Operating Temperature Range			SOL Package	
	EL2030	−55°C to +125°C		Vapor Phase (60 seconds)	215°C
	EL2030C	0°C to +75°C		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±15V, R_L = 200Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level		Units
							EL2030	EL2030C	
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		10	20	I	I	mV
			T_{MIN}, T_{MAX}			30	I	III	mV
		V_S = ±5V	25°C		5	10	I	I	mV
			T_{MIN}, T_{MAX}			15	I	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				25		V	V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		5	15	I	I	µA
			T_{MIN}, T_{MAX}			25	I	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		10	40	I	I	µA
			T_{MIN}, T_{MAX}			50	I	III	µA
$+R_{IN}$	+Input Resistance		Full	1.1	2.0		I	II	MΩ
C_{IN}	Input Capacitance		25°C		1		V	V	pF
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	50	60		I	II	dB
−ICMR	Input Current Common		25°C		5	10	I	I	µA/V
	Mode Rejection (Note 2)		T_{MIN}, T_{MAX}			20	I	III	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	60	70		I	II	dB
+IPSR	+Input Current Power		25°C		0.1	0.5	I	II	µA/V
	Supply Rejection (Note 3)		T_{MIN}, T_{MAX}			1.0	I	III	µA/V
−IPSR	−Input Current Power		25°C		0.5	5.0	I	II	µA/V
	Supply Rejection (Note 3)		T_{MIN}, T_{MAX}			8.0	I	III	µA/V

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 200Ω, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level		Units
							EL2030	EL2030C	
R_{OL}	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$) V_{OUT} = ±10V	V_S = ±15V	25°C	88	150		I	II	V/mA
			T_{MIN}, T_{MAX}	75			I	III	V/mA
	V_{OUT} = ±2.5V (Note 6)	V_S = ±5V	25°C	80	120		I	II	V/mA
			T_{MIN}, T_{MAX}		70		I	III	V/mA
A_{VOL}	Open Loop DC Voltage Gain V_{OUT} = ±10V	V_S = ±15V	Full	60	70		I	II	dB
	V_{OUT} = ±2.5V (Note 6)	V_S = ±5V	Full	56	65		I	II	dB
V_O	Output Voltage Swing (Note 6)	V_S = ±15V	Full	12	13		I	II	V
		V_S = ±5V	Full	3	3.5		I	II	V
I_{OUT}	Output Current (Note 9)	V_S = ±15V	Full	60	65		I	II	mA
		V_S = ±5V	Full	30	35		I	II	mA
R_{OUT}	Output Resistance		25°C		5	18	V	V	Ω
I_S	Quiescent Supply Current		Full		15	21	I	II	mA
						21	I	III	mA
I_{SC}	Short Circuit Current		25°C		85		V	V	mA

Closed Loop AC Electrical Characteristics

V_S = ±15V, A_V = +2, R_F = 820Ω, R_G = 820Ω and R_L = 200Ω

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level		Units
							EL2030	EL2030C	
SR	Slew Rate (Note 7)		25°C	1200	2000		IV	IV	V/μs
FPBW	Full Power Bandwidth (Note 4)		25°C	19	31.8		IV	IV	MHz
t_r, t_f	Rise Time. Fall Time	V_{pp} = 250 mV	25°C		3		V	V	ns
t_s	Settling Time to 0.25% for 10V step (Note 5)		25°C		40		V	V	ns
ΔG	Differential Gain (Note 8)		25°C		0.01		V	V	% p-p
Δϕ	Differential Phase (Note 8)		25°C		0.01		V	V	° p-p
eN	Input Spot Noise at 1 kHz R_G = 101; R_F = 909		25°C		4		V	V	nV/√Hz

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_{CM} = ±10V for V_S = ±15V. For V_S = ±5V, V_{CM} = ±2.5V.
Note 3: V_{OS} is measured at V_S = ±4.5V and at V_S = ±18V. Both supplies are changed simultaneously.
Note 4: Full Power Bandwidth is specified based on Slew Rate measurement FPBW = $SR/2\pi V_P$.
Note 5: Settling Time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.
Note 6: R_L = 100Ω.
Note 7: V_O = ±10V, tested at V_O = ±5. See test circuit.
Note 8: NTSC (3.58 MHz) and PAL (4.43 MHz).
Note 9: For V_S = ±15V, V_{IN} = ±12V, V_{OUT} = ±10V. For V_S ±5V, V_{IN} = ±3.5V, V_{OUT} = ±2.5V.

EL2030/EL2030C
120 MHz Current Feedback Amplifier

Typical Performance Curves

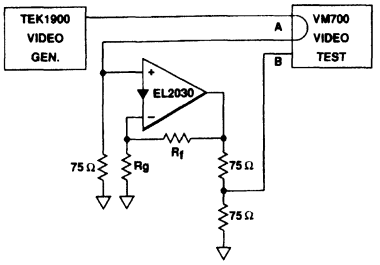


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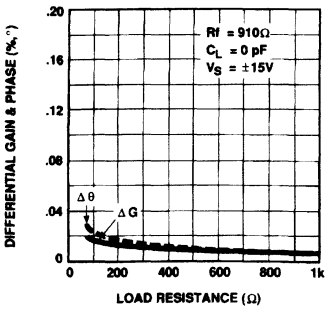
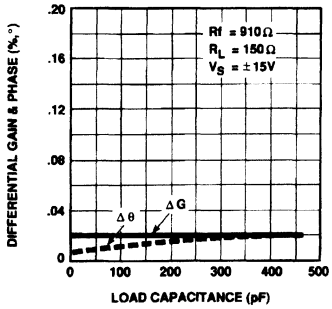
Figure 1. NTSC Video Differential Gain and Phase Test Set-Up

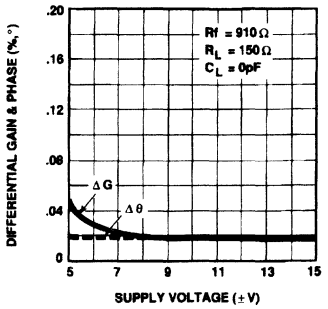
Differential Gain and Phase vs Load Resistance, Gain = +1



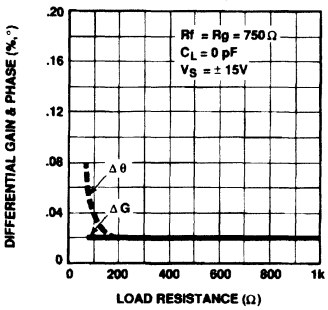
Differential Gain and Phase vs Load Capacitance, Gain = +1



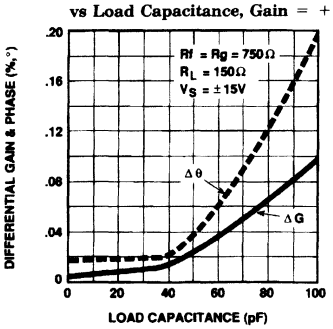
Differential Gain and Phase vs Supply Voltage, Gain = +1



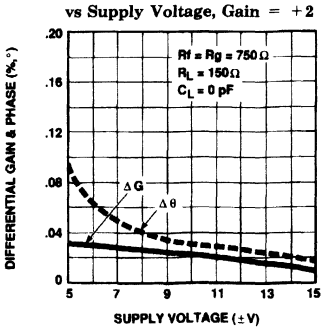
Differential Gain and Phase vs Load Resistance, Gain = +2



Differential Gain and Phase vs Load Capacitance, Gain = +2



Differential Gain and Phase vs Supply Voltage, Gain = +2



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Typical Performance Curves — Contd.

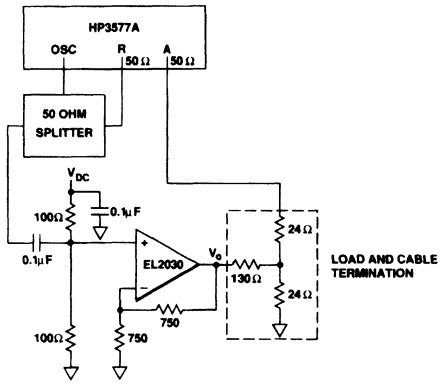
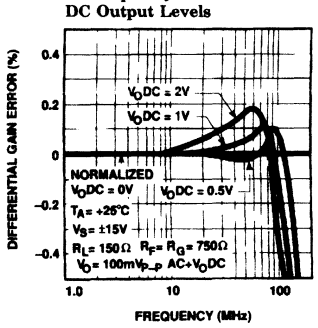
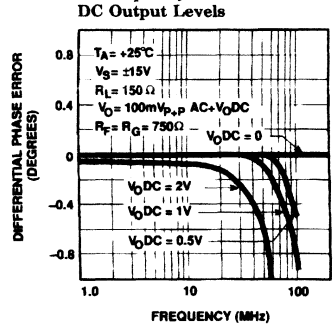


Figure 2. HDTV and Wideband Video Differential Gain and Phase Test Set-Up

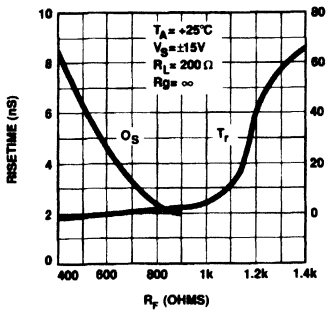
Differential Gain Error vs Frequency for Various DC Output Levels



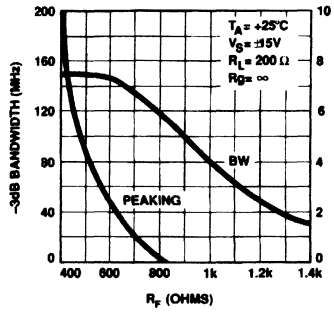
Differential Phase Error vs Frequency for Various DC Output Levels



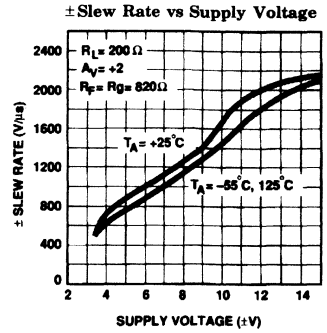
Risetime and Overshoot vs R_F for A_V = +1



Bandwidth and Peaking vs R_F for A_V = +1



±Slew Rate vs Supply Voltage



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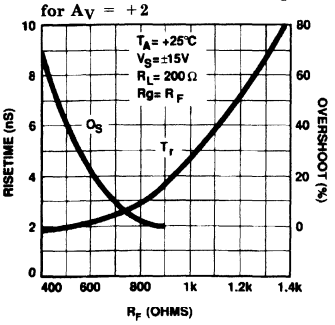
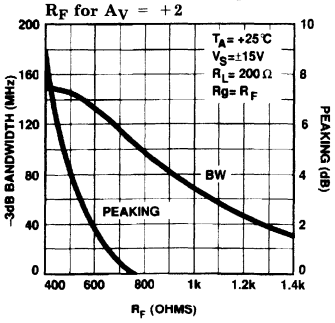
120 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

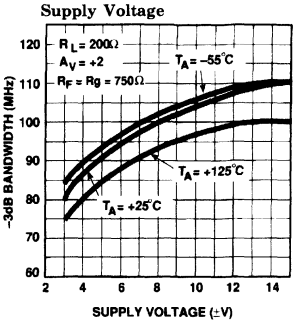
Risetime and Overshoot vs R_F for $A_V = +2$



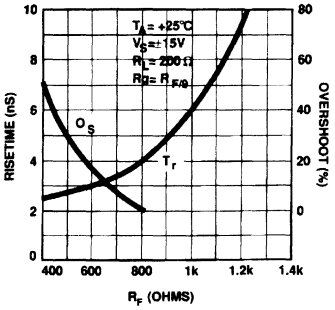
Bandwidth and Peaking vs R_F for $A_V = +2$



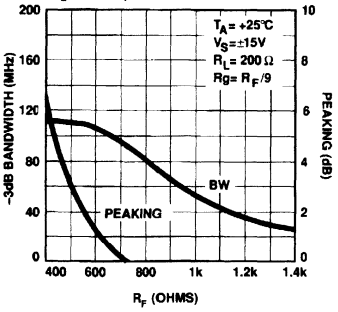
−3 dB Bandwidth vs Supply Voltage



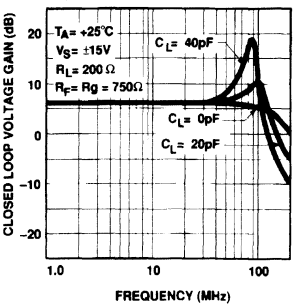
Risetime and Overshoot vs R_F for $A_V = +10$



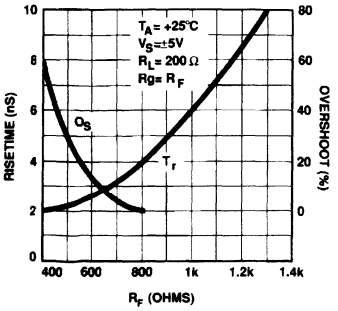
Bandwidth and Peaking vs R_F for $A_V = +10$



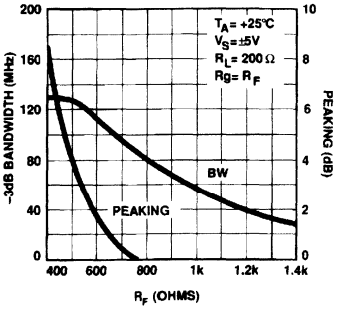
Voltage Gain vs Frequency for $A_V = +2$, various Capacitive Loads



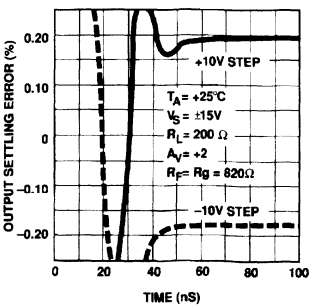
Risetime and Overshoot vs R_F for $A_V = +2$, $V_S = \pm 5V$



Bandwidth and Peaking vs R_F for $A_V = +2$, $V_S = +5V$



Output Settling Error vs Time



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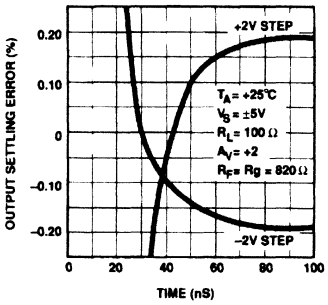
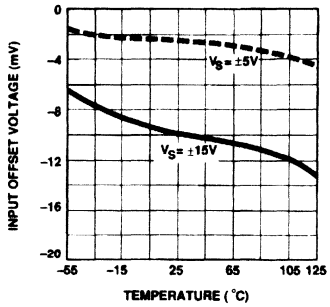
Typical Performance Curves — Contd.

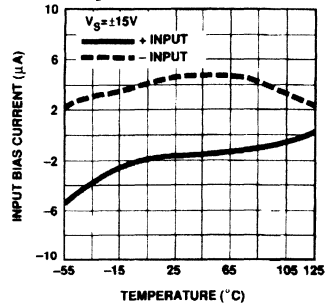
Output Settling Error vs Time, V_S = ±5V



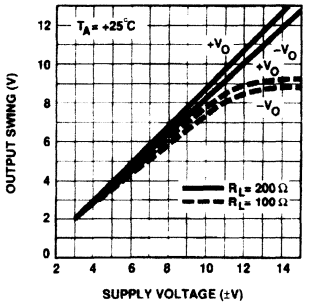
Input Offset Voltage vs Temperature



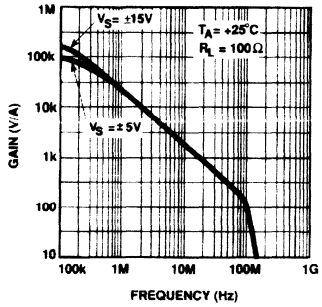
Input Bias Current vs Temperature



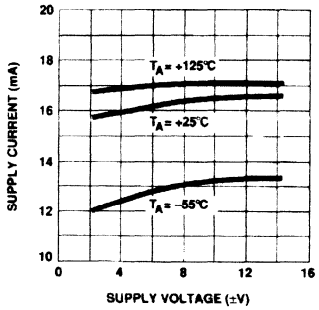
Output Swing vs Supply Voltage



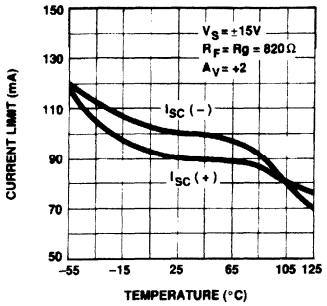
Transimpedance (R_{OL})



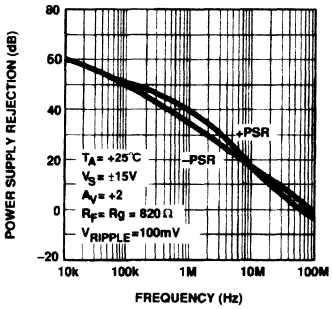
Supply Current vs Supply Voltage



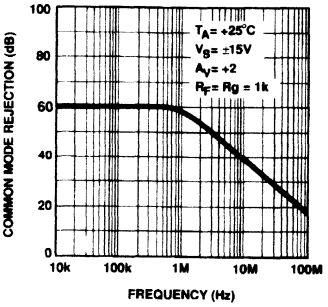
Current Limit vs Temperature



Power Supply Rejection vs Frequency



Common Mode Rejection vs Frequency



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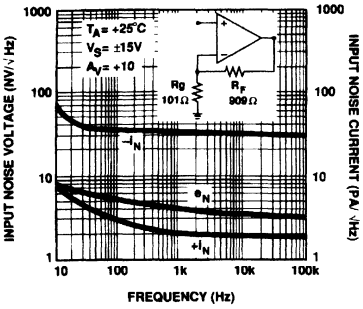
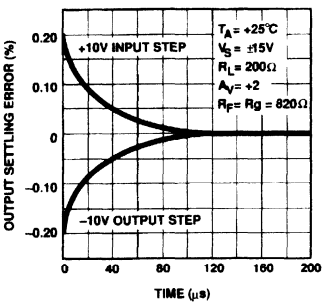
120 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

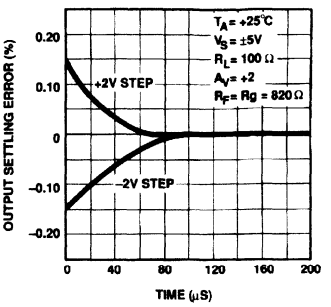
Equivalent Input Noise



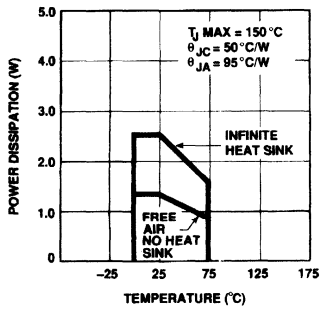
Long-Term Output Settling Error vs Time



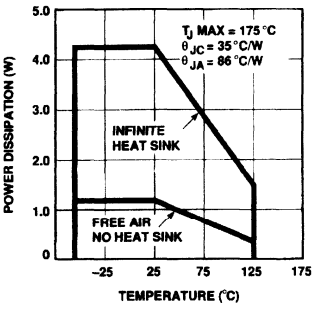
Long-Term Output Settling Error vs Time, V_S = ±5V



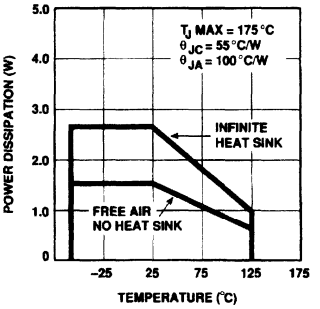
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



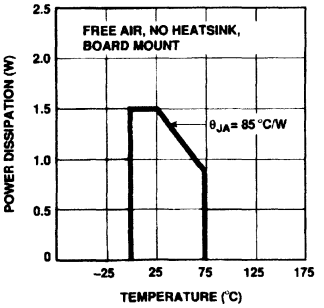
14-Lead CerDIP
Maximum Power Dissipation
vs Ambient Temperature



20-Pad LCC
Maximum Power Dissipation
vs Ambient Temperature



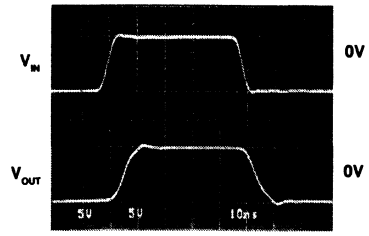
20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2030-11

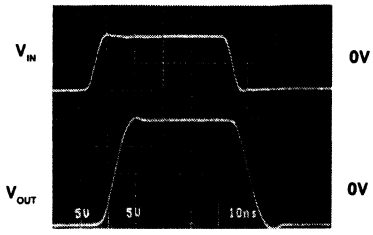
Typical Performance Curves — Contd.

Large Signal Response



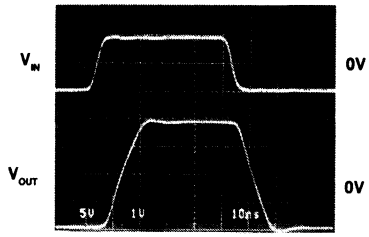
$A_V = +1$, $R_F = 1\ k\Omega$, $R_L = 200\Omega$, $V_S = \pm 15V$ 2030-12

Large Signal Response



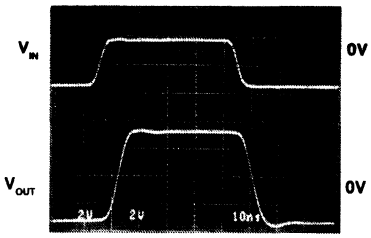
$A_V = +2$, $R_F = R_G = 820$, $R_L = 200\Omega$, $V_S = \pm 15V$ 2030-13

Large Signal Response



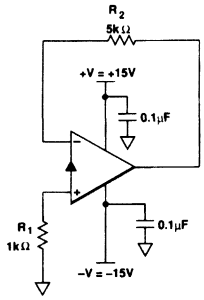
$A_V = +10$, $R_F = 750$, $R_G = 82\Omega$, $R_L = 200\Omega$, $V_S = \pm 15V$ 2030-14

Large Signal Response



$A_V = +2$, $R_F = R_G = 750\Omega$, $R_L = 200\Omega$, $V_S = \pm 15V$ 2030-15

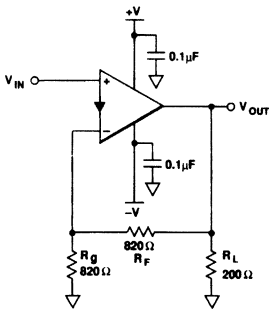
Burn-In Circuit



2030-16

ALL PACKAGES USE THE SAME SCHEMATIC.

Test Circuit



2030-17

EL2030/EL2030C
120 MHz Current Feedback Amplifier

Application Information

Product Description

The EL2030 is a current mode feedback amplifier similar to the industry standard EL2020, but with greatly improved AC characteristics. Most significant among these are the extremely wide bandwidth and very low differential gain and phase. In addition, the EL2030 is fully characterized and tested at ±5V and ±15V supplies.

Power Supply Bypassing/Lead Dressing

It is important to bypass the power supplies of the EL2030 with 0.1 μF ceramic disc capacitors. Although the lead length is not critical, it should not be more the ½ inch from the IC pins. Failure to do this will result in oscillation, and possible destruction of the part. Another important detail is the lead length of the inputs. The inputs should be designed with minimum stray capacitance and short lead lengths to avoid ringing and distortion.

Differential Gain and Differential Phase

Composite video signals contain intensity, color, hue, timing and audio information in AM, FM, and Phase Modulation. These video signals pass through many stages during their production, processing, archiving and transmission. It is important that each stage not corrupt these signals to provide a "high fidelity" image to the end viewer.

An industry standard way of measuring the distortion of a video component (or system) is to measure the amount of differential gain and phase error it introduces. A 100 mV peak to peak sine wave at 3.58 MHz for NTSC (4.3 MHz for PAL), with 0V DC component serves as the reference. The reference signal is added to a DC offset, shifting the sine wave from 0V to 0.7V which is then applied to the device under test (DUT). The output signal from the DUT is compared to the reference signal. The Differential Gain is a measure of the change in amplitude of the sine wave and is measured in percent. The Differential Phase is a measure of the change in the phase of the sine wave and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak differential gain and differential phase errors. The test setup in Figure 1 was used to characterize the EL2030. For higher than NTSC and PAL frequencies, an alternate Differential Gain and Phase measurement can be made using an HP3577A Network Analyser and the setup shown in Figure 2. The frequency response is normalized to gain or phase with 0V DC at the input. From the normalized value a DC offset voltage is introduced and the Differential Gain or Phase is the deviation from the normalized value.

Video Applications

The video signals that must be transmitted for modest distances are usually amplified by a device such as the EL2030 and carried via coax cable. There are at least two ways to drive cables, single terminated and double terminated.

When driving a cable, it is important to terminate it properly to avoid unwanted signal reflections. Single termination (75Ω to ground at receive end) may be sufficient for less demanding applications. In general, a double terminated cable (75Ω in series at drive end and 75Ω to ground at receive end) is preferred since the impedance match at both ends of the line will absorb signal reflections. However, when double termination is used (a total impedance of 150Ω), the received signal is reduced by half; therefore, the amplifier is usually set at a gain of 2 or higher to compensate for attenuation.

Video signals are 1V peak-peak in amplitude, from sync tip to peak white. There are 100 IRE (0.714V) of picture (from black to peak white of the transmitted signal) and 40 IRE (0.286V) of sync in a composite video signal (140 IRE = 1V).

For video applications where a gain of two is used (double termination), the output of the video amplifier will be a maximum of 2V peak-peak. With ±5V power supply, the EL2030 output swing of 3.5V is sufficient to satisfy the video output swing requirements. The EL2030 can drive two double terminated coax cables under these conditions. With ±15V supplies, driving four double terminated cables is feasible.

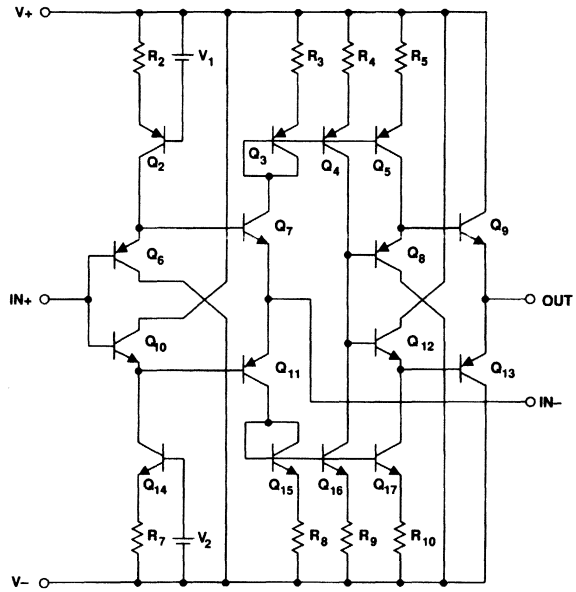
Video Applications — Contd.

Although the EL2030's video characteristics (differential gain and phase) are impressive with ±5V supplies at NTSC and PAL frequencies, it can be optimized when the supplies are increased to ±15V, especially at 30 MHz HDTV applications. This is primarily due to a reduction in internal parasitic junction capacitance with increased power supply voltage.

The following table summarizes the behavior of the EL2030 at ±5V and ±15V for NTSC. In addition, 30 MHz HDTV data is included. Refer to the differential gain and phase typical performance curves for more data.

$\pm V_S$	Rload	A_V	ΔGain	ΔPhase	Comments
15V	75Ω	1	0.02%	0.03°	Single terminated
15V	150Ω	1	0.02%	0.02°	Double terminated
5V	150Ω	1	0.05%	0.02°	Double terminated
15V	75Ω	2	0.02%	0.08°	Single terminated
15V	150Ω	2	0.01%	0.02°	Double terminated
5V	150Ω	2	0.03%	0.09°	Double terminated
15V	150Ω	2	0.05%	0.02°	HDTV, Double terminated

Equivalent Circuit



2030-18

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2038/EL2038C
1 GHz Operational Amplifier

Features

- Wide gain-bandwidth—1 GHz
- High slew rate—1000 V/μs
- High power bandwidth—16 MHz
- Low offset voltage—0.5 mV
- Low supply current—13 mA
- Standard ±15V op amp supplies
- Large Open Loop Gain—15 kV/V (83 dB)
- MIL-STD-883 Rev. C Compliant
- Output voltage swing ±11V

Applications

- Pulse and Video amplifiers
- Wideband amplifiers
- High speed sample-hold circuits
- Local area Networks

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2038CJ	0°C to +75°C	CerDIP	MDP0014
EL2038CN	0°C to +75°C	P-DIP	MDP0012
EL2038J	−55°C to +125°C	CerDIP	MDP0014
EL2038J/883B	−55°C to +125°C	CerDIP	MDP0014
EL2038L/883B	−55°C to +125°C	20-Pad LCC	MDP0007

General Description

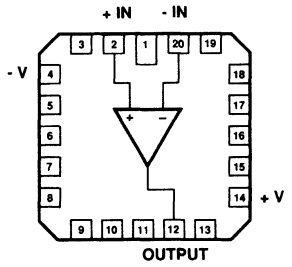
The EL2038 monolithic operational amplifier offers a 1 GHz gain-bandwidth and 1000 V/μs slew rate with excellent DC accuracy. The EL2038 is 67% faster than the HA2539 but with a typical power reduction of 35%. This patented amplifier is stable when driving capacitive loads and is well behaved when the output is overdriven. The EL2038 is compensated for closed loop gains ≥ 20. The EL2038 is fabricated with Elantec's Complementary Bipolar process, and is zener zap trimmed for low offset voltage.

Elantec's high speed amplifiers are widely used in military, video and medical applications. The EL2038 is especially well-suited for high speed video amplifiers, pulse detectors and wide bandwidth filters.

Elantec's EL2038/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

EL2038L



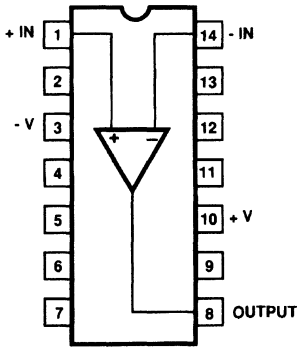
2038-1

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EL2038J EL2038CN



2038-2

Top View

EL2038/EL2038C
1 GHz Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Operating Temperature Range	
Differential Input Voltage	6V	EL2038	−55°C to +125°C
Output Current	50 mA (Peak)	EL2038C	0°C to +75°C
	30 mA (Continuous)	Operating Junction Temperature	
Internal Power Dissipation	See Curves	CerDIP, Ceramic LCC	175°C
		Plastic DIP	150°C
		Lead Temperature (Soldering, 5 seconds)	300°C
		Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ; unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	EL2038 Test Level	EL2038C Test Level	Units
V_{OS}	Offset Voltage	+25°C		0.5	2	I	I	mV
		Full			6	I	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	V	µV/°C
I_B	Bias Current	+25°C		5	15	I	I	µA
		Full			20	I	III	µA
I_{OS}	Offset Current	+25°C		1	4	I	I	µA
		Full			6	I	III	µA
R_{IN}	Input Resistance	+25°C		10		V	V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V	V	pF
V_{CM}	Common Mode Input Range	Full	±11	±12		I	II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		6		V	V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain	+25°C	10k	15k		I	I	V/V
	(Notes 1, 2)	Full	5k			I	III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	60	90		I	II	dB
V_O	Output Voltage Swing (Note 1)	Full	±11	±12		I	II	V

EL2038/EL2038C
1 GHz Operational Amplifier

DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ; unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	EL2038 Test Level	EL2038C Test Level	Units
I_O	Output Current (Note 13)	Full	±25	±50		I	II	mA
R_O	Output Resistance	+25°C		30		V	V	Ω
I_S	Supply Current	Full		13	17	I	II	mA
PSRR	Power Supply Rejection Ratio (Note 8)	Full	60	85		I	II	dB

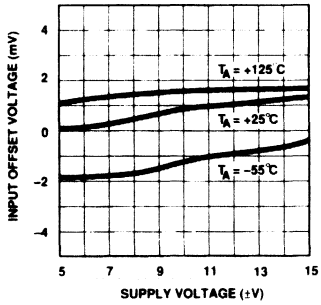
AC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, unless otherwise specified (Note 14)

Parameter	Description	Temp	Min	Typ	Max	EL2038 Test Level	EL2038C Test Level	Units
GBW	Gain-Bandwidth Product (Notes 4, 5)	+25°C	0.875	1.1		I	III	GHz
FPBW	Full Power Bandwidth (Notes 1, 2, 6)	+25°C	13.5	16		I	III	MHz
t_r	Rise Time (Notes 7, 9)	+25°C		4	5	I	III	ns
OS	Overshoot (Notes 7, 10)	+25°C		30	40	I	III	%
SR	Slew Rate (Note 7)	+25°C	850	1000		I	III	V/μs
t_s	Settling Time (Notes 11, 12) 10V Step to 0.1%	+25°C		100		V	V	ns

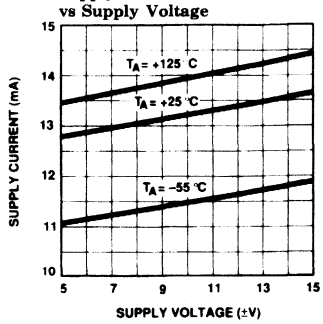
Note 1: R_L = 1k, C_L < 10 pF.
Note 2: V_O = ±10V.
Note 3: Two tests are performed, V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 4: V_O = 90 mV.
Note 5: A_V = 20.
Note 6: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew rate}}{2\pi V_{peak}}$.
Note 7: Refer to Test Circuits section of data sheet.
Note 8: Two tests are performed, V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 9: Risetime measurement of 10% to 90% with V_{OUT} = 200 mV.
Note 10: ΔV_O = 200 mV.
Note 11: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 12: A_V = −20, R_L = 1k.
Note 13: R_L = 200Ω.
Note 14: 100% AC tested commercial parts available. Consult factory.

Typical Performance Curves

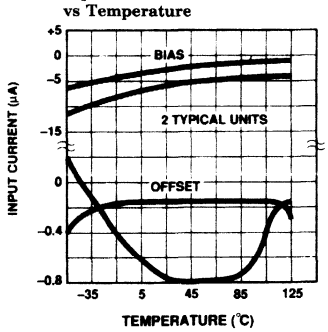
Input Offset Voltage
vs Supply Voltage



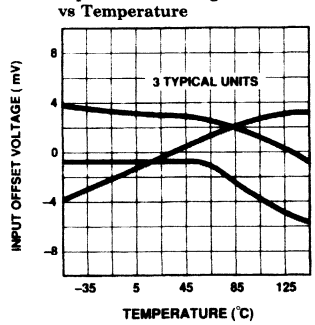
Supply Current
vs Supply Voltage



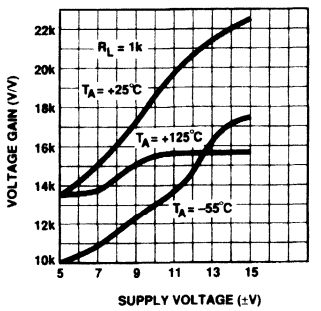
Input Currents
vs Temperature



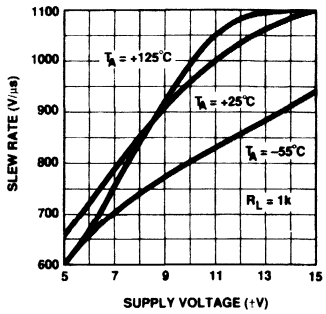
Input Offset Voltage
vs Temperature



Voltage Gain
vs Supply Voltage



Slew Rate
vs Supply Voltage

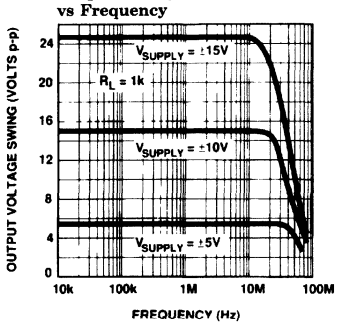


2038-3

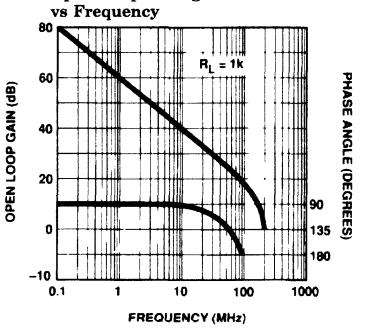
EL2038/EL2038C
1 GHz Operational Amplifier

Typical Performance Curves — Contd.

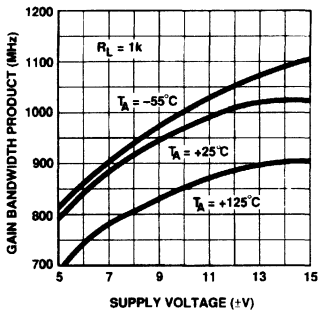
Output Voltage Swing vs Frequency



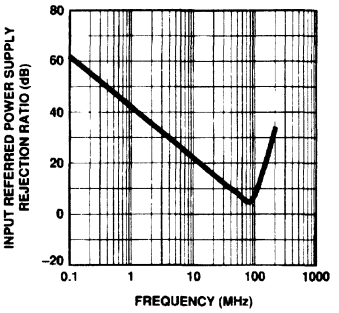
Open Loop Voltage Gain vs Frequency



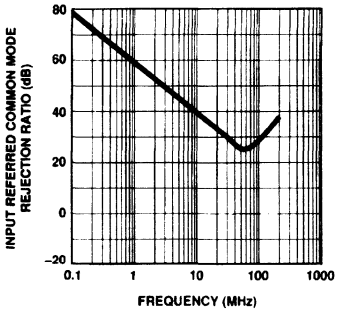
Gain Bandwidth Product at 10 MHz vs Frequency



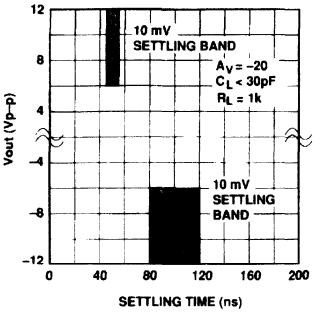
Input Referred Power Supply Rejection Ratio vs Frequency



Input Referred Common Mode Rejection Ratio vs Frequency



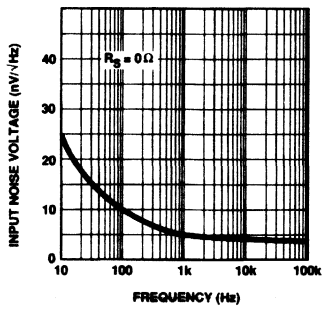
Settling Time



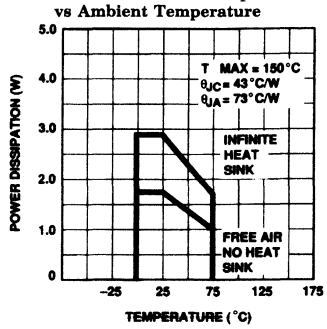
2038–4

Typical Performance Curves — Contd.

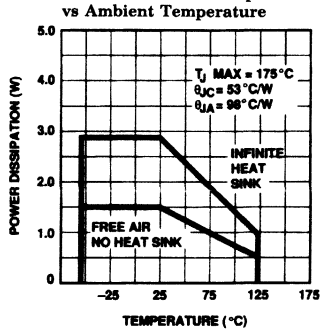
Input Noise Voltage
vs Frequency



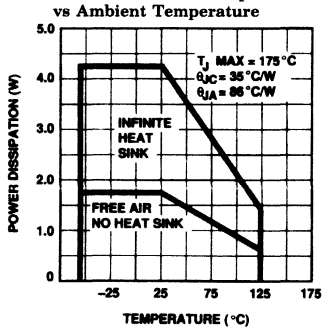
14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



20-Lead LCC
Maximum Power Dissipation
vs Ambient Temperature

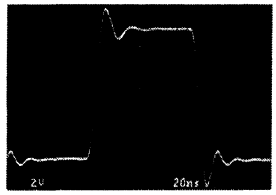


14-Lead CerDIP
Maximum Power Dissipation
vs Ambient Temperature



2038-5

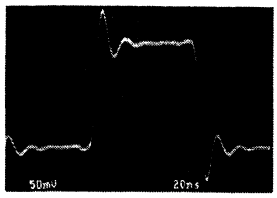
Large Signal Response



V_{IN} = ±0.25V
V_O = ±5V

2038-6

Small Signal Response

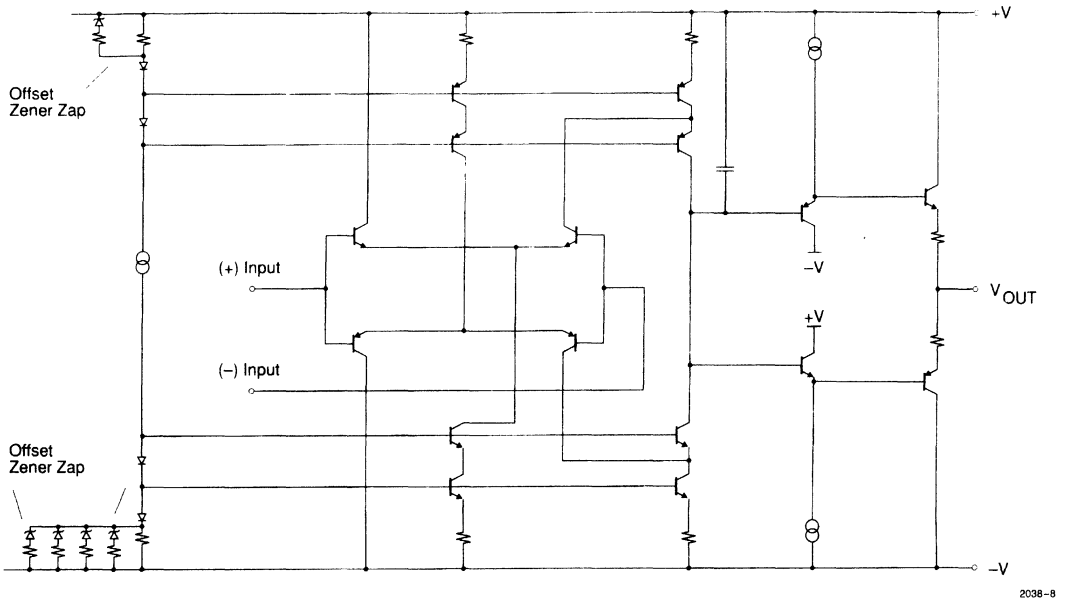


V_{IN} = ±5 mV
V_O = ±100 mV

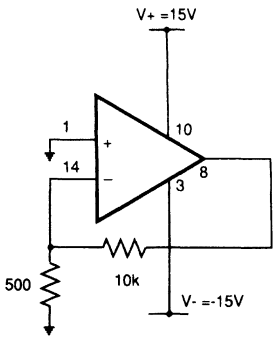
2038-7

EL2038/EL2038C
1 GHz Operational Amplifier

Simplified Schematic

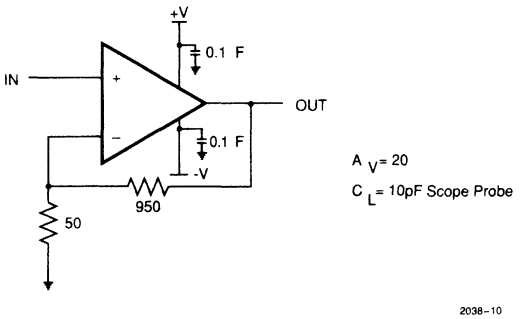


Burn-In Circuit



Pin numbers are for 14-Lead CerDIP. All packages use the same schematic.

Test Circuit



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EHA2539/EHA2540

Very High Slew Rate Wideband Operational Amplifier

Features

- High Slew Rate
  EHA2539—600 V/μs
  EHA2540—400 V/μs
- Large open loop gain 15 kV/V (83 dB)
- Wide gain bandwidth
  EHA2539—600 MHz
  EHA2540—400 MHz
- Power bandwidth
  EHA2539—9.5 MHz
  EHA2540—6.3 MHz
- Low offset voltage 0.5 mV
- Low supply current 13 mA
- Output voltage swing ±10V
- MIL-STD-883 Rev. C compliant
- Exact replacements for HA2539 and HA2540

Applications

- Pulse and video amplifiers
- Wideband amplifiers
- High speed sample-hold circuits
- Local area networks

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EHA1-2539-2	−55°C to +125°C	14-Pin CerDIP	MDP0014
EHA1-2539-5	0°C to +75°C	14-Pin CerDIP	MDP0014
EHA1-2539/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EHA3-2539-5	0°C to +75°C	14-Pin P-DIP	MDP0031
EHA4-2539/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EHA1-2540-2	−55°C to +125°C	14-Pin CerDIP	MDP0014
EHA1-2540-5	0°C to +75°C	14-Pin CerDIP	MDP0014
EHA1-2540/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EHA3-2540-5	0°C to +75°C	14-Pin P-DIP	MDP0031
EHA4-2540/883B	−55°C to +125°C	20-Pad LCC	MDP0007

General Description

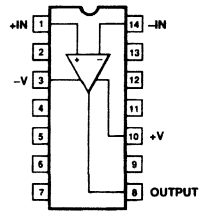
The EHA2539 and EHA2540 monolithic amplifiers are exact replacements for the HA2539 and HA2540 amplifiers. These Elantec amplifiers are well behaved in the presence of capacitive loading, and are stable for closed loop gains of 10 or greater. The EHA2539 is the fastest in the series with a 600 V/μs Slew Rate and 600 MHz gain bandwidth, while the EHA2540 slews at 400 V/μs and has a 400 MHz gain bandwidth. Both amplifiers are fabricated using Elantec's Complementary Bipolar process. For improved guaranteed specifications on offset voltage and supply current see the EL2039/EL2040.

Elantec's high speed amplifiers are widely used in military, video and medical applications. They are especially suited for high speed video amplifiers, pulse detectors, and wide bandwidth filters.

Elantec's EHA2539/883B and EHA2540/883B comply with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

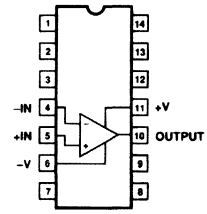
EHA1-2539 EHA3-2539



2539-1

Top View

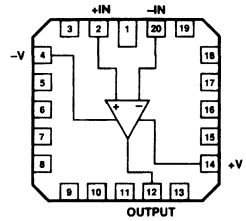
EHA1-2540 EHA3-2540



2539-2

Top View

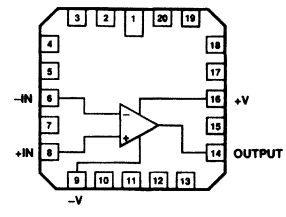
EHA4-2539



2539-3

Top View

EHA4-2540



2539-4

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EHA2539/EHA2540

Very High Slew Rate Wideband Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
V_{DIFF}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
P_D	Internal Power Dissipation	See Curves
T_A	Operating Temperature Range	
	−2, /883B	−55°C to +125°C
	−5	0°C to +75°C
T_J	Operating Junction Temperature	
	CerDIP, Ceramic LCC	175°C
	Plastic DIP	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
T_{LT}	Lead Temperature	
	(Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ; unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	−2, /883B Test Level	−5 Test Level	Units
V_{OS}	Offset Voltage (−2, /883B)	25°C		0.5	10	I		mV
		Full			15	I		mV
V_{OS}	Offset Voltage (−5)	25°C		0.5	15		I	mV
		Full			20		III	μV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	V	μV/°C
I_B	Bias Current	25°C		5	20	I	I	μA
		Full			25	I	III	μA
I_{OS}	Offset Current	25°C		1	6	I	I	μA
		Full			8	I	III	μA
R_{IN}	Input Resistance	25°C		10		V	V	kΩ
C_{IN}	Input Capacitance	25°C		1		V	V	pF
V_{CM}	Common Mode Range	Full	±10	±12		I	II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		6		V	V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Note 1)	25°C	10k	15k		I	I	V/V
		Full	5k			I	III	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	Full	60	90		I	II	dB
V_O	Output Voltage Swing	Full	±10			I	II	V
I_O	Output Current	Full	±10			I	II	mA
R_O	Output Resistance	25°C		30		V	V	Ω
I_S	Supply Current	Full		13	25	I	II	mA
PSRR	Power Supply Rejection Ratio (Note 7)	Full	60	85		I	II	dB

AC Electrical Characteristics—EHA2539

Parameter	Description	Temp	Min	Typ	Max	−2, /883B Test Level	−5 Test Level	Units
GBW	Gain-Bandwidth Product (Notes 3, 4)	25°C		600		V	V	MHz
FPBW	Full Power Bandwidth (Notes 1, 5, 8)	25°C	8.7	9.5		I	I	MHz
t_r	Rise Time (Note 6)	25°C		7		V	V	ns
OS	Overshoot (Note 6)	25°C		35		V	V	%
SR	Slew Rate (Note 6)	25°C	550	600		I	I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.1%	25°C		100		V	V	ns

AC Electrical Characteristics—EHA2540

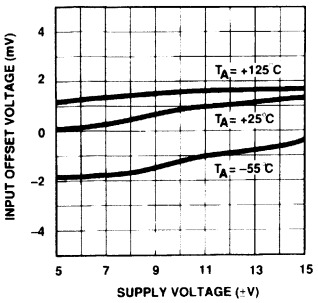
Parameter	Description	Temp	Min	Typ	Max	−2, /883B Test Level	−5 Test Level	Units
GBW	Gain-Bandwidth Product (Notes 3, 4)	25°C		400		V	V	MHz
FPBW	Full Power Bandwidth (Notes 1, 5, 8)	25°C	5.5	6		I	I	MHz
t_r	Rise Time (Note 6)	25°C		14		V	V	ns
OS	Overshoot (Note 6)	25°C		15		V	V	%
SR	Slew Rate (Note 6)	25°C	350	400		I	I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.1%	25°C		70		V	V	ns

Note 1: $V_O = \pm 10V$.
Note 2: Two tests are performed. V_{CM} = 0V to 10V and V_{CM} = 0V to −10V.
Note 3: V_O = 90 mV.
Note 4: A_V = 10.
Note 5: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
Note 6: Refer to Test Circuits section of data sheet.
Note 7: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from 5V to 15V.
Note 8: R_L = 1 kΩ.
Note 9: Settling time measurements are made with techniques in the following reference: "Take the Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 10: A_V = −10, R_L = 1k.

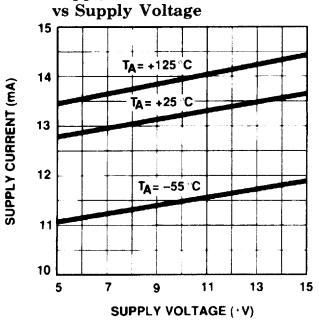
EHA2539/EHA2540
Very High Slew Rate Wideband Operational Amplifier

EHA2539/EHA2540 Typical DC Performance Curves

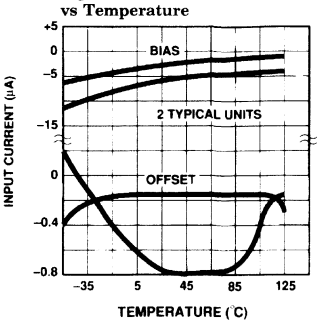
Input Offset Voltage vs Supply Voltage



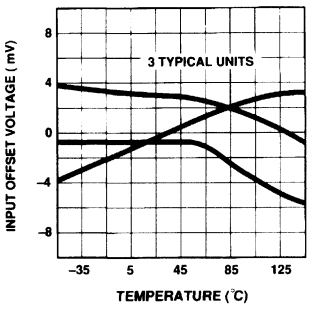
Supply Current vs Supply Voltage



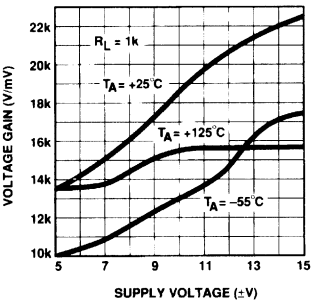
Input Currents vs Temperature



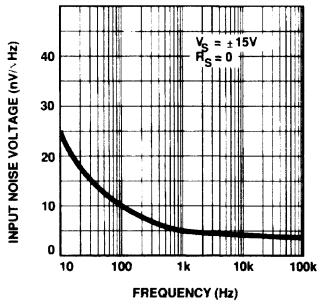
Input Offset Voltage vs Temperature



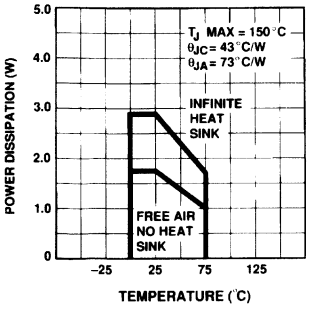
Voltage Gain vs Supply Voltage



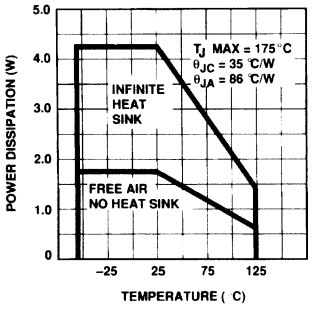
Input Noise Voltage vs Frequency



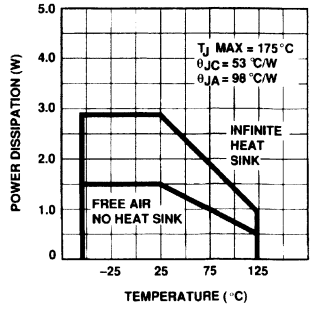
14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



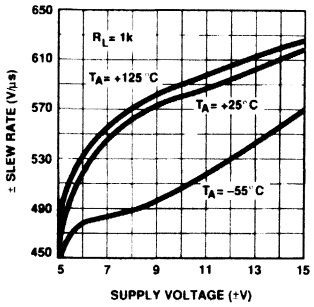
20-Lead LCC Maximum Power Dissipation vs Ambient Temperature



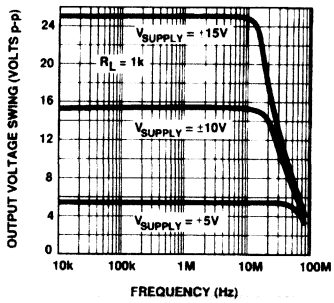
2539-5

EHA2539 Typical AC Performance Curves

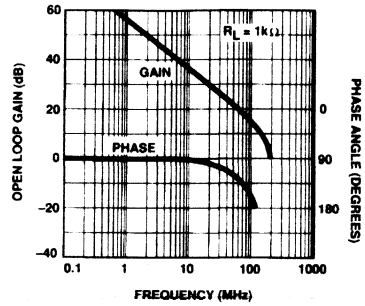
Slew Rate vs Supply Voltage



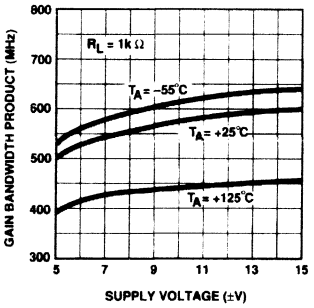
Output Voltage Swing vs Frequency



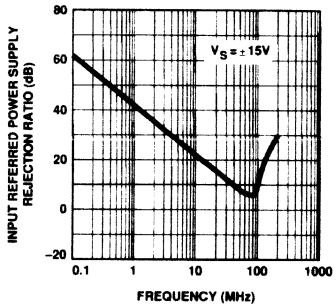
Open Loop Voltage Gain vs Frequency



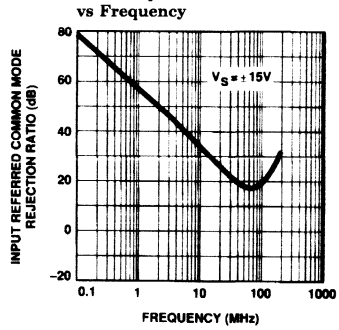
Gain Bandwidth Product at 10 MHz vs Supply Voltage



Input Referred Power Supply Rejection Ratio vs Frequency

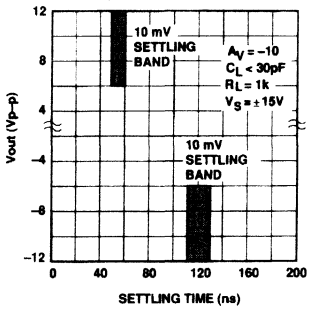


Input Referred Common Mode Rejection Ratio vs Frequency



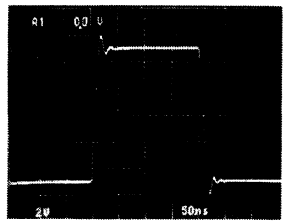
2539-6

Settling Time



2539-7

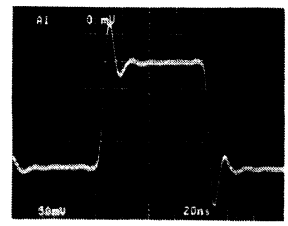
Large Signal Response



V_{IN} = ±0.5V
V_O = ±5V

2539-8

Small Signal Response



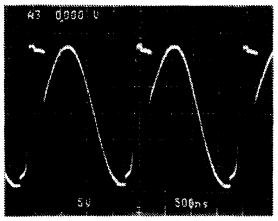
V_{IN} = ±10 mV
V_O = ±100 mA

2539-9

EHA2539/EHA2540
Very High Slew Rate Wideband Operational Amplifier

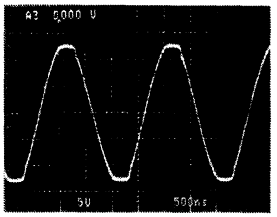
EHA2539 Typical AC Performance Curves — Contd.

EHA2539 at Onset of Clipping



2539-10

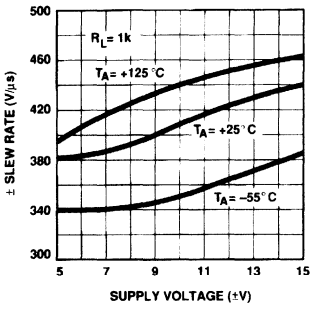
EHA2539 at Onset of Clipping



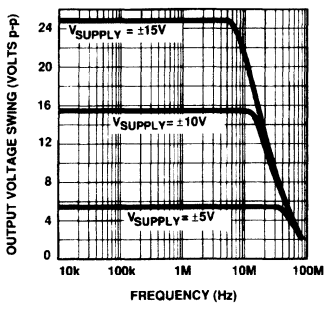
2539-11

EHA2540 Typical AC Performance Curves

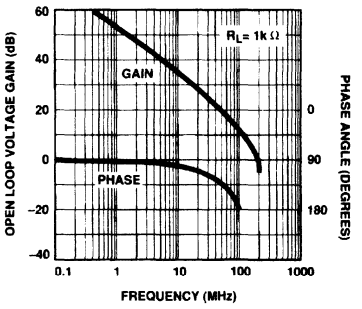
±Slew Rate vs Supply Voltage



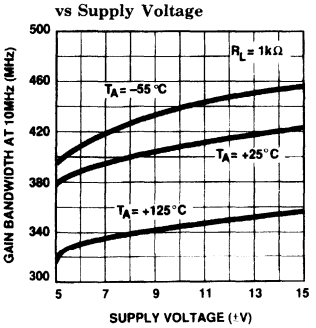
Output Voltage Swing vs Frequency



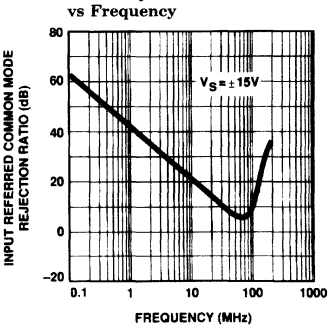
Open Loop Voltage Gain vs Frequency



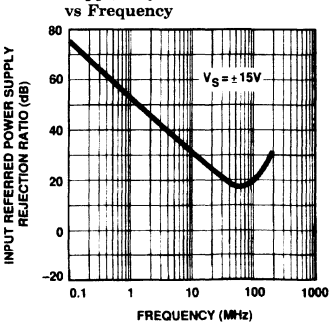
Gain Bandwidth Product at 10 MHz vs Supply Voltage



Input Referred Common Mode Rejection Ratio vs Frequency



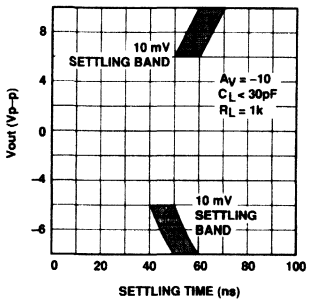
Input Referred Power Supply Rejection Ratio vs Frequency



2539-12

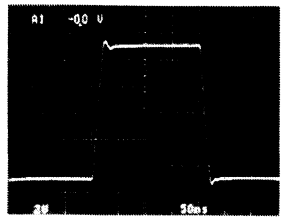
EHA2540 Typical AC Performance Curves — Contd.

Settling Time



2539-13

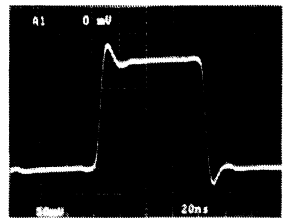
Large Signal Response



V_{IN} = ±0.5V
V_O = ±5V

2539-14

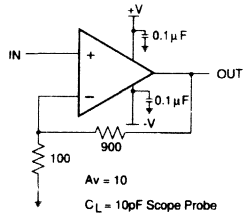
Small Signal Response



V_{IN} = ±10 mV
V_O = ±100 mV

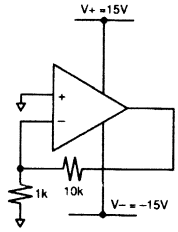
2539-15

Test Circuit



2539-16

Burn-In Circuit

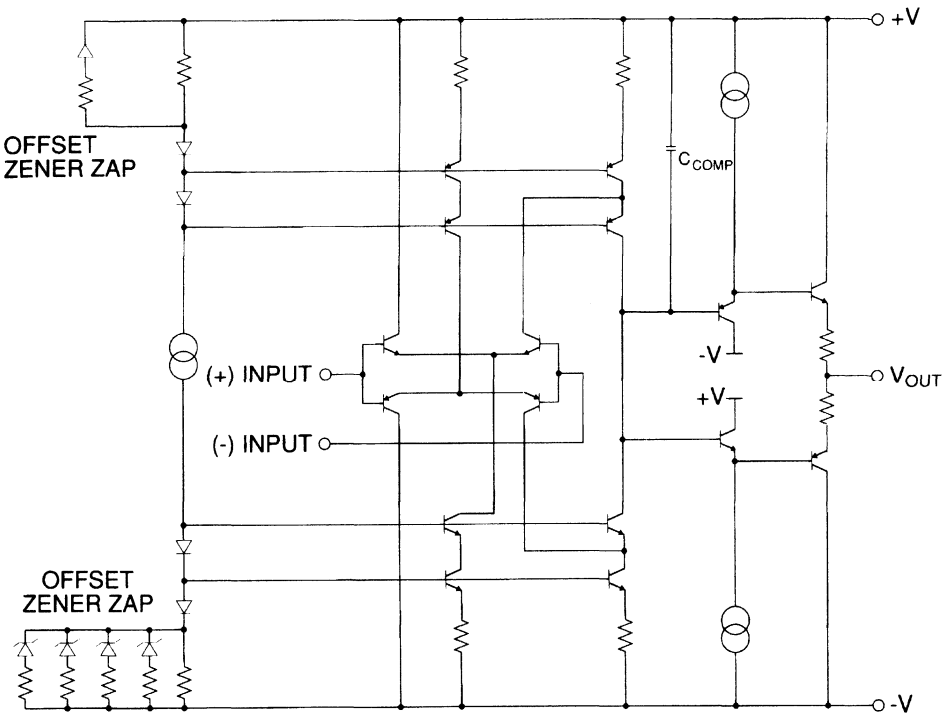


2539-17

EHA2539/EHA2540

Very High Slew Rate Wideband Operational Amplifier

Schematic



2539-18

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2039/EL2040

Very High Slew Rate Wideband Operational Amplifier

Features

- Low offset voltage—0.5 mV typ., 2 mV max
- Low supply current—13 mA typ., 17 mA max
- High slew rate—
  EL2039—600 V/μs
  EL2040—400 V/μs
- Large open loop gain—15 kV/V (83 dB)
- Wide gain-bandwidth—
  EL2039—600 MHz
  EL2040—400 MHz
- High power bandwidth—
  EL2039—9.5 MHz
  EL2040—6.3 MHz
- Output voltage swing—± 11V
- MIL-STD-883 Rev. C compliant
- Improved replacements for HA2539 and HA2540

Applications

- Pulse and video amplifiers
- Wideband amplifiers
- High speed sample-hold circuits
- Local area networks

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2039CJ	0°C to +75°C	14-Pin CerDIP	MDP0014
EL2039CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2039J	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2039J/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2039L/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EL2040CJ	0°C to +75°C	14-Pin CerDIP	MDP0014
EL2040CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2040J	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2040J/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2040L/883B	−55°C to +125°C	20-Pad LCC	MDP0007

General Description

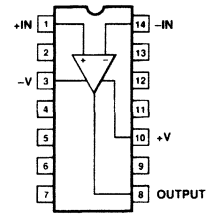
The EL2039 and EL2040 monolithic operational amplifiers are pin compatible with the HA2539 and HA2540, but have patented circuitry for improved dynamic performance and DC accuracy, and a typical power reduction of 35%. Additionally, these Elantec amplifiers are stable when driving capacitive loads and are well behaved when the output is overdriven. Both devices are compensated for closed loop gains ≥ 10. The EL2039 is the fastest of the series with a 600 V/μs slew rate and 600 MHz gain-bandwidth product. The EL2040 has a 400 V/μs slew rate and 400 MHz gain-bandwidth product. The EL2039 and EL2040 are fabricated with Elantec's Complementary Bipolar process and are zener zap trimmed for low offset voltage.

Elantec's high speed amplifiers are widely used in military, video and medical applications. They are especially suited for high speed video amplifiers, pulse detectors, and wide bandwidth filters.

Elantec's EL2039/883B and EL2040/883B comply with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

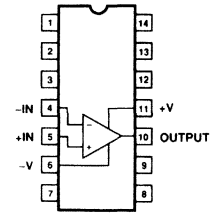
Connection Diagrams

EL2039 DIP



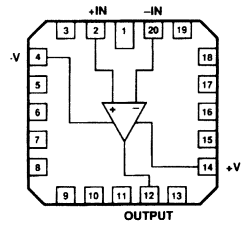
Top View

EL2040 DIP



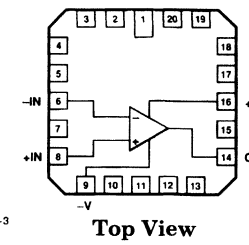
Top View

EL2039 LCC



Top View

EL2040 LCC



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EL2039/EL2040

Very High Slew Rate Wideband Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
V_{DIFF}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
P_D	Internal Power Dissipation	See Curves
T_A	Operating Temperature Range	
	EL2039, EL2040	−55°C to +125°C
	EL2039C, EL2040C	0°C to +75°C
T_J	Operating Junction Temperature	
	CerDIP, Ceramic LCC	175°C
	Plastic DIP	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
T_{LT}	Lead Temperature	
	(Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 1 kΩ, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	EL2039 EL2040 Test Level	EL2039C EL2040C Test Level	Units
V_{OS}	Input Offset Voltage	25°C		0.5	2	I	I	mV
		Full			6	I	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	V	µV/°C
I_B	Bias Current	25°C		5	15	I	I	µA
		Full			20	I	III	µA
I_{OS}	Offset Current	25°C		1	4	I	I	µA
		Full			6	I	III	µA
R_{IN}	Input Resistance	25°C		10		V	V	kΩ
C_{IN}	Input Capacitance	25°C		1		V	V	pF
V_{CM}	Common Mode Range	Full	±11	±12		I	II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		6		V	V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain	25°C	10k	15k		I	I	V/V
	(Note 1)	Full	5k			I	III	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	Full	60	90		I	II	dB
V_O	Output Voltage Swing	Full	±11	±12		I	II	V
I_O	Output Current (Note 11)	Full	±25	±50		I	II	mA
R_O	Output Resistance	25°C		30		V	V	Ω
I_S	Supply Current	Full		13	17	I	II	mA
PSRR	Power-Supply Rejection Ratio (Note 7)	Full	60	85		I	II	dB

AC Electrical Characteristics—EL2039

Parameter	Description	Temp	Min	Typ	Max	EL2039 Test Level	EL2039C Test Level	Units
GBW	Gain-Bandwidth Product (Notes 3, 4)	25°C		600		V	V	MHz
FPBW	Full-Power Bandwidth (Notes 1, 5, 8)	25°C	8.7	9.5		I	I	MHz
t_r	Rise Time (Note 6)	25°C		4		V	V	ns
OS	Overshoot (Note 6)	25°C		35		V	V	%
SR	Slew Rate (Note 6)	25°C	550	600		I	I	V/μs
ts	Settling Time (Note 6) 10V Step to 0.1%	25°C		100		V	V	ns

AC Electrical Characteristics—EL2040

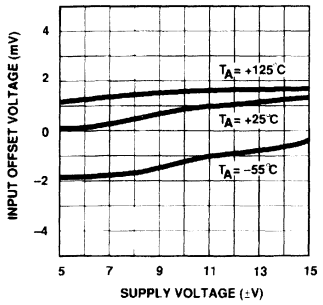
Parameter	Description	Temp	Min	Typ	Max	EL2040 Test Level	EL2040C Test Level	Units
GBW	Gain-Bandwidth Product (Notes 3, 4)	25°C		400		V	V	MHz
FPBW	Full-Power Bandwidth (Notes 1, 5, 8)	25°C	5.5	6		I	I	MHz
t_r	Rise Time (Note 6)	25°C		5		V	V	ns
OS	Overshoot (Note 6)	25°C		15		V	V	%
SR	Slew Rate (Note 6)	25°C	350	400		I	I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.1%	25°C		70		V	V	ns

Note 1: $V_O = \pm 10V$.
Note 2: Two tests are performed, $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0V$ to $-10V$.
Note 3: $V_O = 90$ mV.
Note 4: $A_V = 10$.
Note 5: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
Note 6: Refer to Test Circuits section of data sheet.
Note 7: Two tests are performed. $V+ = +15V$, and $V-$ is changed from $-5V$ to $-15V$. $V- = -15V$, and $V+$ is changed from $+5V$ to $+15V$.
Note 8: $R_L = 1$ kΩ.
Note 9: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 10: $A_V = -10$, $R_L = 1$k.
Note 11: $R_L = 200\Omega$.

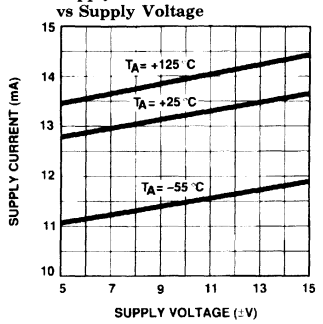
EL2039/EL2040
Very High Slew Rate Wideband Operational Amplifier

EL2039/EL2040 Typical DC Performance Curves

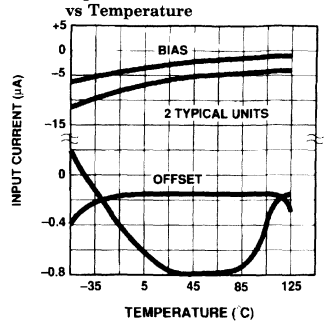
Input Offset Voltage vs Supply Voltage



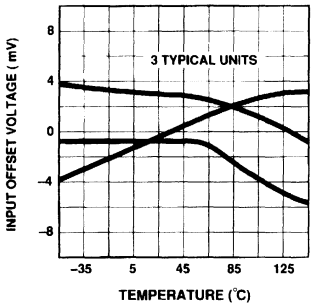
Supply Current vs Supply Voltage



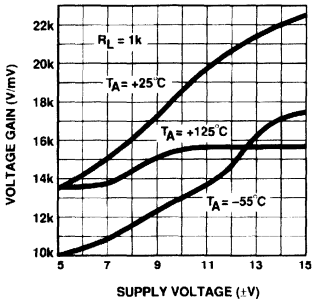
Input Currents vs Temperature



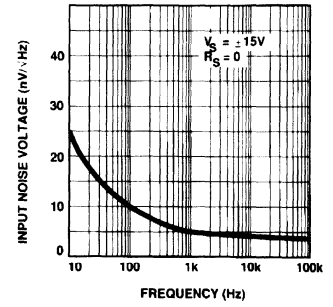
Input Offset Voltage vs Temperature



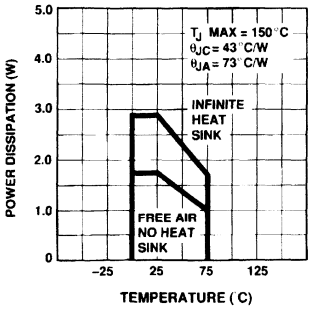
Voltage Gain vs Supply Voltage



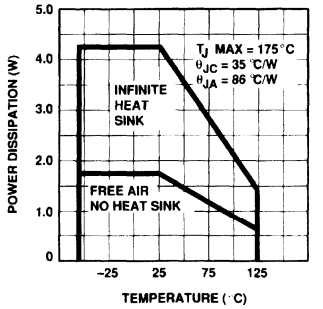
Input Noise Voltage vs Frequency



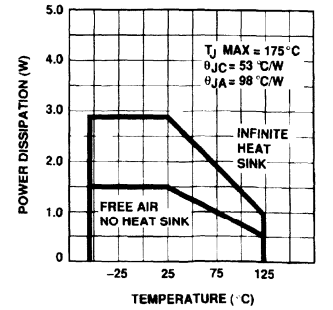
14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



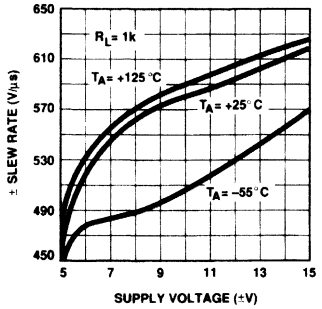
20-Lead LCC Maximum Power Dissipation vs Ambient Temperature



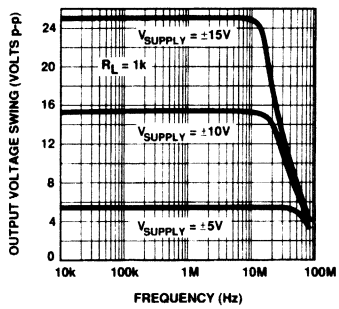
2039-5

EL2039 Typical AC Performance Curves

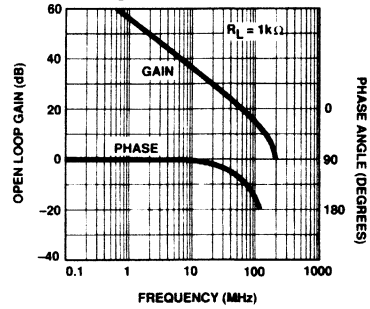
Slew Rate vs Supply Voltage



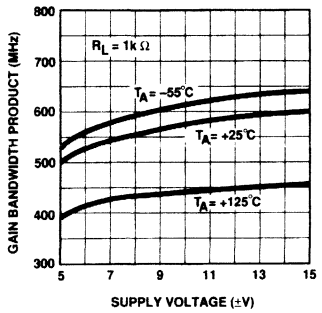
Output Voltage Swing vs Frequency



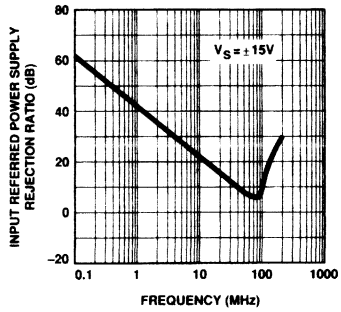
Open Loop Voltage Gain vs Frequency



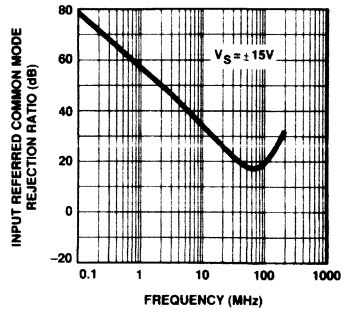
Gain Bandwidth Product at 10 MHz vs Supply Voltage



Input Referred Power Supply Rejection Ratio vs Frequency

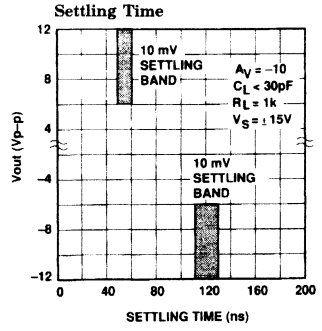


Input Referred Common Mode Rejection Ratio vs Frequency



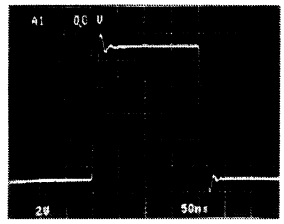
2039-6

Settling Time



2039-7

Large Signal Response



V_{IN} = ±0.5V
V_O = ±5V

2039-8

Small Signal Response

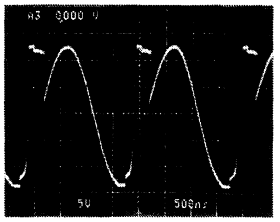
V_{IN} = ±10 mV
V_O = ±100 mV

2039-9

EL2039/EL2040
Very High Slew Rate Wideband Operational Amplifier

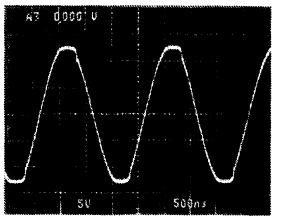
EL2039 Typical AC Performance Curves — Contd.

HA2539 at Onset of Clipping



2039-10

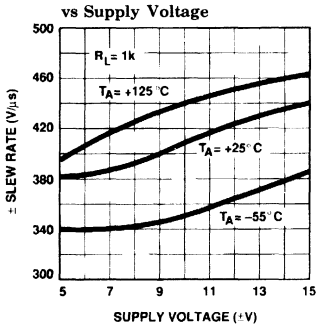
EL2039 at Onset of Clipping



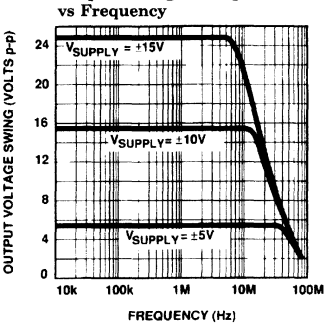
2039-11

EL2040 Typical AC Performance Curves

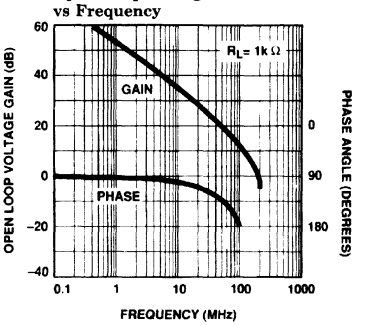
±Slew Rate vs Supply Voltage



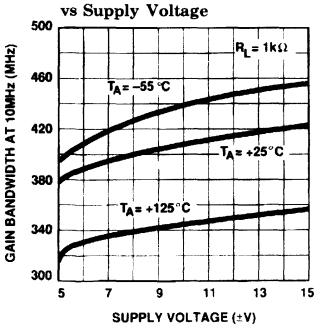
Output Voltage Swing vs Frequency



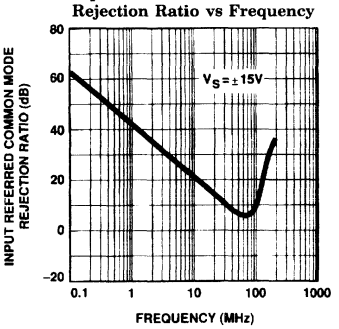
Open Loop Voltage Gain vs Frequency



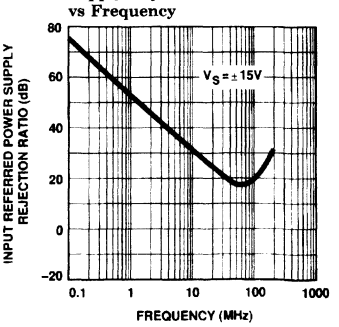
Gain Bandwidth Product at 10 MHz vs Supply Voltage



Input Referred Common Mode Rejection Ratio vs Frequency



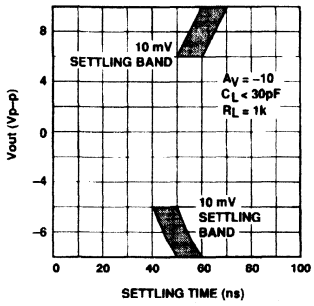
Input Referred Power Supply Rejection Ratio vs Frequency



2039-12

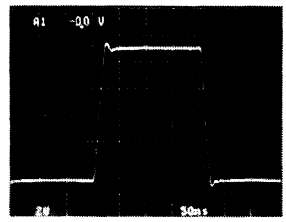
EL2040 Typical AC Performance Curves — Contd.

Settling Time



2039-13

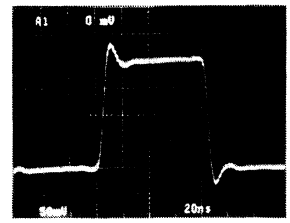
Large Signal Response



V_{IN} = ±0.5V
V_O = +5V

2039-14

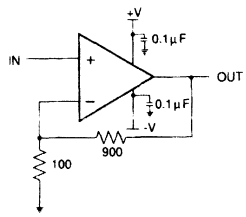
Small Signal Response



V_{IN} = ±10 mV
V_O = ±100 mV

2039-15

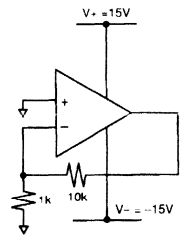
Test Circuit



2039-16

A_V = 10
C_L = 10 pF Scope Probe

Burn-In Circuit

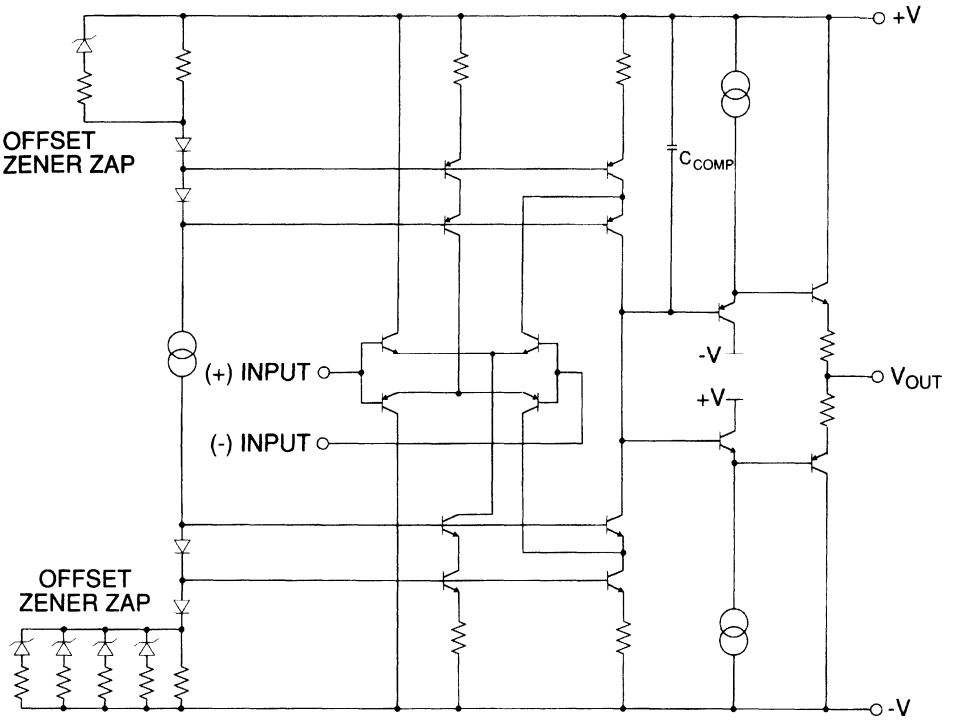


2039-17

EL2039/EL2040

Very High Slew Rate Wideband Operational Amplifier

Schematic



2039-18

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2041/EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Features

- Open loop unity bandwidth—90 MHz
- Unity gain stable
- High gain—10k typ.
- High slew rate—250 V/μs
- Low offset voltage—0.5 mV typ., 2 mV max.
- Low supply current—13 mA typ., 17 mA max.
- Wide supply operation ±5V to ±15V
- Output voltage swing—±11V
- Power bandwidth—4 MHz
- Fast settling time
- MIL-STD-883 Rev. C compliance
- Pin compatible with HA2541

Applications

- Pulse and video amplifiers
- Fast integrators
- Wideband filters
- High speed sample and hold circuits
- Fast, precise D/A converter output amplifier
- High speed A/D input amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2041CG	0°C to +75°C	12-Pin TO-8	MDP0002
EL2041CJ	0°C to +75°C	14-Pin CerDIP	MDP0014
EL2041G	−55°C to +125°C	12-Pin TO-8	MDP0002
EL2041G/883B	−55°C to +125°C	12-Pin TO-8	MDP0002
EL2041J	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2041J/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2041CN	0°C to +75°C	8-Pin P-DIP	MDP0006

General Description

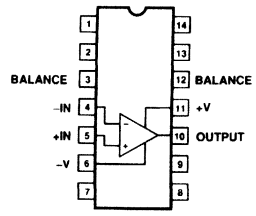
The EL2041 is a unity gain stable monolithic operational amplifier with a 90 MHz open loop unity bandwidth. This unprecedented bandwidth is accomplished with a 45° phase margin and a 6.5 dB gain margin. Unlike other wideband amplifiers, the patented EL2041 operates on standard ±15V supplies, swings ±11V at its output, and maintains an 80 dB open loop gain into a 1k load.

In addition, the EL2041 has a 250 V/μs slew rate while drawing only 13 mA of supply current. Zener Zap techniques are used to trim the offset voltage to 2 mV maximum, making the EL2041 an excellent choice for applications requiring both speed and accuracy.

Elantec's EL2041/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

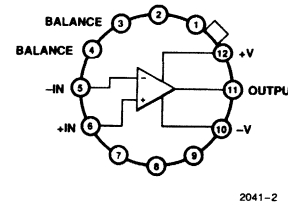
CerDIP Package



2041-1

Top View

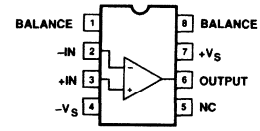
12-Lead TO-8



2041-2

Top View

Plastic DIP



2041-3

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EL2041/EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−		35V
Differential Input Voltage		6V
Output Current	Continuous	25 mA
	Peak	50 mA
Internal Power Dissipation	See Curves	
Operating Temperature Range		
EL2041		−55°C to +125°C
EL2041C		0°C to +75°C

Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	
CerDIP, TO-8	175°C
Plastic DIP	150°C
Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 1 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2041				EL2041C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	+25°C		0.5	2	I		0.5	5	I	mV
		Full			10	I			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V		20		V	µV/°C
I_B	Bias Current	+25°C		5	15	I		5	15	I	µA
		Full			20	I			20	III	µA
I_{OS}	Offset Current	+25°C		1	4	I		1	4	I	µA
		Full			6	I			6	III	µA
R_{IN}	Input Resistance	+25°C		20		V		20		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±8	±11		I	±8	±11		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω	+25°C		10		V		10		V	$nV\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain (Notes 1, 2)	+25°C	7k	10k		I	5k	10k		I	V/V
		Full	5k			I	4k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	70	80		I	60	80		II	dB
V_O	Output Voltage Swing	Full	±11	±12		I	±11	±12		II	V
I_O	Output Current (Note 11)	Full	±25	±50		I	±25	±50		I	mA
R_O	Output Resistance	+25°C		40		V		40		V	Ω
I_S	Supply Current	Full		13	17	I		13	17	II	mA
PSRR	Power Supply Rejection Ratio (Note 7)	Full	60	80		I	60	80		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 1\ k\Omega$, unless otherwise specified

Symbol	Parameter	Temp	EL2041				EL2041C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Notes 4, 10)	+25°C		90		V		90		V	MHz
FPBW	Full Power Bandwidth (Notes 1, 5)	+25°C	2.8	4		I	2.8	4		I	MHz
t_r	Rise Time (Note 6)	+25°C		4		V		4		V	ns
OS	Overshoot (Note 6)	+25°C		10		V		10		V	%
SR	Slew Rate (Note 6)	+25°C	180	250		I	180	250		I	V/μs
t_s	Settling Time (Notes 8, 9, 10) 10V Step to 0.05%	+25°C		90		V		90		V	ns

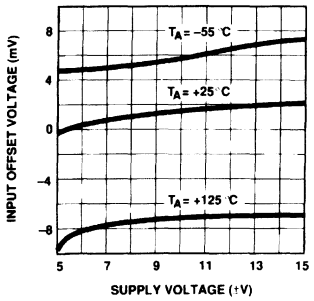
Note 1: $V_O = \pm 10V$.
Note 2: $R_L = 1\ k\Omega$.
Note 3: Two tests are performed. $V_{CM} = 0V$ to $+8V$ and $V_{CM} = 0V$ to $-8V$.
Note 4: $V_O = 90\ mV$.
Note 5: Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi\ V\text{peak}}$.
Note 6: Refer to Test Circuits section of data sheet.
Note 7: Two tests are performed. V+ = +15V, and V− is changed from −7V to −15V. V− = −15V, and V+ changed from +7 to +15V.
Note 8: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 9: $A_V = +1$, $R_L = 1k$.
Note 10: 200Ω, 20 pF output snubber, see application section.
Note 11: $R_L = 200\Omega$.

EL2041/EL2041C

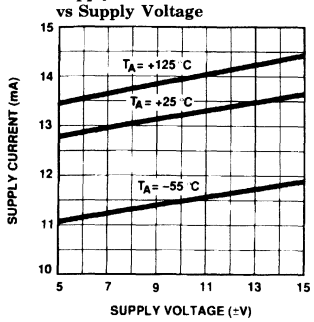
Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Typical Performance Curves

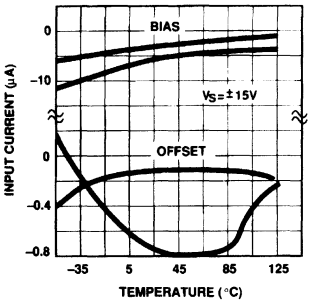
Input Offset Voltage vs Supply Voltage



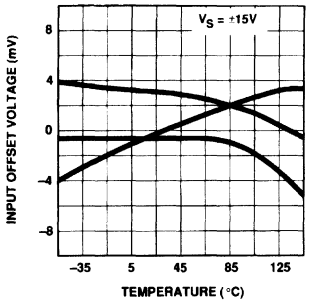
Supply Current vs Supply Voltage



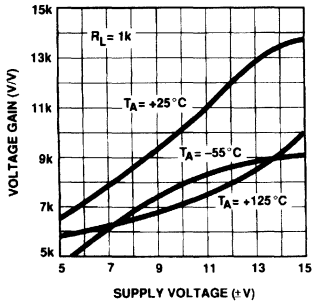
Input Current vs Temperature (2 Typical units)



Input Offset Voltage vs Temperature (3 Typical units)



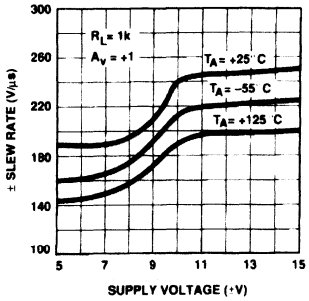
Voltage Gain vs Supply Voltage



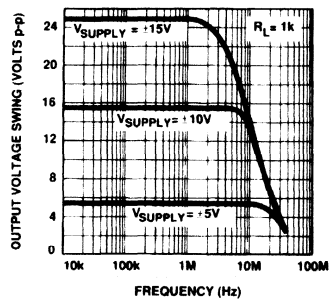
2041-4

Typical Performance Curves — Contd.

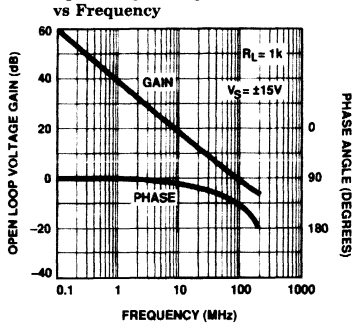
Slew Rate
vs Supply Voltage



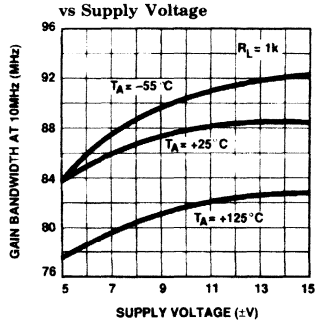
Output Voltage Swing
vs Frequency



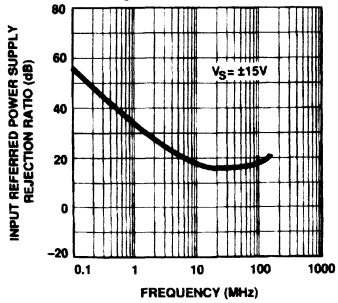
Open Loop Voltage Gain
vs Frequency



Gain Bandwidth Product
at 10 MHz
vs Supply Voltage



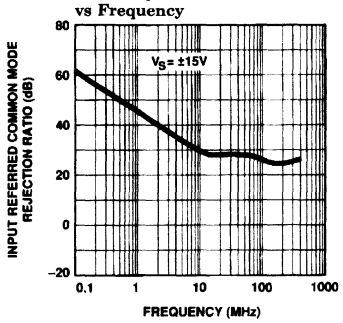
Input Referred Power
Supply Rejection Ratio
vs Frequency



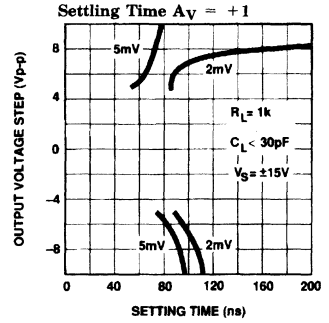
2041-5

Typical Performance Curves — Contd.

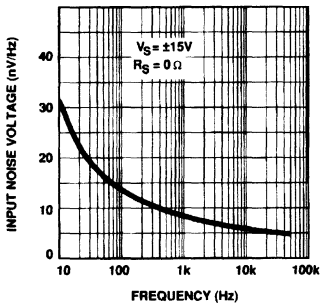
Input Referred Common Mode Rejection Ratio vs Frequency



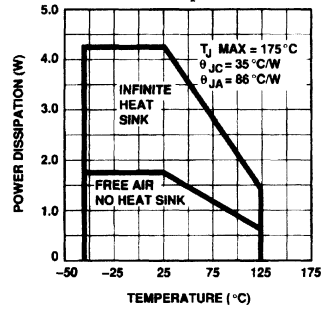
Settling Time A_V = +1



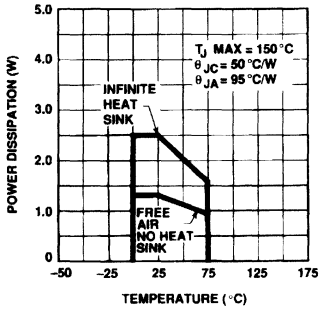
Input Noise Voltage vs Frequency



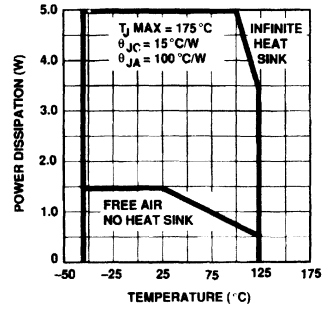
14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



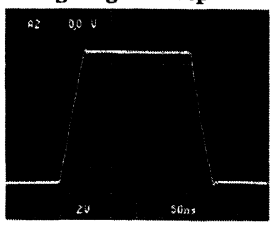
12-Lead TO-8 Maximum Power Dissipation vs Ambient Temperature



2041-6

Typical Performance Curves — Contd.

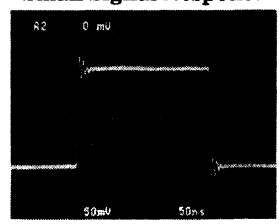
Large Signal Response



2041-7

$A_V = +1$
$V_{IN} = \pm 5V$
$V_O = \pm 5V$

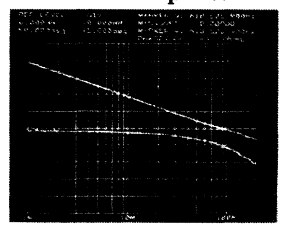
Small Signal Response



2041-8

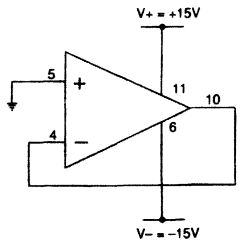
$A_V = +1$
$V_{IN} = \pm 100$ mV
$V_O = \pm 100$ mV

Open Loop Gain and Phase Response



2041-9

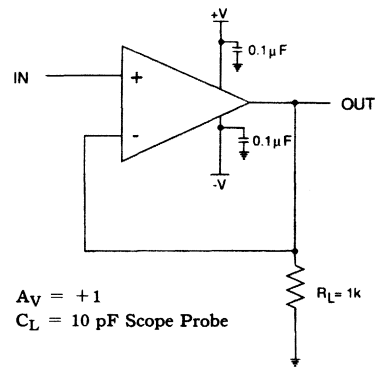
Burn-In Circuit



2041-10

Pin numbers are for 14-Lead cerDIP. Burn-in circuit is identical for all package types.

Test Circuit



$A_V = +1$
$C_L = 10$ pF Scope Probe

2041-11

EL2041/EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Application Hints

Product Description

The EL2041 is a wideband monolithic operational amplifier built on Elantec's proprietary Complementary Bipolar process. Unlike many ±5V wideband op amps available today, the EL2041 operates from ±5V to ±15V and is capable of driving ±11V at its output. The large signal swing and open loop voltage gain of 80 dB with a 1 kΩ load, differentiate the EL2041 from other op amps that do not have sufficient load isolation. Another unusual characteristic of the amplifier is the extremely wide unity gain bandwidth of 90 MHz. This bandwidth is accomplished with a 45° phase margin, a 6.5 dB gain margin, and a slew rate of 250 V/μs. These AC characteristics are realized with a 13 mA supply current, which means lower power dissipation and higher reliability than competing products.

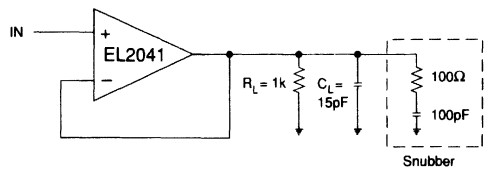
Power Supply Bypass

It is important to bypass the power supplies of the EL2041 with 0.1 μF or 0.01 μF ceramic disc capacitors. Failure to do this will result in oscillation or signal distortion. Although the lead length is not critical, it should not be more than ½" from the IC pins.

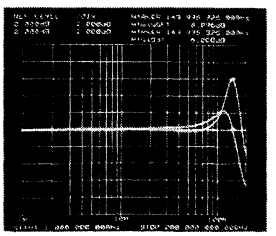
Capacitive Loading

Like all high speed op amps, the EL2041 is sensitive to capacitive loading. There are at least two ways to approach this problem: The use of a snubber (Q spoiler), or the use of feedback isolation.

The first approach is to consider the output stage of the amplifier as a highly inductive element due to the application of feedback. When this output stage is loaded with a capacitance a natural resonance occurs. By putting a series RC at the output of the amplifier, the energy of the tank can be absorbed, quenching the instability. The way to select the RC values for the Q spoiler is to drive a small signal (few 100 mV) squarewave into the desired capacitive load. Place a small resistor (few 100Ω) at the output to ground, and note the reduction in ringing. When the desired response has been obtained, the capacitance value can be chosen. Start with a few 10's of pico farads in series with the selected resistor. Adjust the capacitor for the desired response. The capacitor value cannot be chosen arbitrarily large because of the reduction in open loop gain the series resistor will cause. In the example shown, the effects of a 15 pF load have been eliminated. Larger values of load capacitance can be tamed with a different RC value.

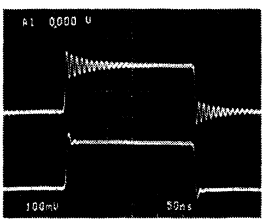


2041-12



2041-13

Frequency Response +6 dB Peak without Snubber and +2 dB with 200Ω, 20 pF Snubber.



2041-14

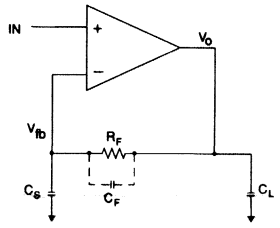
Top Trace is without Snubber; Bottom Trace is 100Ω, 100 pF Snubber.

Another way to look at the effect of capacitive loading is in the frequency domain. The open loop output impedance of the EL2041 is about 40Ω; when the output is loaded with 15 pF, an output pole is formed at 265 MHz. This pole sounds innocent enough until it's realized that it causes a phase shift of $\tan^{-1}$ ωRC, and at 100 MHz that is 21°. If the amplifier has a 45°

Application Hints — Contd.

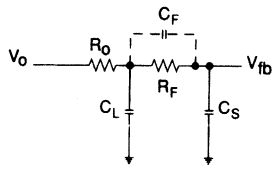
phase margin with no capacitive loading, then with 15 pF it will reduce to 24° and considerable ringing will occur. Some help can be obtained by isolating the output from the capacitance on the inverting input.

Voltage Follower with Feedback Isolation



2041-15

Equivalent Circuit for Signal, Fed Back



2041-16

The signal fed back is:

$$\frac{V_{FB}}{V_O} = \frac{1}{(1+SC_LR_O)(1+SR_FC_S)}$$

The situation now appears to have been made worse with an output pole and a feedback pole, but with the addition of a capacitor C_F, the effects of the stray capacitance at the inverting input can be swamped.

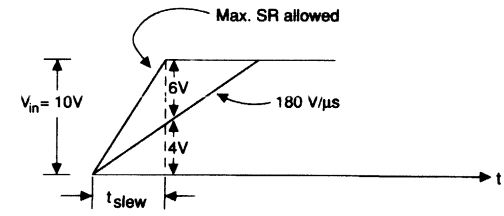
$$\frac{V_{FB}}{V_O} = \frac{1+SC_FR_F}{(1+SC_LR_O)(1+SR_F\,[C_F+C_S])}$$

The trick here is to pick C_F large enough to overwhelm C_S and cancel the feedback pole. However C_F cannot be made too large or it will look like an AC short and C_S will again appear in parallel with C_L. Some typical values to begin design work are: $R_F = 200$, $C_F = 15$ pF, for C_L = 15 pF, and C_S depends on board layout (try to minimize). It should also be realized that these values of R_F and C_F will begin to roll-off the close loop gain at 40 MHz.

Input Overdrive

It is important not to overdrive the input of the EL2041. Input slew rates in excess of 180 V/μs can cause distortion in the large signal square wave response, and this will show up as an increase in settling time (see typical performance curves). There are several solutions to this: Slew rate limit the input source, put clamp diodes across the amplifier inputs, or take some voltage gain in the amplifier.

Slew rate limit the input: For example with a 10 V_{p-p} step at the input, the input rate should be limited to:



2041-17

$$t_{SLEW} = \frac{V_{IN} - V_{ZENER}}{\min SR},$$

$$\text{Max source SR} = \frac{V_{IN}}{t_{SLEW}}$$

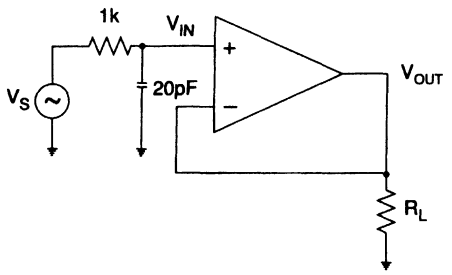
or

$$\frac{10-6}{180\ V/\mu s} = 22\ ns\ ,\quad \text{Max SR} = \frac{10}{22\ ns} = 450\ V/\mu s$$

If the input slew rate is limited by a 1k resistor, how large a capacitor is needed?

$$\frac{10V}{1k} = 10\ mA = C\frac{dv}{dt}\ ,\quad C = \frac{10\ mA}{450\ V/\mu s} = 22\ pF$$

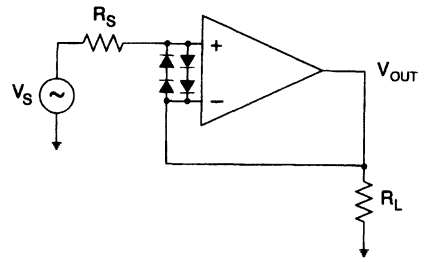
Application Hints — Contd.



2041-18

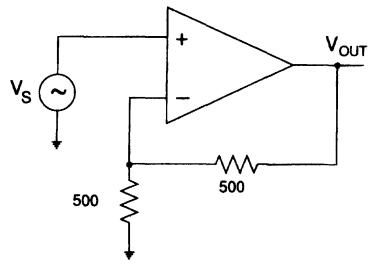
This value of R and C will give a −3 dB bandwidth of 8 MHz through the op amp. This technique should be avoided if the intended use is a small signal sinewave application.

Clamp diodes across the inputs: To obtain full slew rate at elevated temperature requires a V_{BE} of overdrive across the inputs. To insure adequate protection and slew rate requires two diodes in each direction across the inputs. A small series resistance in the input will limit the current through the diodes.



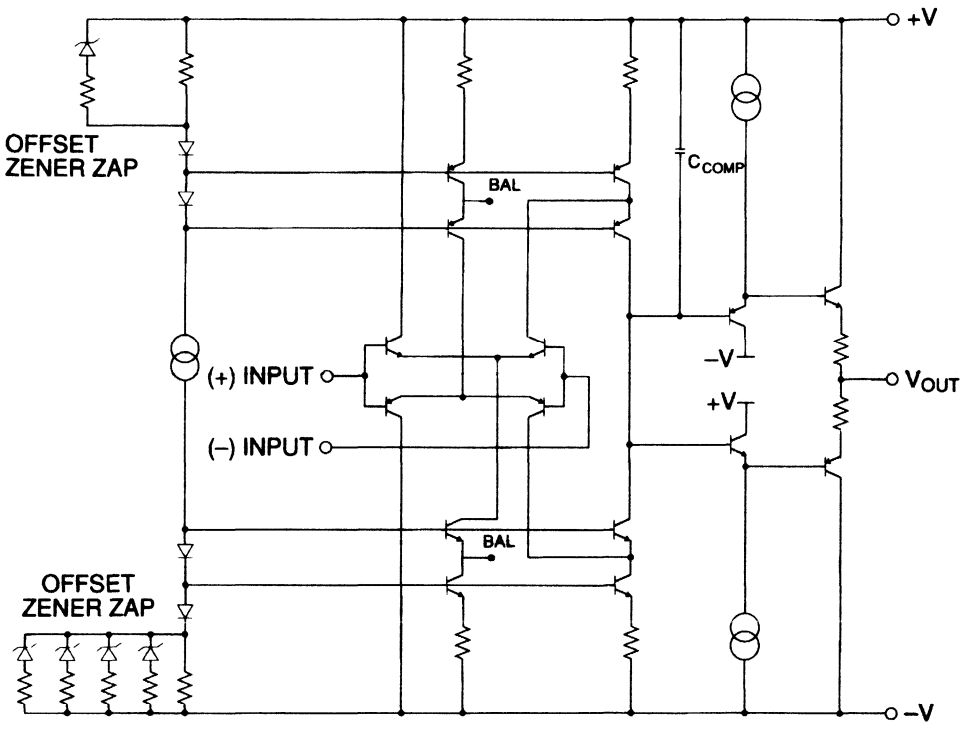
2041-19

Take voltage gain in the op amp: By taking voltage gain, the input stage does not have to handle as large a signal swing for a given output swing. For a voltage gain of 2, remember that the closed loop bandwidth will go to 45 MHz.



2041-20

Simplified Schematic



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2190/EL2195

Wideband, Fast Settling Operational Amplifier

Features

- Low offset voltage—0.5 mV typ., 2 mV max
- Low supply current—13 mA typ., 17 mA max
- Very high Slew Rate—200 V/μs
- Wide gain-bandwidth—150 MHz
- Power bandwidth—6.5 MHz
- Fast settling—70 ns
- Input voltage noise—6 nV/$\sqrt{Hz}$
- MIL-STD-883 Rev. C compliant
- Improved replacement for HA5190/5195

Applications

- Fast, precise D/A converters
- High speed sample-hold circuits
- Pulse and video amplifiers
- Wideband amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2190G	−55°C to +125°C	12-Pin TO-8	MDP0002
EL2190G/883B	−55°C to +125°C	12-Pin TO-8	MDP0002
EL2190J	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2190J/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2190L/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EL2195CJ	0°C to +75°C	12-Pin CerDIP	MDP0014
EL2195CG	0°C to +75°C	12-Pin TO-8	MDP0002

General Description

The EL2190/EL2195 are an improved design over the HA5190/HA5195 monolithic operational amplifiers. The EL2190/EL2195 feature a zener zapped trim design for tighter offset voltage, and a supply current 40% less than the previous generation devices. Employing patented circuit techniques and monolithic Complementary Bipolar construction, these devices are capable of delivering a 200 V/μs slew rate and 70 ns settling times with only 13 mA supply current. These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding EL2190/EL2195 features are 150 MHz gain-bandwidth product and 6.5 MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 2 mV max offset voltage and 6.0 nV/$\sqrt{Hz}$ input voltage noise (at 1 kHz).

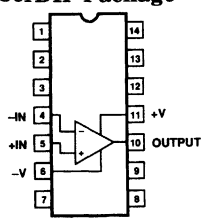
These devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample and hold circuits. 150 MHz gain-bandwidth-product, 6.5 MHz power bandwidth, and 2 mV maximum offset voltage all make the EL2190/EL2195 well suited for a variety of pulse and wideband video amplifier applications.

The EL2190 is specified over the −55°C to +125°C range while the EL2195 is specified from 0°C to +75°C.

Elantec's EL2190/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing Monolithic Products.*

Connection Diagrams

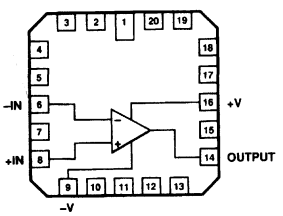
CerDIP Package



2190-1

Top View

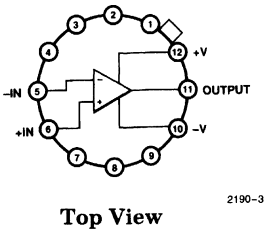
20-Lead LCC



2190-2

Top View

12-Lead TO-8



2190-3

Top View

Note: Case tied to pin 10.

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EL2190/EL2195
Wideband, Fast Settling Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Operating Temperature Range	
Differential Input Voltage	6V	EL2190	−55°C to +125°C
Output Current	50 mA (Peak)	EL2195	0°C to +75°C
	30 mA (Continuous)	Operating Junction Temperature	
Internal Power Dissipation	See Curves	CerDIP, Ceramic LCC, TO-8	175°C
		Lead Temperature (Soldering, 5 seconds)	300°C
		Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 200Ω; unless otherwise specified

Parameter	Description	Temp	EL2190				EL2195				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	+25°C		0.5	2	I		0.5	2	I	mV
		Full			6	I			6	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V		20		V	µV/°C
I_B	Bias Current	+25°C		5	15	I		5	15	I	µA
		Full			20	I			20	III	µA
I_{OS}	Offset Current	+25°C		1	4	I		1	4	I	µA
		Full			6	I			6	III	µA
R_{IN}	Input Resistance	+25°C		10		V		10		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±6	±10		I	±6	±10		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		6		V		6		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 1, 2)	+25°C	15k	30k		I	10k	30k		I	V/V
		Full	5k			I	5k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	74	90		I	74	90		II	dB

EL2190/EL2195
Wideband, Fast Settling Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 200\Omega$; unless otherwise specified — Contd.

Parameter	Description	Temp	EL2190				EL2195				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing (Notes 1, 11)	Full	±5	±8		I	±5	±8		II	V
		Full	±11	±12		I	±11	±12		II	V
I_O	Output Current	Full	±25	±50		I	±25	±50		II	mA
R_O	Output Resistance	+25°C		30		V		30		V	Ω
I_S	Supply Current	Full		13	17	I		13	17	II	mA
PSRR	Power Supply Rejection Ratio (Note 8)	Full	70	80		I	70	80		II	dB

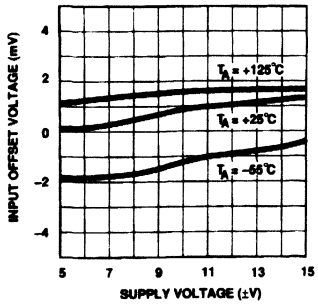
AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 200\ \Omega$; unless otherwise specified

Parameter	Description	Test Conditions	EL2190				EL2195				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
GBW	Gain-Bandwidth Product (Notes 4, 5)	+25°C		150		V		150		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 6)	+25°C	5	6.5		I	5	6.5		I	MHz
t_r	Rise Time (Note 7)	+25°C		7	18	IV		7	18	IV	ns
OS	Overshoot (Note 7)	+25°C		25		V		25		V	%
SR	Slew Rate (Note 7)	+25°C	160	200		I	160	200		I	V/μs
t_s	Settling Time (Notes 9, 10)										
	5V Step to 0.1%	+25°C		50		V		50		V	ns
	5V Step to 0.05%	+25°C		70		V		70		V	ns

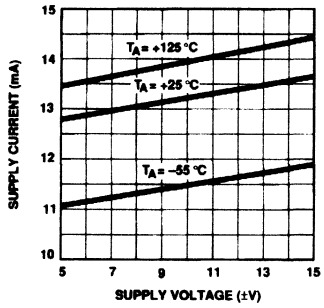
Note 1: $R_L = 200\Omega$, $C_L < 10$ pF.
Note 2: $V_O = \pm 5V$.
Note 3: Two tests are performed. $V_{CM} = 0V$ to $+5V$ and $V_{CM} = 0V$ to $-5V$.
Note 4: $V_O = 90$ mV.
Note 5: $A_V = 10$.
Note 6: Full Power Bandwidth guaranteed based on slew rate measurement using : $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
Note 7: Refer to Test Circuits section of data sheet.
Note 8: Two tests are performed. V+ = +15V, and V− is changed from 10V to 20V. V− = −15V, and V+ is changed from +10V to +20V.
Note 9: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 10: $R_L = 1k$, $A_V = -5$.
Note 11: $R_L = 1k$.

Typical Performance Curves

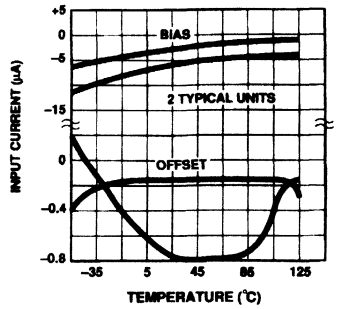
Input Offset Voltage vs Supply Voltage



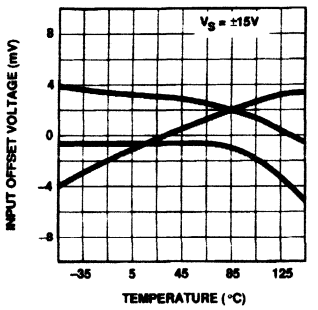
Supply Current vs Supply Voltage



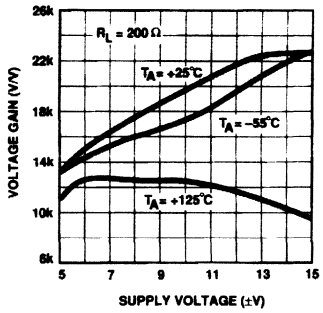
Input Currents vs Temperature



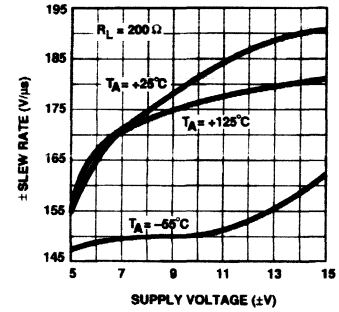
Input Offset Voltage vs Temperature (3 Typical Units)



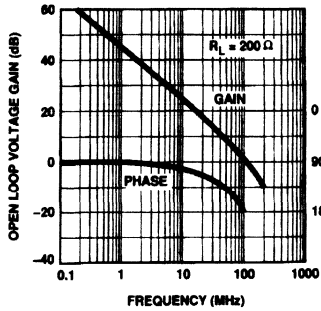
Voltage Gain vs Supply Voltage



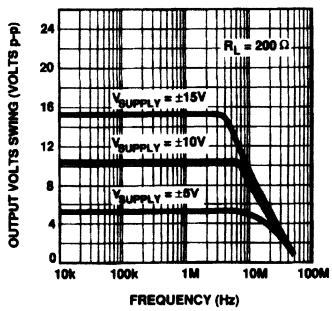
±Slew Rate vs Supply Voltage



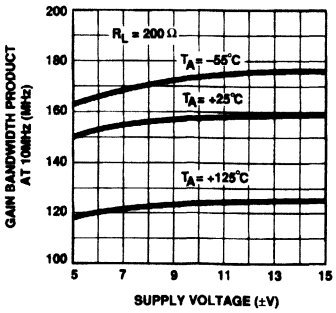
Open Loop Voltage Gain vs Frequency



Output Voltage Swing vs Frequency



Gain Bandwidth Product at 10 MHz vs Supply Voltage

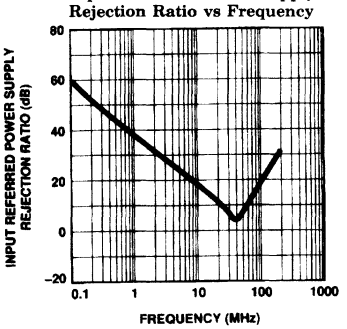


2190-4

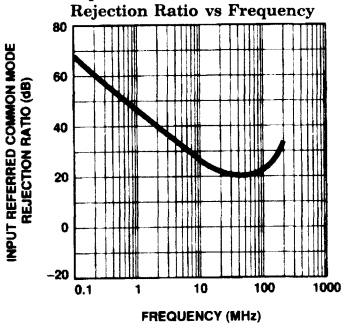
EL2190/EL2195
Wideband, Fast Settling Operational Amplifier

Typical Performance Curves — Contd.

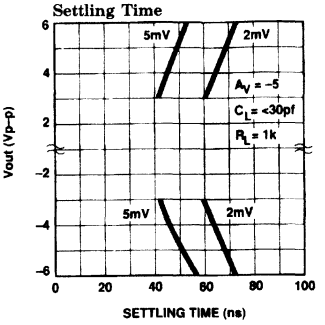
Input Referred Power Supply Rejection Ratio vs Frequency



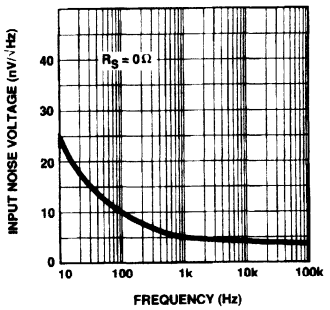
Input Referred Common Mode Rejection Ratio vs Frequency



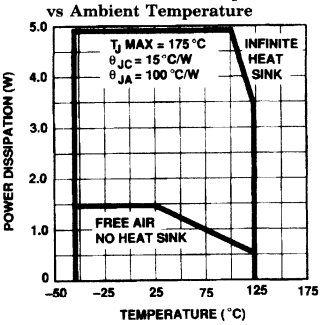
Settling Time



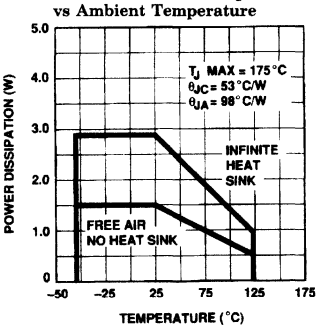
Input Noise Voltage vs Frequency



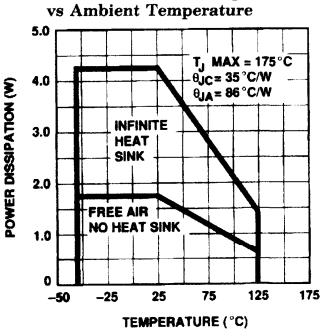
12-Lead TO-8 Maximum Power Dissipation vs Ambient Temperature



20-Lead LCC Maximum Power Dissipation vs Ambient Temperature



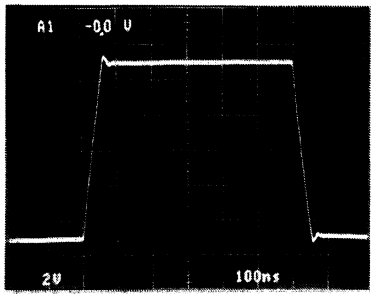
14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



2190-5

Typical Performance Curves — Contd.

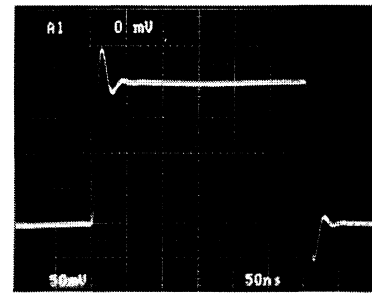
Large Signal Response



V_{IN} = ±1V
V_O = ±5V

2190-6

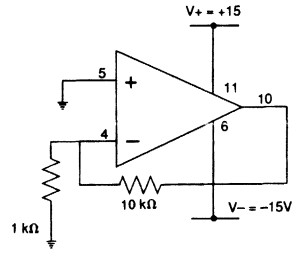
Small Signal Response



V_{IN} = ±20 mV
V_O = ±100 mV

2190-7

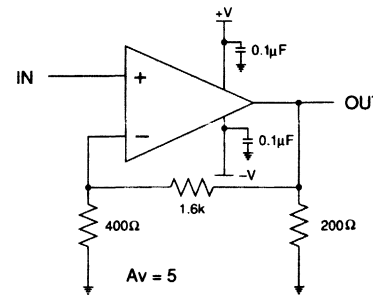
Burn-In Circuit



2190-8

Pin numbers are for 14-lead cerDIP. Burn-in circuit is identical for all package types.

Test Circuit

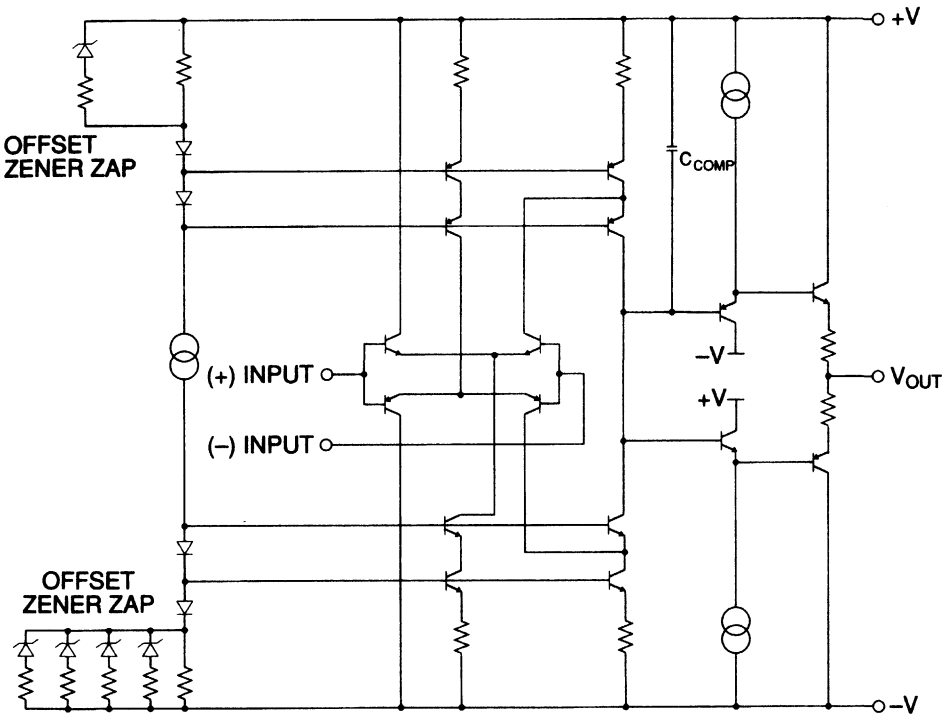


2190-9

EL2190/EL2195

Wideband, Fast Settling Operational Amplifier

Schematic



2190-10

EL2223/EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

élantec HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Features

- Wide gain bandwidth—500 MHz
- High slew rate—350 V/μs
- High power bandwidth (± 10 V_{out}) 5.5 MHz
- Large open loop gain 83 dB
- Low power—5 mA/amplifier
- Low input offset—0.5 mV typ.
- Wide supply voltage range $V_s = \pm 5V$ to $\pm 15V$
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers
- Replace two HA2540s

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2223CJ	0°C to +75°C	CerDIP	MDP0010
EL2223CN	0°C to +75°C	P-DIP	MDP0006
EL2223J	−55°C to +125°C	CerDIP	MDP0010
EL2223J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2223L/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EL2223CM	0°C to +75°C	SOL	MDP0027

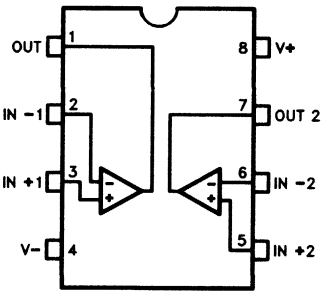
General Description

The EL2223 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This patented amplifier features 350 V/μs slew rate, a 500 MHz gain bandwidth gain-of-10 stable, along with an excellent speed power relationship. The dual 500 MHz EL2223 consumes only 10 mA, making it ideal for HA2540 type applications. The EL2223 has short-circuit-protected outputs and will operate from $\pm 5V$ to $\pm 15V$. It is fabricated using Elantec's complementary bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: *"Elantec's Military Processing, Monolithic Integrated Circuits"*.

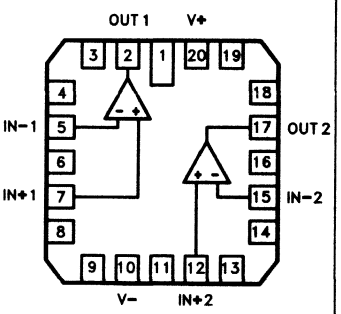
Connection Diagrams

EL2223J/CN



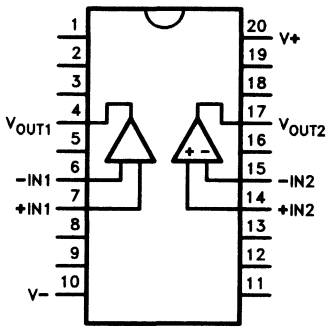
2223-1

EL2223L



2223-2

EL2223CM



2223-3

This product covered under U.S. Patent No. 4,837,523

EL2223/EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Maximum Junction Temperature	
Internal Power Dissipation	See Curves	CerDIP, LCC	175°C
Peak Output Current	Short Circuit Protected	Plastic DIP, SOL	150°C
Output Short Circuit Duration (Note 1)	Continuous	Lead Temperature	
Operational Temperature Range		DIP Package	300°C
EL2223	−55°C to +125°C	SOL Package	
EL2223C	0°C to +75°C	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	+25°C Full		0.5	5 8	I I		0.5	5 8	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift	Full		3		V		3		V	µV/°C
I_B	Bias Current	+25°C Full		1.5	4 6	I I		1.5	4 6	I III	µA µA
I_{OS}	Offset Current	+25°C Full		0.2	2 3	I I		0.2	2 3	I III	µA µA
R_{IN}	Input Resistance	+25°C		6		V		6		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±12		I	±10	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		7		V		7		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	+25°C Full	20k 10k	40k		I I	20k 10k	40k		I III	V/V V/V

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	90		I	70	90		II	dB
V_O	Output Voltage Swing	Full	±11	±12.5		I	±11	±12.5		II	V
I_O	Short Circuit Current	+25°C		±50	±70	I		±50	±70	I	mA
R_O	Output Resistance	+25°C		40		V		40		V	Ω
I_s	Supply Current	Full		9.5	13	I		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	70	90		I	70	90		II	dB

AC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

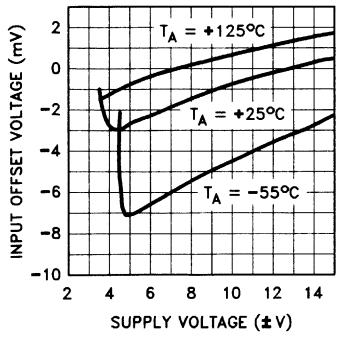
Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	+25°C		500		V		500		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	+25°C	3.98	5.5		I	3.98	5.5		I	MHz
t_r	Rise Time (Note 8)	+25°C		7		V		7		V	ns
OS	Overshoot (Note 8)	+25°C		30		V		30		V	%
SR	Slew Rate (Note 8)	+25°C	250	350		I	250	350		I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%	+25°C		330		V		330		V	ns
Ch S_p	Channel Separation (f = 10 MHz)			70		V		70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_O = ±10V.
Note 3: RL = 2 kΩ.
Note 4: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: V_O = 100 mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/ 2 π V_{peak}.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.
Note 10: A_V = +10, R_L = 2 kΩ.

EL2223/EL2223C
Dual, 500 MHz High Speed, Operational Amplifier

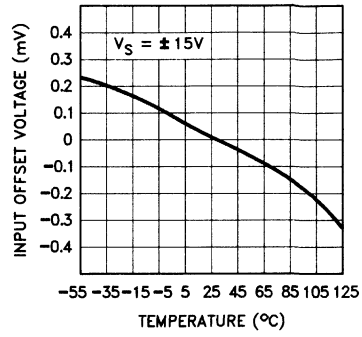
Typical Performance Curves

Input Offset Voltage vs Supply Voltage



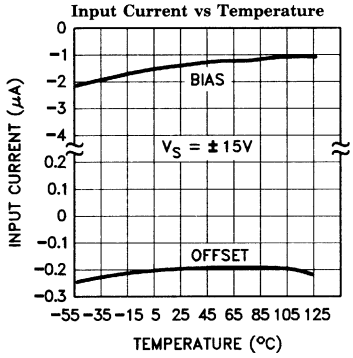
2223-4

Normalized Input Offset Voltage vs Temperature



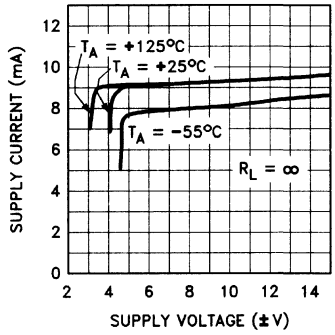
2223-5

Input Current vs Temperature



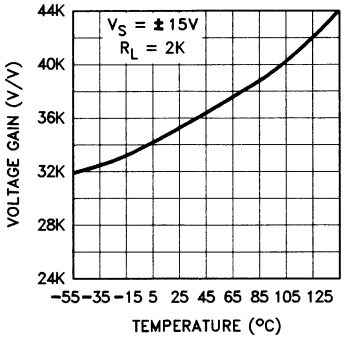
2223-6

Supply Current vs Supply Voltage



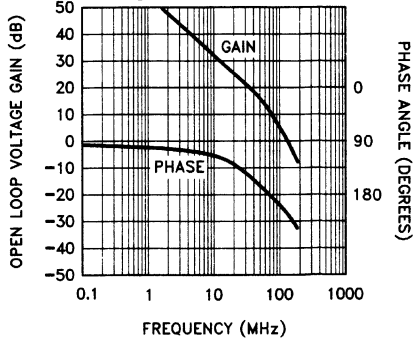
2223-7

Voltage Gain vs Temperature



2223-8

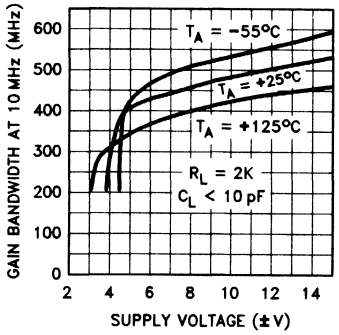
Open Loop Voltage Gain vs Frequency



2223-9

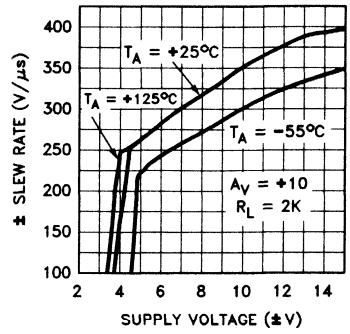
Typical Performance Curves — Contd.

Gain Bandwidth at 10 MHz vs Supply Voltage



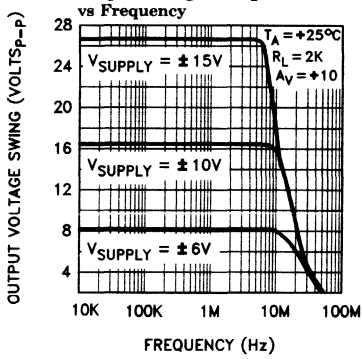
2223-10

Slew Rate vs Supply Voltage



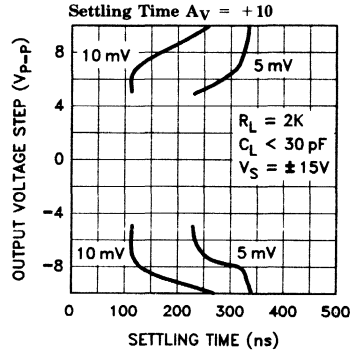
2223-11

Output Voltage Swing vs Frequency



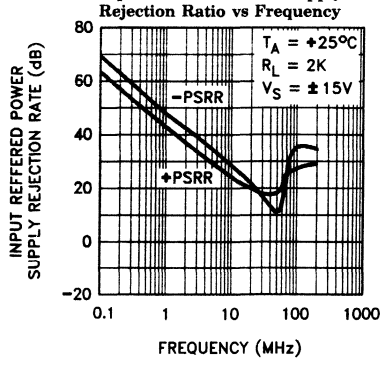
2223-12

Settling Time A_V = +10



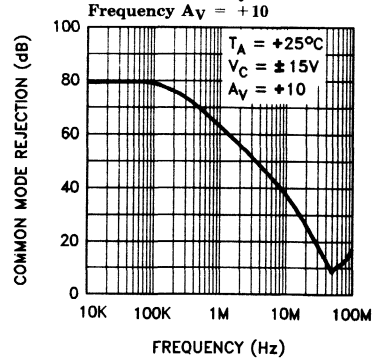
2223-13

Input Referred Power Supply Rejection Ratio vs Frequency



2223-14

Common Mode Rejection vs Frequency A_V = +10



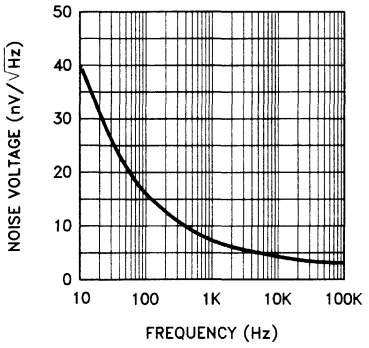
2223-15

EL2223/EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

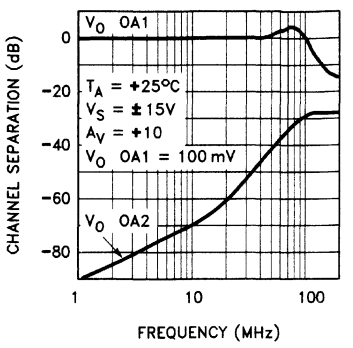
Typical Performance Curves — Contd.

Noise Voltage vs Frequency



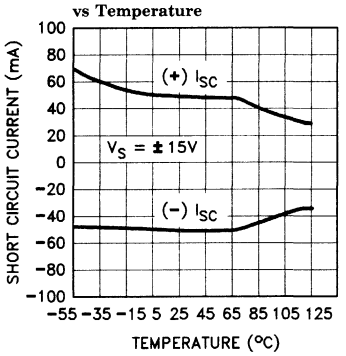
2223-16

Channel Separation vs Frequency



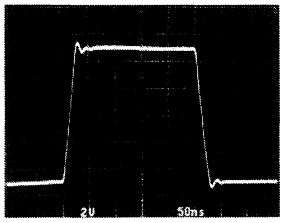
2223-17

Short Circuit Current vs Temperature



2223-18

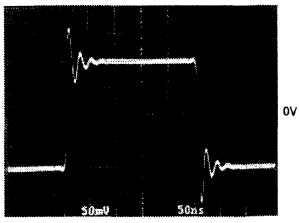
Large Signal Response



A_V = +10
V_{IN} = ±0.5V
V_O = ±5V
R_L = 2k

2223-19

Small Signal Response

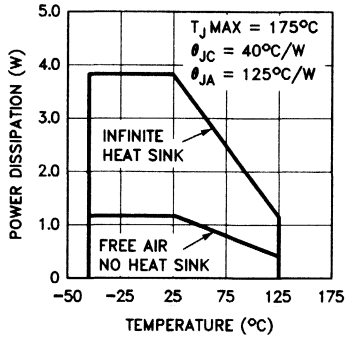


A_V = +10
V_{IN} = ±10 mV
V_O = ±100 mV
R_L = 2k

2223-20

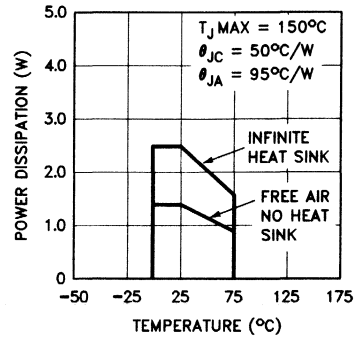
Typical Performance Curves — Contd.

8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



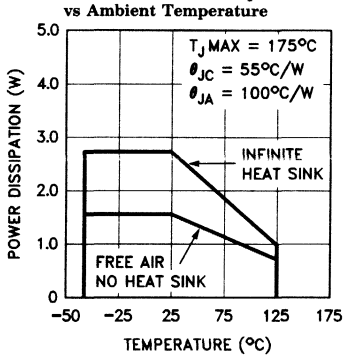
2223-21

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



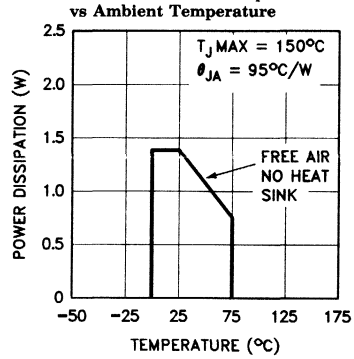
2223-22

20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



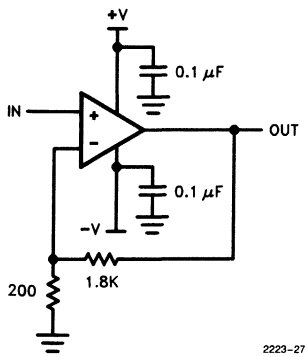
2223-23

20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2223-24

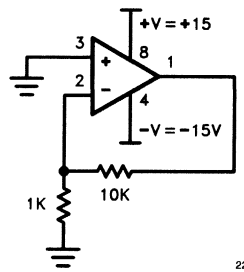
Test Circuit



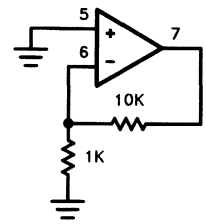
2223-27

$A_V = +10$
$C_L \leq 10$ pF Scope Probe

Burn-In Circuit



2223-28

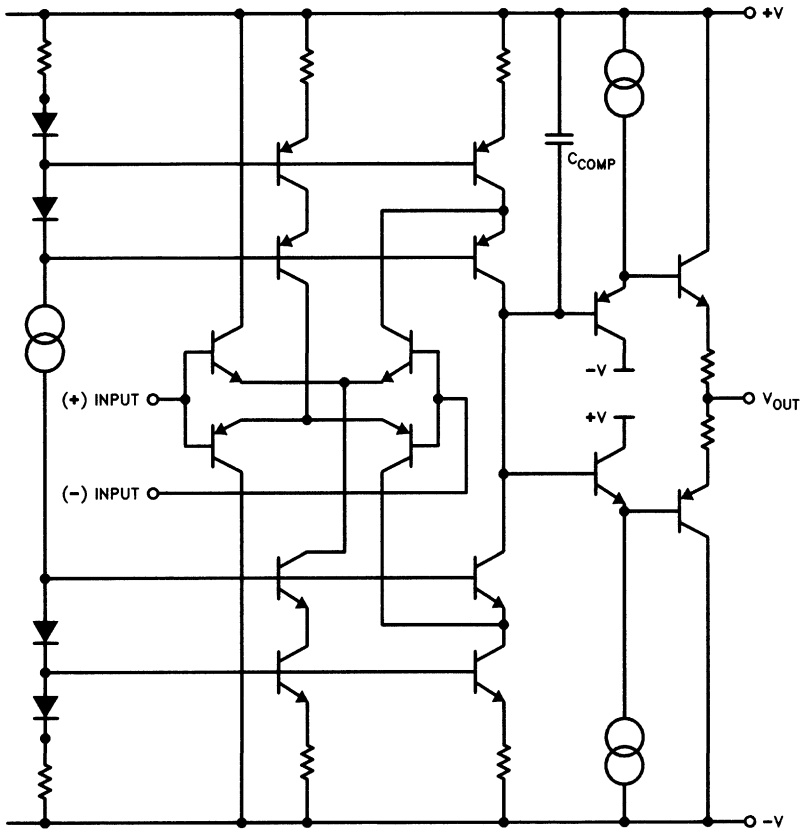


2223-29

Pin numbers are for the 8-Lead CerDIP.
Burn-in circuit is identical for all package types.

EL2223/EL2223C
Dual, 500 MHz High Speed, Operational Amplifier

Simplified Schematic (one amplifier)



EL2224/EL2224C

Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

Features

- Unity gain stable
- Wide bandwidth—60 MHz
- High slew rate—200 V/μs
- High power bandwidth (± 10 V_{out}) 3 MHz
- Large open loop gain 75 dB
- Low power—5 mA/amplifier
- Low input offset—1 mV typ.
- Wide supply voltage range $V_s = \pm 5V$ to $\pm 15V$
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2224CJ	0°C to +75°C	CerDIP	MDP0010
EL2224CN	0°C to +75°C	P-DIP	MDP0006
EL2224J	−55°C to +125°C	CerDIP	MDP0010
EL2224J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2224L/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EL2224CM	0°C to +75°C	SOL	MDP0027

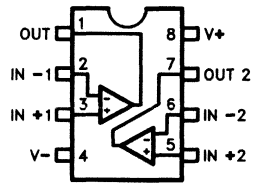
General Description

The EL2224 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This amplifier features unity gain stability, high slew rate and wide bandwidth, along with an excellent speed power relationship. The dual 60 MHz EL2224 consumes only 10 mA, making it ideal for video applications. The EL2224 has short circuit protected outputs and will operate from $\pm 5V$ to $\pm 15V$. It is fabricated using Elantec's Complementary Bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: *"Elantec's Military Processing, Monolithic Integrated Circuits"*.

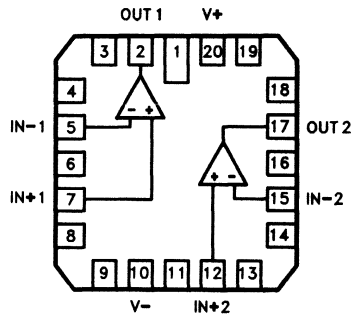
Connection Diagrams

EL2224J/CN



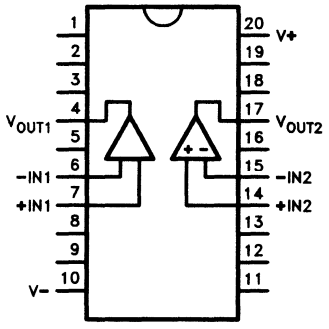
2224-1

EL2224L



2224-2

EL2224CM



2224-3

This product covered under U.S. Patent No. 4,837,523

EL2224/EL2224C

Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage Between V+ and V−	35V
Differential Input Voltage	±6V
Internal Power Dissipation	See Curves
Peak Output Current	Short Circuit Protected
Output Short Circuit Duration (Note 1)	Continuous

Operational Temperature Range	
EL2224	−55°C to +125°C
EL2224C	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	
CerDIP, LCC	175°C
Plastic DIP, SOL	150°C
Lead Temperature	
DIP Package	300°C
SOL Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	EL2224					EL2224C				Units
		Temp	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	+25°C Full		0.5	5 8	I I		0.5	5 8	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V		20		V	µV/°C
I_B	Bias Current	+25°C Full		1.5	4 6	I I		1.5	4 6	I III	µA µA
I_{OS}	Offset Current	+25°C Full		0.2	2 3	I I		0.2	2 3	I III	µA µA
R_{IN}	Input Resistance	+25°C		40		V		40		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±12		I	±10	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		15		V		15		V	$nV/\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	+25°C Full	4k 2.5k	6k		I	4k 2.5k	6k		I III	V/V V/V

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified — Contd.

Parameter	Description	EL2224					EL2224C				Units
		Temp	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	80		I	60	80		II	dB
V_O	Output Voltage Swing	Full	±11	±12.5		I	±11	±12.5		II	V
I_{SC}	Short Circuit Current	25°C		±50	±70	I		±50	±70	I	mA
R_O	Output Resistance	25°C		40		V		40		V	Ω
I_s	Supply Current	Full		9.5	13	I		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	60	75		I	60	75		II	dB

AC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	EL2224					EL2224C				Units
		Temp	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	25°C		60		V		60		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	25°C	2.4	3.1		I	2.4	3.1		I	MHz
t_r	Rise Time (Note 8)	25°C		6		V		6		V	ns
OS	Overshoot (Note 8)	25°C		20		V		20		V	%
SR	Slew Rate (Note 8)	25°C	150	200		I	150	200		I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%	25°C		120		V		120		V	ns
Ch S_p	Channel Separation (f = 10 MHz)	Full		70		V		70		V	dB

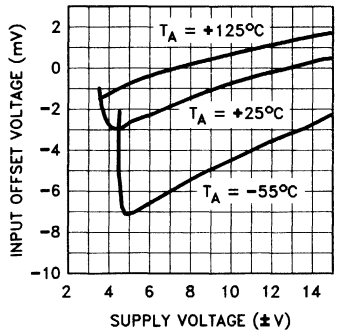
Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_O = ±10V.
Note 3: R_L = 2 kΩ.
Note 4: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0 to −10V.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: V_O = 100 mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/ 2 π V_{PEAK}.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.
Note 10: A_V = + 1, R_L = 2 kΩ.

EL2224/EL2224C

Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

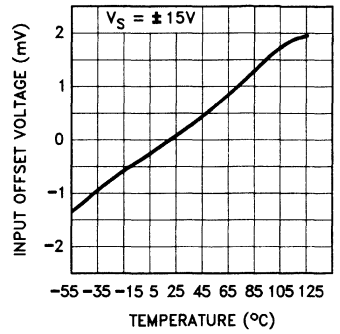
Typical Performance Curves

Input Offset Voltage vs Supply Voltage



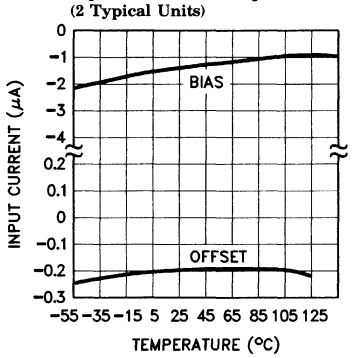
2224-4

Normalized Input Offset Voltage vs Temperature



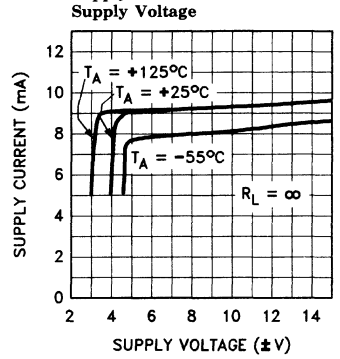
2224-5

Input Current vs Temperature (2 Typical Units)



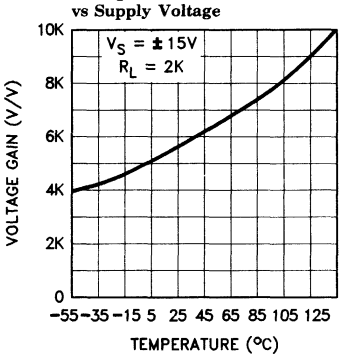
2224-6

Supply Current vs Supply Voltage



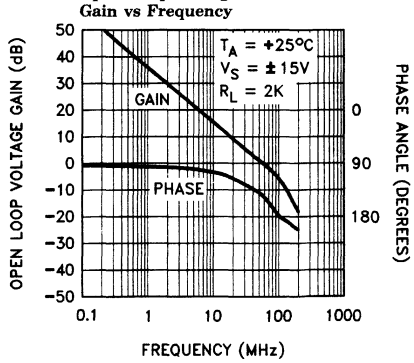
2224-7

Voltage Gain vs Supply Voltage



2224-8

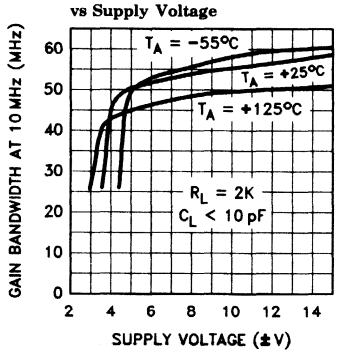
Open Loop Voltage Gain vs Frequency



2224-9

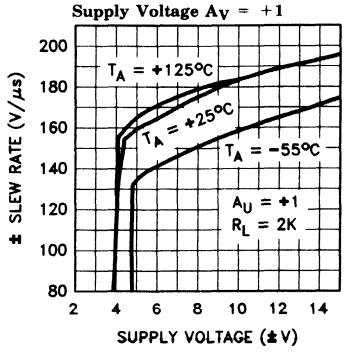
Typical Performance Curves — Contd.

Gain Bandwidth at 10 MHz vs Supply Voltage



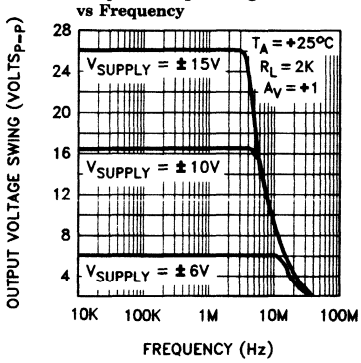
2224-10

Slew Rate vs Supply Voltage A_V = +1



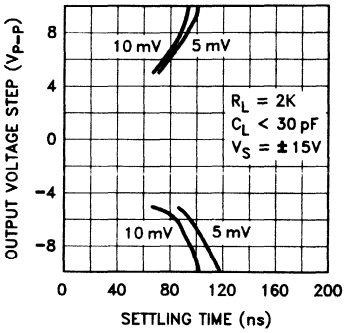
2224-11

Output Voltage Swing vs Frequency



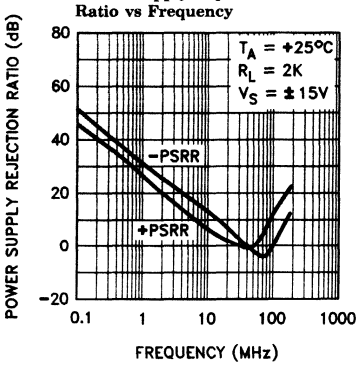
2224-12

Settling Time A_V = +1



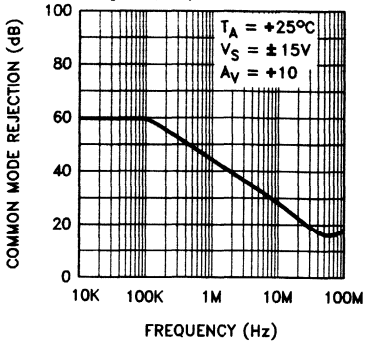
2224-13

Power Supply Rejection Ratio vs Frequency



2224-14

Common Mode Rejection vs Frequency A_V = +10

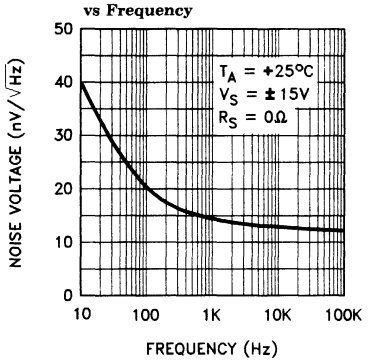


2224-15

EL2224/EL2224C
Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

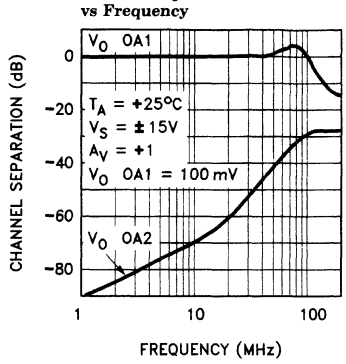
Typical Performance Curves — Contd.

Noise Voltage vs Frequency



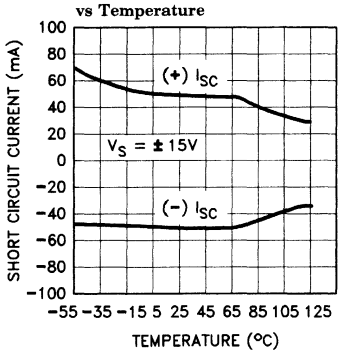
2224-16

Channel Separation vs Frequency



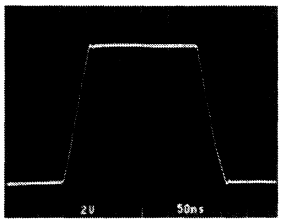
2224-17

Short Circuit Current vs Temperature



2224-18

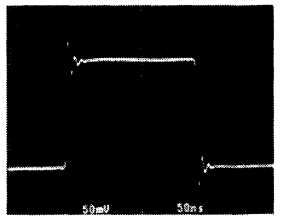
Large Signal Response



A_V = +1
V_{IN} = ±5V
V_O = ±5V
R_L = 2k

2224-19

Small Signal Response

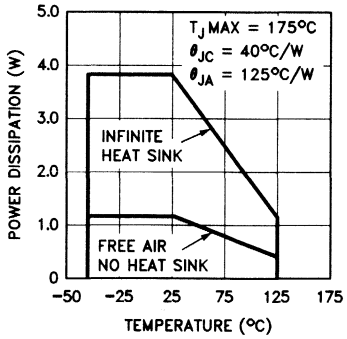


A_V = +1
V_{IN} = ±100 mV
V_O = ±100 mV
R_L = 2k

2224-20

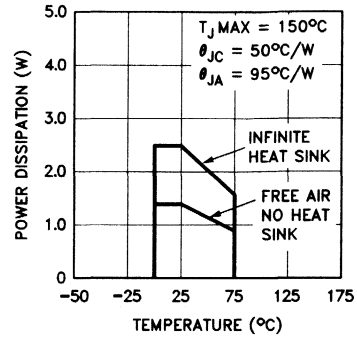
Typical Performance Curves — Contd.

8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



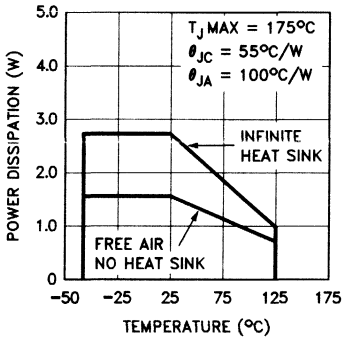
2224-21

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



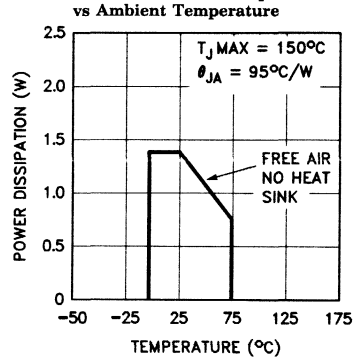
2224-22

20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



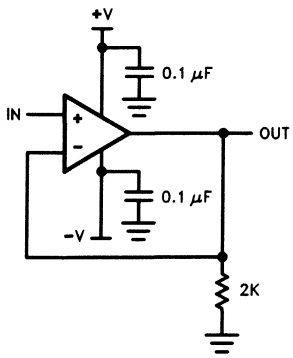
2224-23

20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2224-24

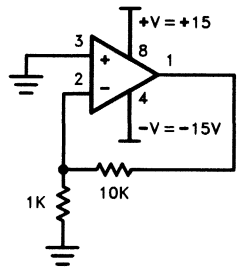
Test Circuit



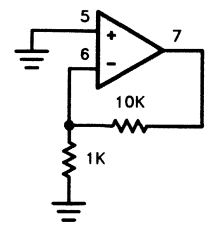
2224-27

A_V = +1
$C_L \leq$ 10 pF Scope Probe

Burn-In Circuit



2224-28

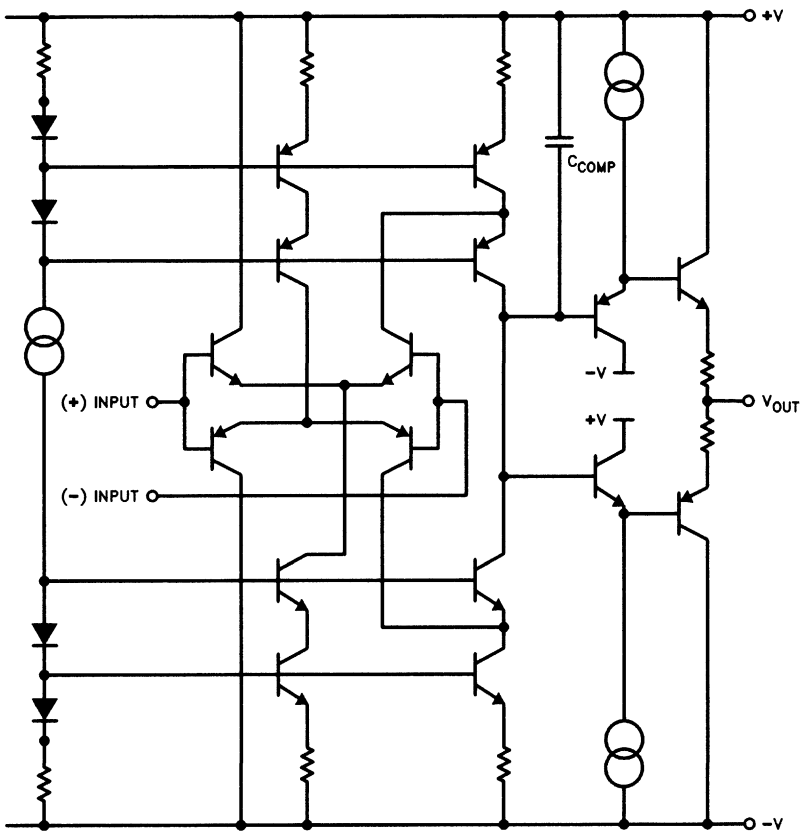


2224-29

Pin numbers are for the 8-lead CerDIP.
Burn-in circuit is identical for all package types.

EL2224/EL2224C
Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

Simplified Schematic (one amplifier)



EL2242/EL2242C

Dual Fast Single-Supply Unity-Gain Stable Op Amp

Features

- Inputs and outputs operate at negative supply rail
- Unity gain bandwidth—30 MHz
- High slew rate—40 V/μs
- Settles to 0.01% of a 10V swing in 500 ns
- Operates with supplies as low as 3V or as great as 32V while consuming only 3.7 mA per amplifier
- Large open loop gain—110 dB
- Inputs tolerant of overload
- MIL-STD-883 Rev. C compliant

Applications

- Battery-powered instruments
- 12-bit DAC output amplifiers
- Fast-settling instrumentation amplifiers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2242CJ	0°C to +75°C	8-Pin CerDIP	MDP0010
EL2242CN	0°C to +75°C	8-Pin P-DIP	MDP0006
EL2242CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2242J	0°C to +75°C	8-Pin CerDIP	MDP0010
EL2242J/883B	−55°C to +125°C	8-Pin CerDIP	MDP0010

General Description

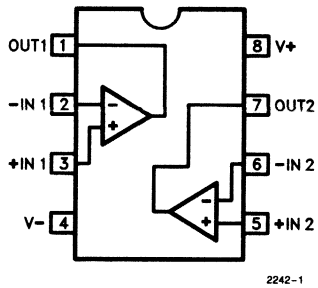
The EL2242 dual monolithic operational amplifier is as flexible as prior 324 devices but offers 30 times the bandwidth and slew-rate. Its inputs and outputs are able to operate down to the negative supply and are not damaged by overloads.

The EL2242 is useable in battery-operated systems with supplies as low as 3V, yet it has excellent gain and settling times while consuming only 3.7 mA per amplifier.

Elantec's EL2242/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document QRA-2: *Elantec's Military processing-Monolithic Products.*

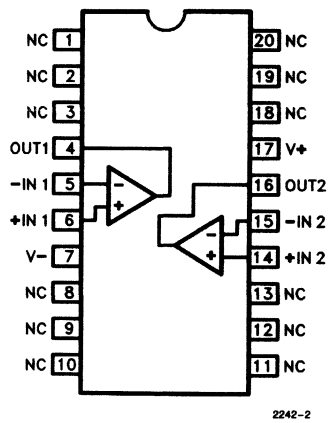
Connection Diagrams

Mini DIP



Top View

SOL



Top View

EL2242/EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	
Voltage between −IN and +IN pins	36V	CerDIP	175°C
Voltage at −IN or +IN pins	V+ to V−	Plastic DIP	150°C
Output Current	50 mA (Peak)	Storage Temperature Range	−65°C to +150°C
	30 mA (Continuous)	Lead Temperature	
Current into +IN or −IN	5 mA	DIP Package	
Internal Power Dissipation	See Curves	(Soldering, <10 seconds)	300°C
Operating Ambient Temperature Range		SOL Package	
EL2242	−55°C to +125°C	Vapor Phase (<60 seconds)	215°C
EL2242C	0°C to +75°C	Infrared (<15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V; R_L = 1k; T_A = 25°C, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2242	EL2242C	
V_{OS}	Input Offset Voltage	25°C		2	5	I	I	mV
		Full			7	I	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		7		V	V	µV/°C
I_B	Input Bias Current	25°C		0.5	0.7	I	I	µA
		Full			1.0	I	III	µA
I_{OS}	Input Offset Current	25°C		0.01	0.1	I	I	µA
		Full			0.2	I	III	µA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		20		V	V	MΩ
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		100		V	V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	V	pF
V_{CM+}	Positive Common-Mode Input Range	Full	12	13.3		I	II	V
V_{CM-}	Negative Common-Mode Input Range	Full	−15	−15.3		I	II	V
E_{IN}	Input Noise Voltage (f = 1 kHz, R_S = 0Ω)	25°C		15		V	V	nV/√Hz

DC Electrical Characteristics

$V_S = \pm 15V$; $R_L = 1k$; $T_A = 25°C$, unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2242	EL2242C	
A_{VOL}	Large Signal Voltage Gain ($V_O = \pm 10V$)	25°C	150	300		I	I	V/mV
		Full	35			I	III	V/mV
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	80	95		I	II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	76	95		I	II	dB
V_O	Output Voltage Swing	Full	±12	±13.5		I	II	V
	Negative Swing, R_L to V−	Full	−14.98	−15		I	II	V
I_O	Output Current (Note 3)	Full	±15	±25	±50	I	II	mA
I_S	Supply Current (Both Amplifiers)	Full		8.2	10	I	II	mA

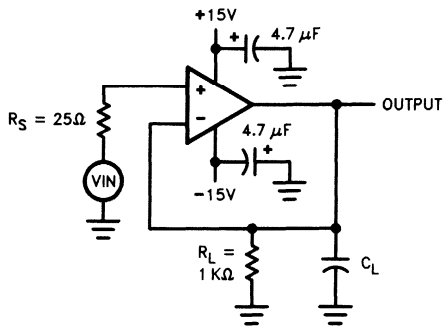
AC Electrical Characteristics

$V_S = \pm 15V$; $R_L = 1\ k\Omega$; $C_L = 20\ pF$; $T_A = 25°C$, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level		Units
					EL2242	EL2242C	
BW	Unity Gain −3 dB Bandwidth (Note 4)		30		V	V	MHz
GBW	Gain-Bandwidth Product (Note 4)		16		V	V	MHz
SR	Slew Rate ($V_O = \pm 10V$)		40		V	V	V/μs
OS	Overshoot (Note 4)		30		V	V	%
t_s	Settling Time to 0.1%		480		V	V	ns
	10V Step to 0.01%		550		V	V	ns

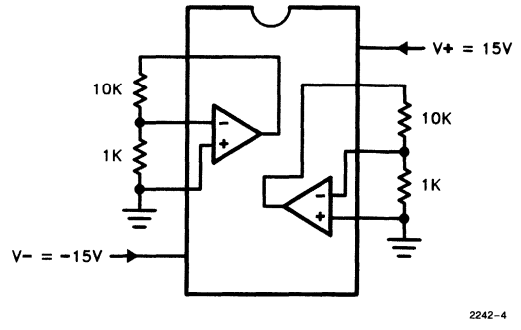
Note 1: Two tests are performed with V_{CM} = 0V to −12V and V_{CM} = 0V to 12V.
Note 2: Two tests are performed with V+ = 3V, V− changed from −2V to −27V; V− = −2V, V+ changed from 3V to 28V.
Note 3: The inputs are overdriven by ±15V and the output $R_L = 100\Omega$.
Note 4: V_{IN} = 100 mV peak-to-peak.

Test Circuit



2242-3

Burn-In Circuit

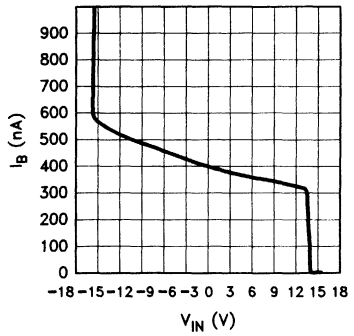


2242-4

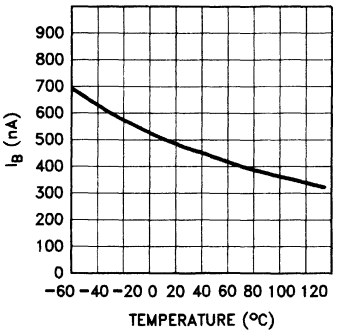
EL2242/EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Typical Performance Curves

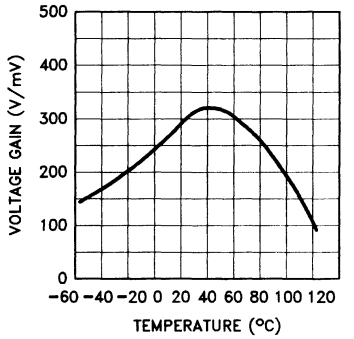
Input Bias Current vs Common-Mode Voltage



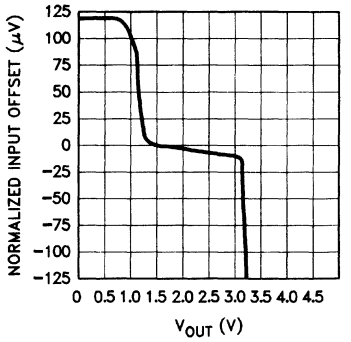
Input Bias Current vs Temperature



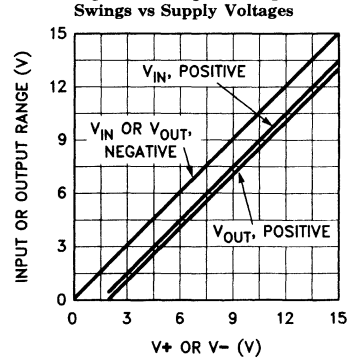
Voltage Gain vs Temperature



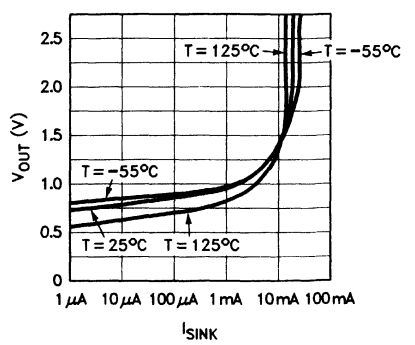
Input-Output Transfer Function, +5V Supply



Input and Output Voltage Swings vs Supply Voltages



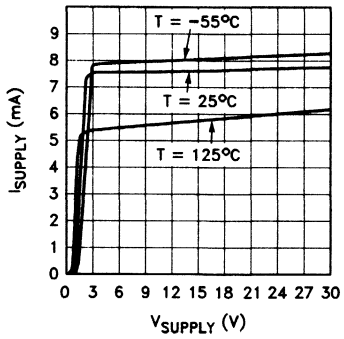
Output Voltage vs Current Sinking



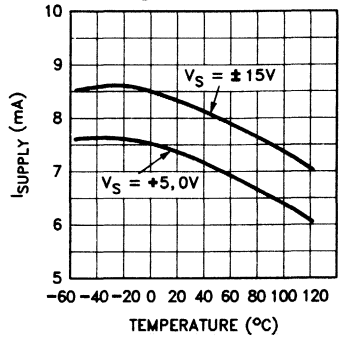
2242-5

Typical Performance Curves — Contd.

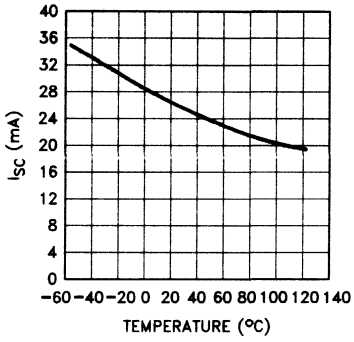
Supply Current vs Supply Voltage—Both Amplifiers



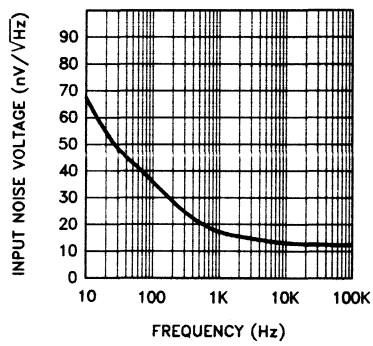
Supply Current vs Temperature Both Amplifiers



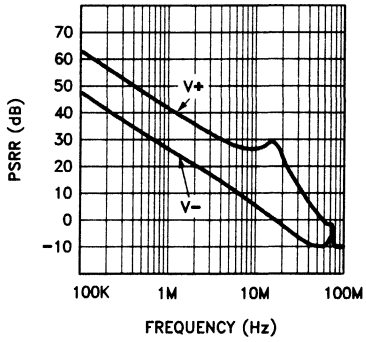
Output Short-Circuit Current vs Temperature



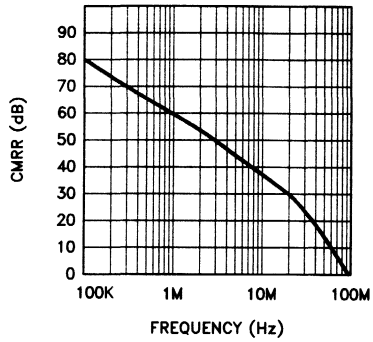
Input Voltage Noise vs Frequency



Power Supply Rejection Ratio vs Frequency



Common-Mode Rejection Ratio vs Frequency

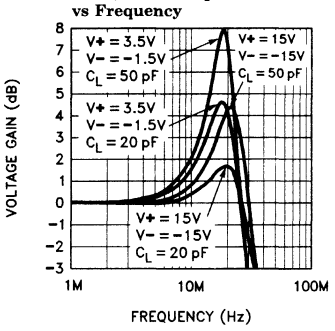


2242-6

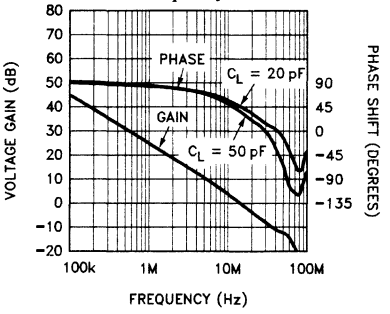
EL2242/EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Typical Performance Curves — Contd.

Utility-Gain Response vs Frequency

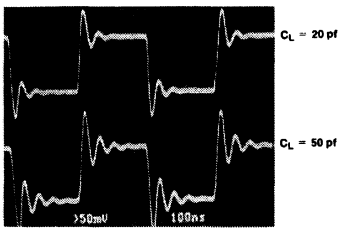


Open-Loop Gain and Phase vs Frequency



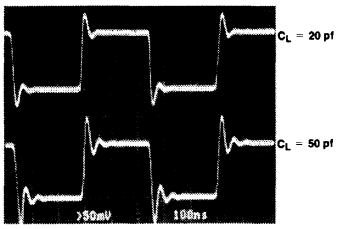
2242-7

Pulse Response with V+ = 3V, V− = −2V



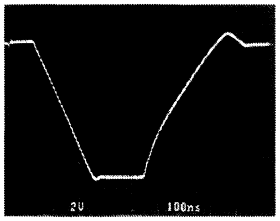
2242-8

Pulse Response with V+ = 15V, V− = −15V



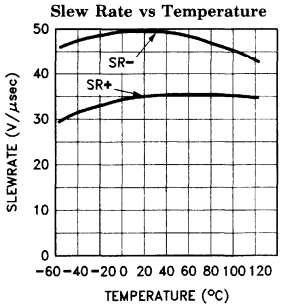
2242-9

Slew Characteristics



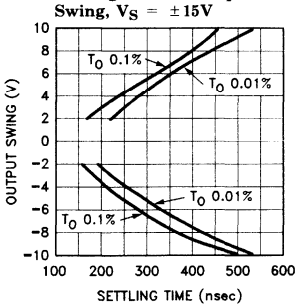
2242-10

Slew Rate vs Temperature

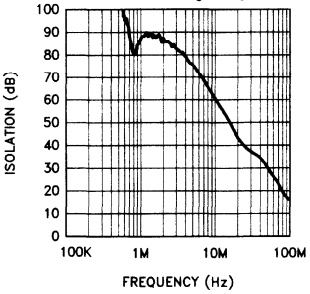


2242-11

Settling Time vs Output Swing, V_S = ±15V



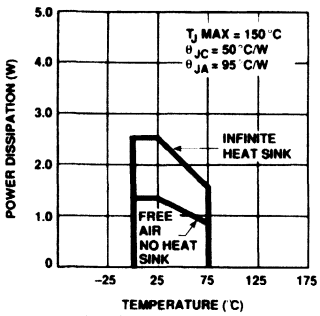
Amplifier-to-Amplifier Isolation vs Frequency



2242-12

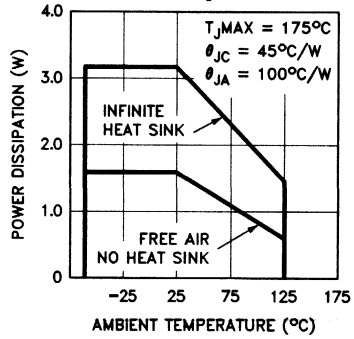
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



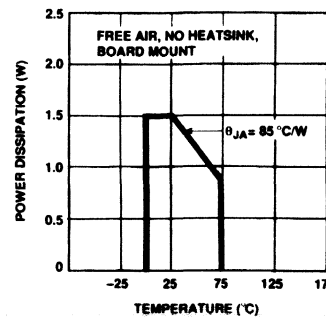
2242-13

8-Pin CerDIP Package
Maximum Power Dissipation
vs Ambient Temperature



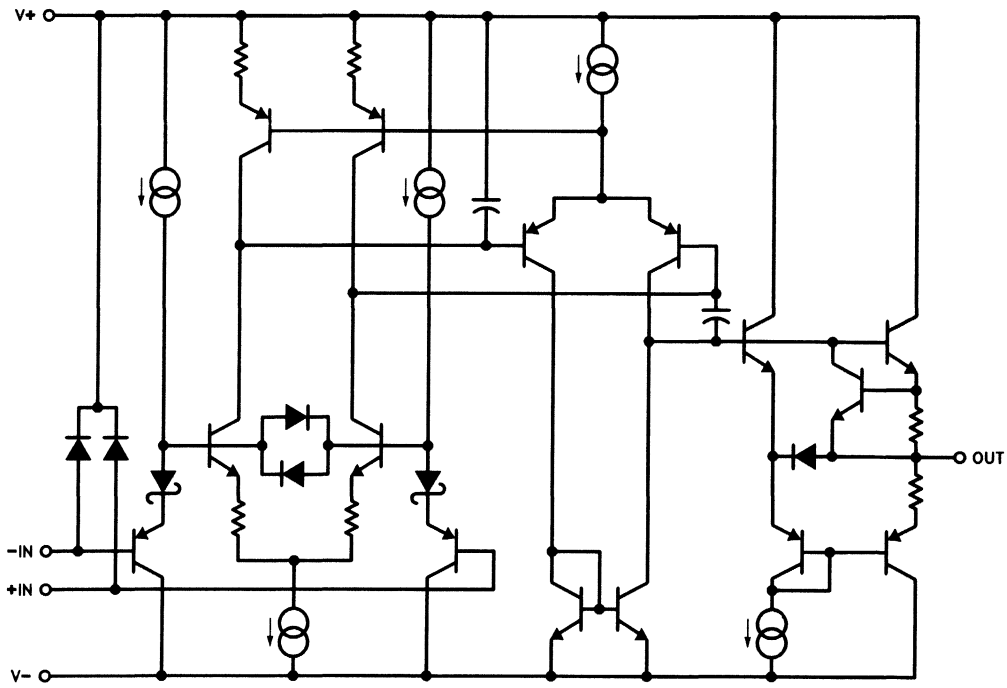
2242-14

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2242-15

Simplified Schematic (One Amplifier)



2242-16

EL2242/EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Applications Information

The EL2242 is a fast amplifier designed to operate from a very wide range of power supply voltages. The inputs operate all the way to the negative supply (actually about 200 mV below it) and up to typically 2V below the positive supply. The outputs swing a similar range, but some attention is required in practice.

Specifically, while the output NPN transistor can source load current over the full output span (see the simplified schematic), the output PNP device simply turns off at negative swings below about a volt above the negative supply rail. This property is shown in the "Output Voltage vs Current-Sinking" typical curve. All single-supply amplifiers have this characteristic, and the solution is to provide a load resistor from the output to the negative supply rail.

When the output is in this extreme negative swing region, the bandwidth, gain, and settling properties are all degraded by a factor of about 2. Even so, the AC characteristics are well-behaved in this region.

Electrostatic discharge protection devices clamp the inputs a diode drop above V+ and a diode drop below V−.

As for all amplifiers, good supply bypassing will optimize settling and amplifier-to-amplifier rejection. 4.7 μF tantalum capacitors seem to be the best, and no additional small capacitor is needed in parallel for very high-frequency bypassing. Reasonably low feedback impedances are important to preserving closed-loop stability, 1k or less being acceptable when capacitive parasitics are minimized. Stability is best when the EL2242 is operated from large supplies, especially when driving capacitive loads.

EL2243/EL2243C

Dual Fast Single-Supply Decompensated Op Amp

Features

- Inputs and outputs operate at negative supply rail
- Gain bandwidth product—70 MHz
- High slew rate—90 V/μs
- Settles to 0.01% of a 10V swing in 400 ns
- Operates with supplies as low as 3V or as great as 32V while consuming only 3.7 mA per amplifier
- Large open loop gain—114 dB
- Inputs tolerant of overload
- MIL-STD-883 Rev. C compliant

Applications

- Battery-powered instruments
- 12-bit DAC output amplifiers
- Fast-settling instrumentation amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2243CJ	0°C to +75°C	8-Pin CerDIP	MDP0010
EL2243CN	0°C to +75°C	8-Pin P-DIP	MDP0006
EL2243CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2243J	−55°C to +125°C	8-Pin CerDIP	MDP0010
EL2243CJ/883B	−55°C to +125°C	8-Pin CerDIP	MDP0010

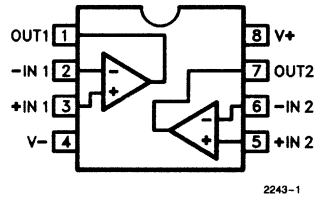
General Description

The EL2243 dual monolithic operational amplifier is as flexible as prior 324 devices but offers 100 times the bandwidth and slewrate. Its inputs and outputs are able to operate down to the negative supply and are not damaged by overloads.

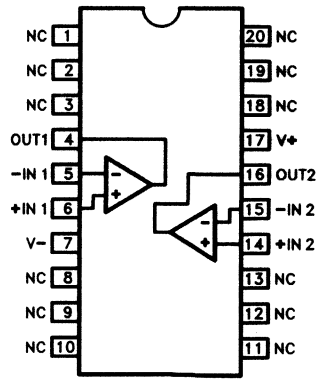
The EL2243 is useable in battery-operated systems with supplies as low as 3V, yet it has excellent gain and settling times while consuming only 3.7 mA per amplifier.

Elantec's EL2243/883B complies with MIL-STD-883 Revision C in all aspects, including burn-in at 125°C. Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document QRA-2: *"Elantec's Military processing-Monolithic Products"*.

Connection Diagrams



2243-1



2243-2

EL2243/EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	
Voltage between −IN and +IN Pins	36V	CerDIP	175°C
Voltage at −IN or +IN Pins	V+ to V−	Plastic DIP	150°C
Output Current	50 mA (Peak)	Storage Temperature Range	−65°C to +150°C
	30 mA (Continuous)	Lead Temperature	
Current into +IN or −IN	5 mA	DIP Package	
Internal Power Dissipation	See Curves	(Soldering, 10 seconds)	300°C
Operating Ambient Temperature Range		SOL Package	
EL2243	−55°C to +125°C	Vapor Phase (<60 seconds)	215°C
EL2243C	0°C to +75°C	Infrared (<15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1k; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2243	EL2243C	
V_{OS}	Input Offset Voltage	25°C Full		1.5	5 7	I I	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift	Full		5		V	V	µV/C
I_B	Input Bias Current	25°C Full		0.5	0.7 1.0	I I	I III	µA µA
I_{OS}	Input Offset Current	25°C Full		0.01	0.1 0.2	I I	I III	µA µA
R_{IN}, Diff	Input Differential Resistance	25°C		10		V	V	MΩ
R_{IN}, Comm	Input Common-Mode Resistance	25°C		100		V	V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	V	pF
V_{CM+}	Positive Common-Mode Input Range	Full	12	13.3		I	II	V
V_{CM-}	Negative Common-Mode Input Range	Full	−15	−15.3		I	II	V
E_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		12		V	V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (V_O = ±10V)	25°C Full	250 80	500		I I	I III	V/mV V/mV
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	80	100		I	II	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k$; $T_A = 25°C$ unless otherwise specified — Contd.

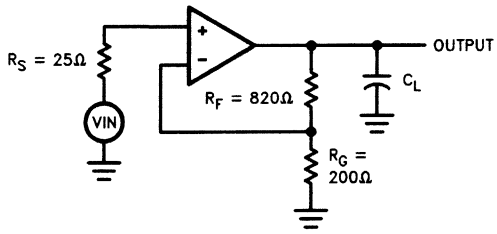
Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2243	EL2243C	
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	80	100		I	II	dB
V_O	Output Voltage Swing	Full	±12	±13.5		I	II	V
	Negative Swing, R_L to V−	Full	−14.98	−15		I	II	V
I_O	Output Current (Note 3)	Full	±15	±25	±50	I	II	mA
I_S	Supply Current (Both Amplifiers)	Full		8.2	10	I	II	mA

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 1\,k\Omega$; $C_L = 20\,pF$; $T_A = 25°C$; unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level		Units
					EL2242	EL2242C	
GBW	Gain-Bandwidth Product (Note 4)		70		V	V	MHz
SR	Slew Rate ($V_O = \pm 10V$)		90		V	V	V/μs
OS	Overshoot (Note 4)		30		V	V	%
t_s	Settling Time to 0.1%		320		V	V	ns
	10V Step to 0.01%		380		V	V	ns

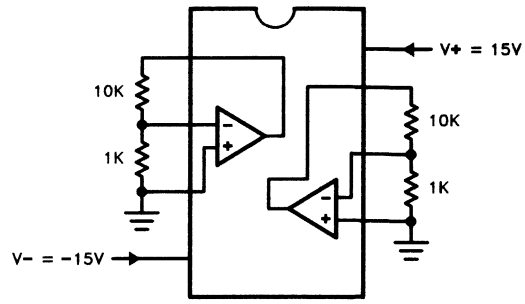
Note 1: Two tests are performed with V_{CM} = 0V to −12V and V_{CM} = 0V to 12V.
Note 2: Two tests are performed with V+ = 3V, V− changed from −2V to −27V; V− = −2V, V+ changed from 3V to 28V.
Note 3: The inputs are overdriven by ±15V and the output R1 = 100Ω.
Note 4: V_{OUT} = 100 mV peak-to-peak.

Test Circuit



2243-3

Burn-In Circuit

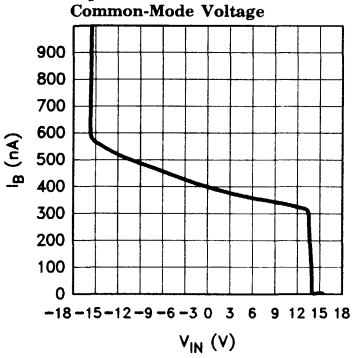


2243-4

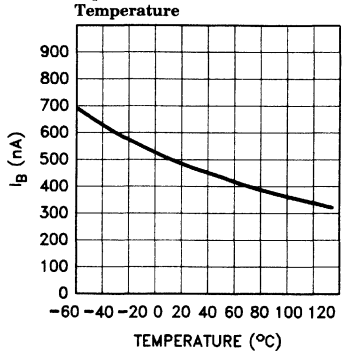
EL2243/EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Typical Performance Curves

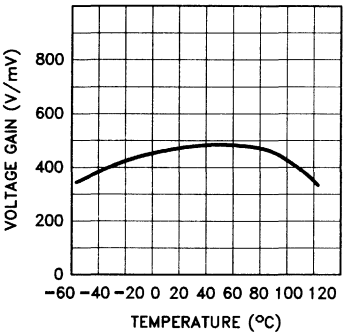
Input Bias Current vs Common-Mode Voltage



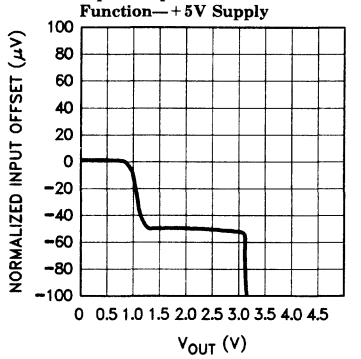
Input Bias Current vs Temperature



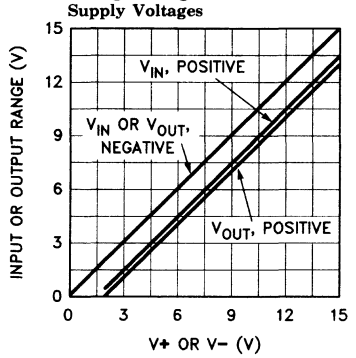
Voltage Gain vs Temperature



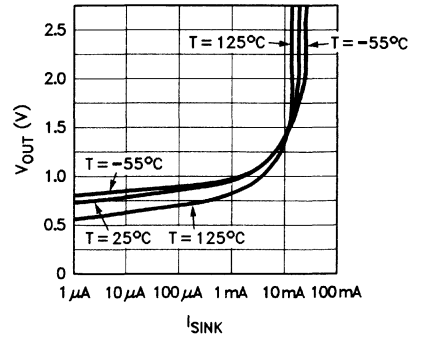
Input-Output Transfer Function—+5V Supply



Input and Output Voltage Swing vs Supply Voltages



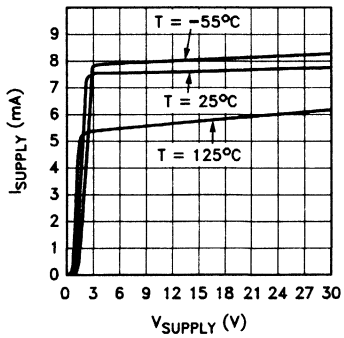
Output Voltage vs Current Sinking



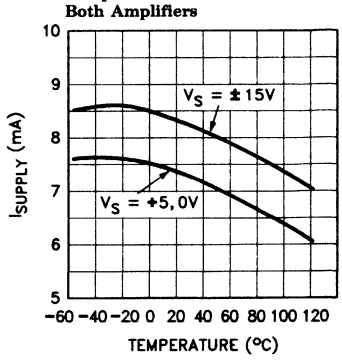
2243-5

Typical Performance Curves — Contd.

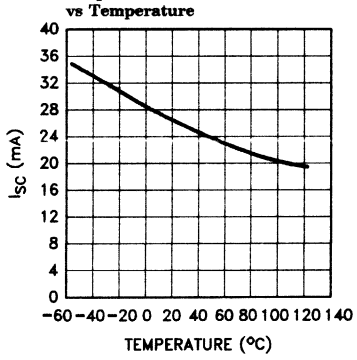
Supply Current vs Supply Voltage— Both Amplifiers



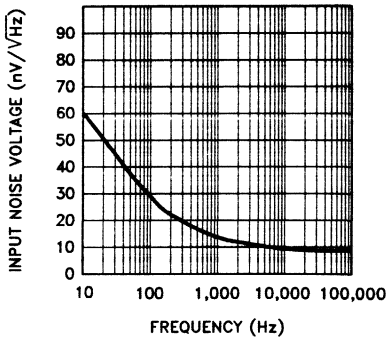
Supply Current vs Temperature— Both Amplifiers



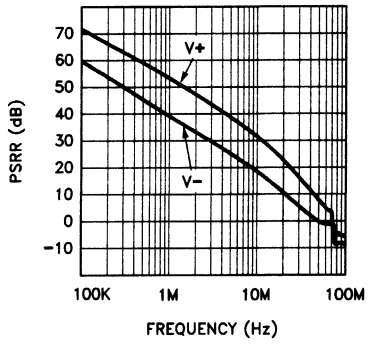
Output Short-Circuit Current vs Temperature



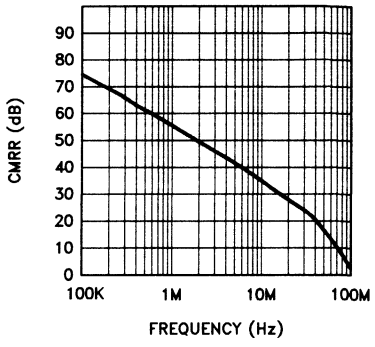
Input Voltage Noise vs Frequency



Power Supply Rejection Ratio vs Frequency



Common-Mode Rejection Ratio vs Frequency

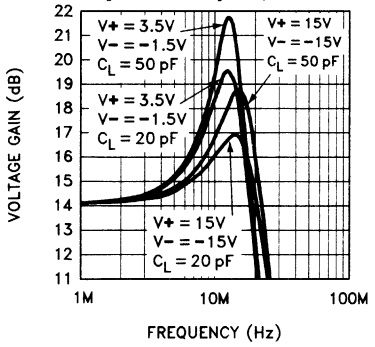


2243-6

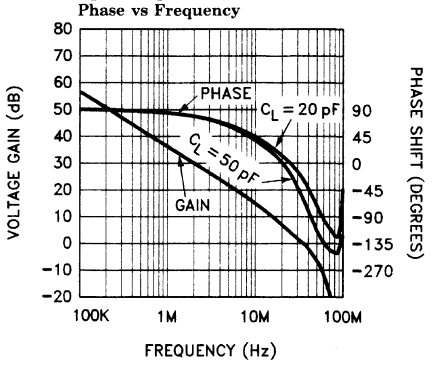
EL2243/EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Typical Performance Curves — Contd.

Gain of +5 Response vs Frequency

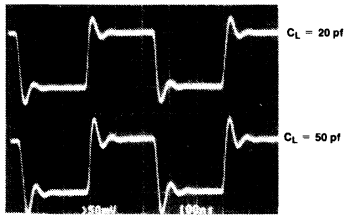


Open-Loop Gain and Phase vs Frequency



2243-7

Pulse Response with V+ = 15V, V− = −15V

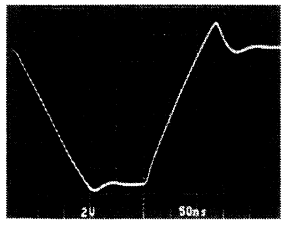


2243-8

Pulse Response with V+ = 3V, V− = −2V

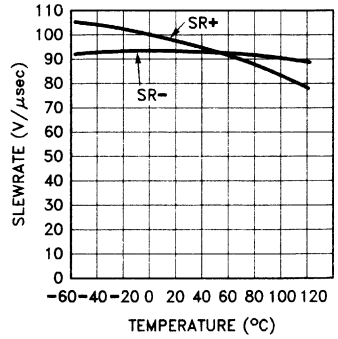
2243-9

Slew Characteristic



2243-10

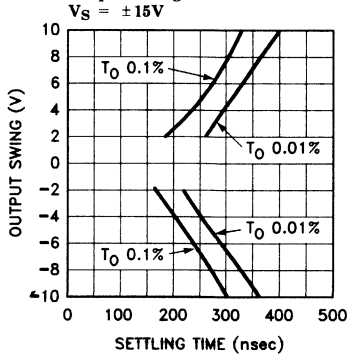
Slew Rate vs Temperature



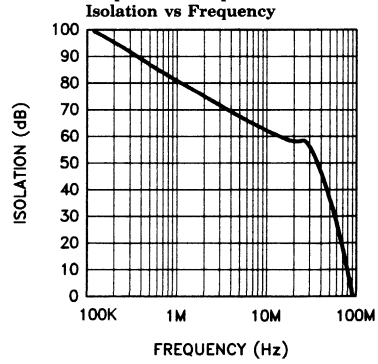
2243-11

Typical Performance Curves — Contd.

Settling Time vs Output Swing
$V_S = \pm 15V$

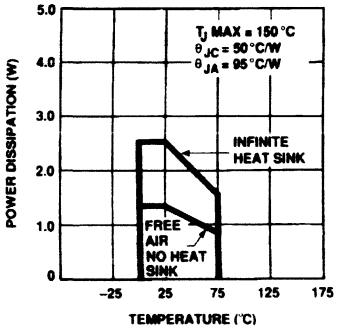


Amplifier-to-Amplifier Isolation vs Frequency



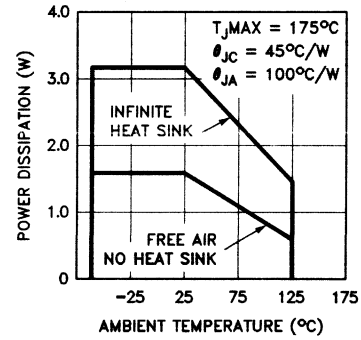
2243-12

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



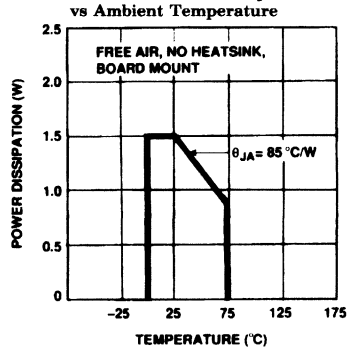
2243-13

8-Pin CerDIP Package Maximum Power Dissipation vs Ambient Temperature



2243-14

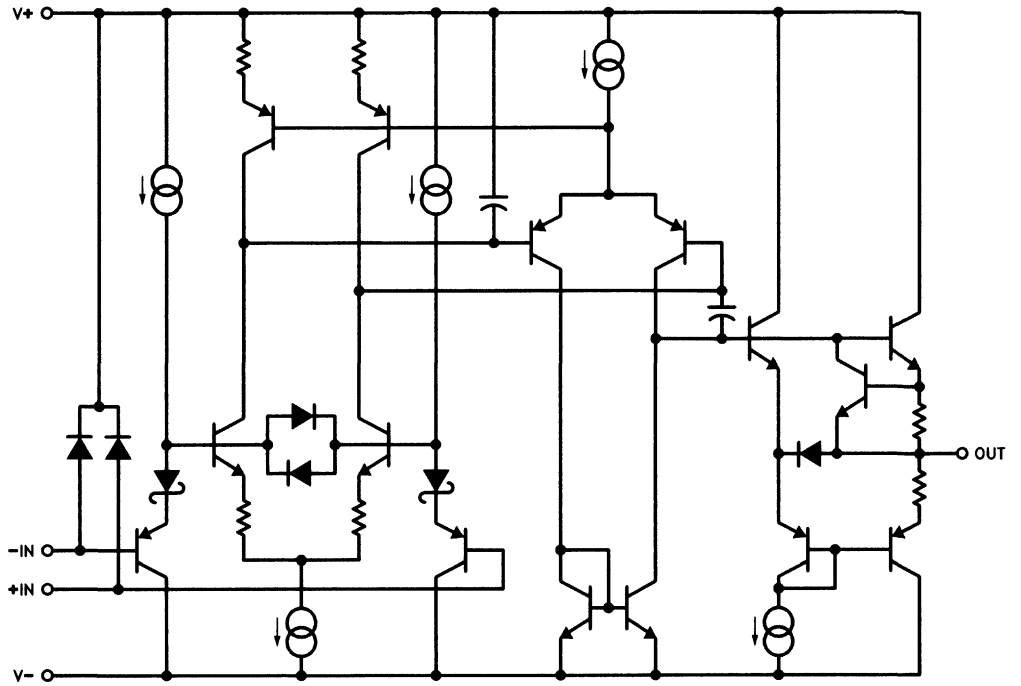
20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2243-15

EL2243/EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Simplified Schematic (One Amplifier)



2243-16

Applications Information

The EL2243 is a fast amplifier designed to operate from a very wide range of power supply voltages. The inputs operate all the way to the negative supply (actually about 200 mV below it) and up to typically 2V below the positive supply. The outputs swing a similar range, but some attention is required in practice.

Specifically, while the output NPN transistor can source load current over the full output span (see the simplified schematic), the output PNP device simply turns off at negative swings below about a volt above the negative supply rail. This property is shown in the "Output Voltage vs. Current-Sinking" typical curve. All single-supply amplifiers have this characteristic, and the solution is to provide a load resistor from the output to the negative supply rail.

When the output is in this extreme negative swing region, the bandwidth, gain, and settling properties are all degraded by a factor of about 2. Even so, the AC characteristics are well-behaved in this region.

Electrostatic discharge protection devices clamp the inputs a diode drop above V+ and a diode drop below V−.

As for all amplifiers, good supply bypassing will optimize settling and amplifier-to-amplifier rejection. 4.7 μF tantalum capacitors seem to be the best, and no additional small capacitor is needed in parallel for very high-frequency bypassing. Reasonably low feedback impedances are important to preserving closed-loop stability, 1k or less being acceptable when capacitive parasitics are minimized. Stability is best when the EL2243 is operated from large supplies, especially when driving capacitive loads.

EL2423/EL2423C

Quad De-Compensated High Speed Operational Amplifier

Features

- Stable for gains > 10
- Wide bandwidth—500 MHz
- High slew rate—350 V/μs
- Wide supply range—
  ±5V to ±15V
- Output short circuit protected
- Low supply current—4 mA per amplifier

Applications

- High frequency active filters
- Video amplifiers
- Pulse amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2423CJ	0°C to +75°C	CerDIP	MDP0010
EL2423CN	0°C to +75°C	P-DIP	MDP0006
EL2423J	−55°C to +125°C	CerDIP	MDP0010
EL2423J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2423L/883B	−55°C to +125°C	CerDIP	MDP0007
EL2423CM	0°C to +75°C	SOL	MDP0027

General Description

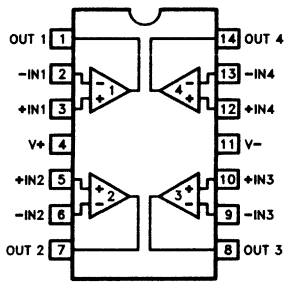
The EL2423 monolithic quad operational amplifier is an example of Elantec's commitment to high speed low power consumption products. This amplifier is stable for gains of 10 or greater, exhibits Slew Rates of 350V per microsecond, and a Gain Bandwidth of 500 MHz while drawing supply currents of 4 mA per amplifier. The output provides short circuit protection but is capable of delivering currents in excess of 50 mA. The device is manufactured using Elantec's advanced Complementary Bipolar process.

The EL2423 is available in 14-lead Plastic DIP, 14-lead CerDIP, 20-pad LCC, and 20-pad SOL.

Elantec's products and facilities comply with MIL-STD-883, Revision C, MIL-I-45082A, and other applicable quality assurance specifications. For information on Elantec's Military processing, see QRA-2, *"Elantec's Military Processing, Monolithic Integrated Circuits"*. For information on Elantec's Commercial processing, see QRA-1, *"Summary of Elantec's Reliability and Quality Assurance Policy"*.

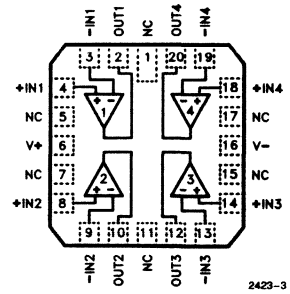
Connection Diagrams

EL2423J/CN

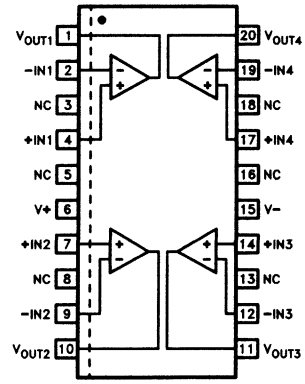


2423-1

EL2423L



2423-3



2423-2

EL2423/EL2423C
Quad De-Compensated High Speed Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	6V	Maximum Junction Temperature	
Peak Output Current	Short Circuit Protected	CerDIP, LCC	175°C
Output Short Circuit Duration (Note 1)	Continuous	Plastic DIP, SOL	150°C
Internal Power Dissipation	See Curves	Lead Temperature	
Operating Temperature Range		DIP Package	300°C
EL2423	−55°C to +125°C	SOL Package	
EL2423C	0°C to +75°C	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2423				EL2423C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	25°C		1.0	6	I		1.0	6	I	mV
		Full			10	I			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		10		V		10		V	µV/°C
I_B	Bias Current	25°C		1.0	4	I		1.0	4	I	µA
		Full			6	I			6	III	µA
I_{OS}	Offset Current	25°C		0.5	2	I		0.5	2	I	µA
		Full			3	I			3	III	µA
R_{IN}	Input Resistance	25°C		20		V		20		V	kΩ
C_{IN}	Input Capacitance	25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±11		I	±10	±11		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		7		V		7		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	25°C	20k	40k		I	20k	40k		I	V/V
		Full	10k			I	10k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	80		I	70	80		II	dB

DC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2423				EL2423C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	Full	±11	±12		I	±11	±12		II	V
I_O	Short Circuit Current	25°C	±10	+50	±85	I	±10	±50	±85	I	mA
R_O	Output Resistance	25°C		40		V		40		V	Ω
I_S	Supply Current	Full		16	18	I		16	18	II	mA
PSRR	Power Supply Rejection Ration (Note 5)	Full	70	80		I	70	80		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified

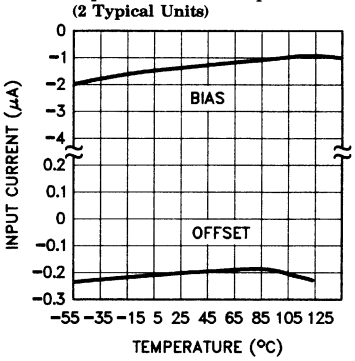
Parameter	Description	Temp	EL2423				EL2423C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	25°C		200		V		200		V	MHz
FPBW	Full Power Bandwidth (Note 7)	25°C	3.48	5.5		I	4.7	5.5		I	MHz
t_r	Rise Time (Note 6)	25°C		7		V		7		V	ns
OS	Overshoot (Note 6)	25°C		20		V		20		V	%
SR	Slew Rate (Note 6)	25°C	250	350		I	250	350		I	V/μs
t_s	Settling Time (Note 9) 10V Step to 0.05%	25°C		330		V		330		V	ns
CHSp	Channel Separation f = 10 MHz	25°C		70		V		70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: $V_O = \pm 10V$.
Note 3: $R_L = 2k\Omega$.
Note 4: Two tests are performed. $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0V$ to $-10V$.
Note 5: Two tests are performed. $V+ = 15V$, and $V-$ is changed from $-5V$ to $-15V$. $V- = -15V$, and $V+$ is changed from $+5V$ to $+15V$.
Note 6: $V_O = 100$ mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/2π V_{peak}.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurements are made with techniques in the following reference: *"Take The Guesswork Out of Settling-Time Measurements,"* EDN September 19, 1985.

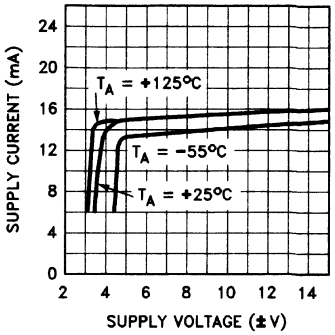
EL2423/EL2423C
Quad De-Compensated High Speed Operational Amplifier

Typical Performance Curves

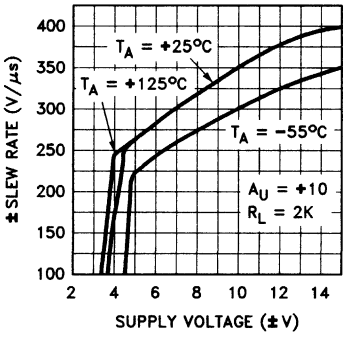
Input Current vs Temperature (2 Typical Units)



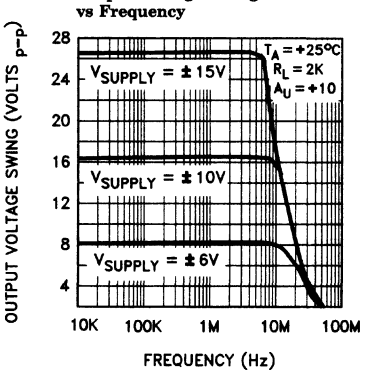
Supply Current vs Supply Voltage



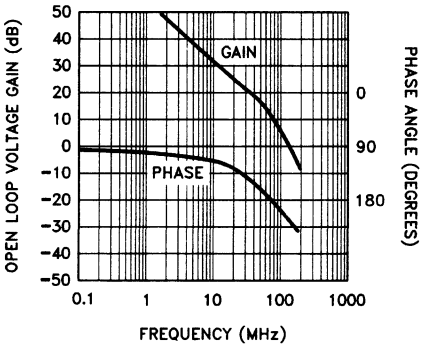
Slew Rate vs Supply Voltage



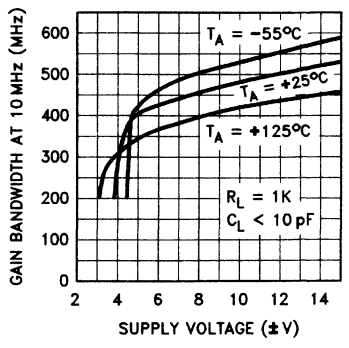
Output Voltage Swing vs Frequency



Open Loop Voltage Gain vs Frequency



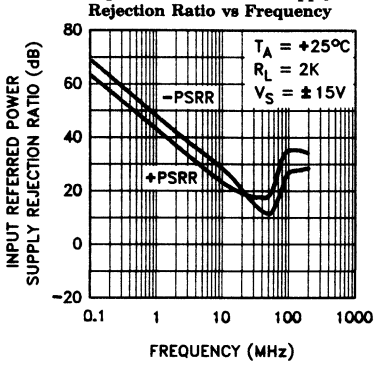
Gain Bandwidth at 10 MHz vs Supply Voltage



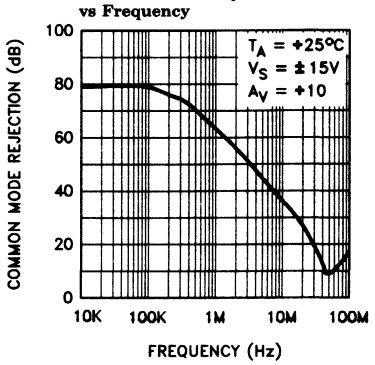
2423-4

Typical Performance Curves — Contd.

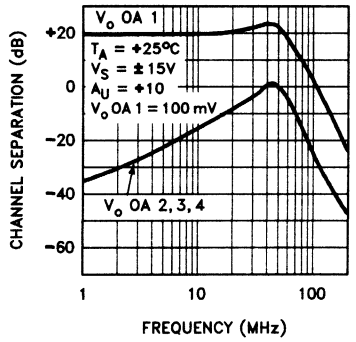
Input Referred Power Supply Rejection Ratio vs Frequency



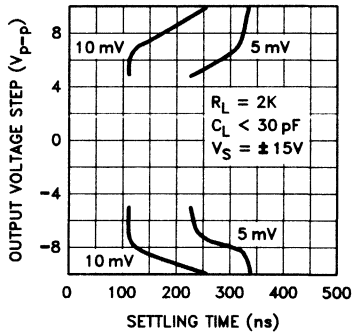
Common Mode Rejection vs Frequency



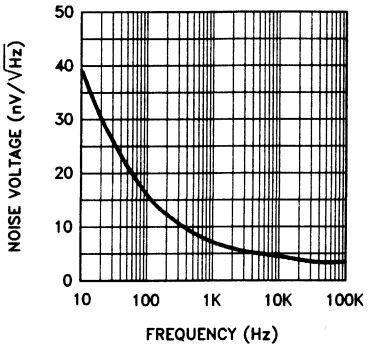
Channel Separation vs Frequency



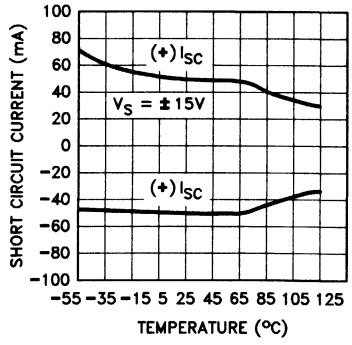
Settling Time A_V = +10



Noise Voltage vs Frequency



Short Circuit Current vs Temperature



2423-5

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0021/ELH0021C
1 Amp Power Operational Amplifier

Features

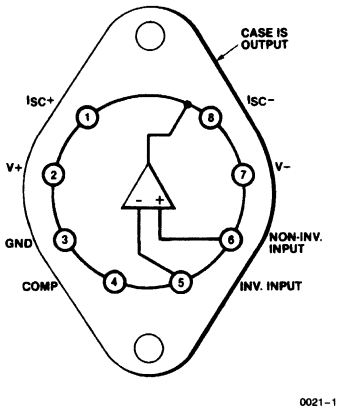
- High output current—1.2A
- Large output voltage swing—±12V
- Low standby power—100 mW
- Wide full power bandwidth—20 kHz
- Low input bias current
- Low input offset voltage
- High open-loop gain >100 dB
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0021CK	−25°C to +85°C	TO-3	MDP0003
ELH0021K	−55°C to +125°C	TO-3	MDP0003
ELH0021K/883B	−55°C to +125°C	TO-3	MDP0003

8508801YX is the DESC version of this device.

Connection Diagram



Top View

General Description

The ELH0021/ELH0021C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC op amps; the ELH0021 will provide output currents in excess of 1A at voltage levels of ±12V. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

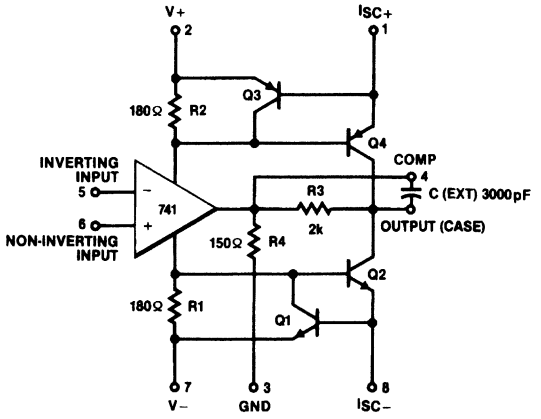
The excellent input characteristics and high output capability of the ELH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

Other applications include torque drivers for inertial guidance systems, diddle yoke drivers for alphanumeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The ELH0021 is supplied in an 8-pin TO-3 package rated at 20W with suitable heatsink. The ELH0021 is guaranteed over the temperature range of −55°C to +125°C while the ELH0021C is guaranteed from −25°C to +85°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Equivalent Schematic



ELH0021/ELH0021C
1 Amp Power Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage (Note 1)	±15V		ELH0021	−55°C to +125°C
P_D	Power Dissipation (See Curves)			ELH0021C	−25°C to +85°C
	Differential Input Voltage	±30V	T_{ST}	Storage Temperature	−65°C to +150°C
	Peak Output Current (Note 2)	2A		Lead Temperature	
	Output Short			(Soldering, 10 seconds)	300°C
	Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, C_C = 3000 pF

Parameter	Description	Test Conditions	ELH0021				ELH0021C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$, T_C = 25°C (Note 4)		1	3	I		3	6	I	mV
		$R_S \le 100\Omega$ (Note 4)			5	I			7.5	III	mV
$\Delta V_{OS}/\Delta T$	Voltage Drift with Temperature	$R_S \le 100\Omega$		3	25	IV		5	30	IV	µV/°C
	Offset Voltage Drift with Time	T_A = 25°C		5		V		5		V	$\mu V\sqrt{wk}$
$\Delta V_{OS}/\Delta P$	Offset Voltage Change with Output Power			5	15	I		5	20	II	µV/W
I_{OS}	Input Offset Current	T_C = 25°C (Note 4)		30	100	I		50	200	I	nA
		(Note 4)			300	I			500	III	nA
	Offset Current Drift with Temperature			0.1	1	IV		0.2	1	IV	nA/°C
	Offset Current Drift with Time	T_A = 25°C		2		V		2		V	$nA/\sqrt{wk}$
I_B	Input Bias Current	T_C = 25°C (Note 4)		100	300	I		200	500	I	nA
		(Note 4)			1	I			1	III	µA
R_{IN}	Input Resistance	T_C = 25°C	0.3	1		I	0.3	1		I	MΩ
CMRR	Common-Mode Rejection Ratio	$R_S \le 100\Omega$, V_{CM} = ±10V	70	90		I	70	90		II	dB
V_{INCM}	Input Voltage Range		±12			IV	±12			IV	V

ELH0021/ELH0021C
1 Amp Power Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$, $C_C = 3000$ pF — Contd.

Parameter	Description	Test Conditions	ELH0021				ELH0021C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $V_S = \pm 5V$ to $\pm 15V$	80	96		I	70	90		II	dB
A_{VOL}	Voltage Gain (Note 5)	$V_O = \pm 10V$, $R_L = 1$ kΩ, $T_C = 25°C$	100	200		I	100	200		I	V/mV
		$V_O = \pm 10V$, $R_L = 100\Omega$	25			I	20			II	V/mV
V_O	Output Voltage Swing	$R_L = 100\Omega$	± 13.5	14		I	± 13	± 14		II	V
		$R_L = 10\Omega$, $T_C = 25°C$	± 11	± 12		I	± 10	± 12		I	V
I_{SC}	Output Short Circuit Current	$T_C = 25°C$, $R_{SC} = 0.5\Omega$	0.8	1.2	1.6	I	0.8	1.2	1.6	I	A
I_S	Supply Current	$V_{OUT} = 0V$		2.5	3.5	I		3	4	II	mA
P_C	Power Consumption	$V_{OUT} = 0V$		75	105	I		90	120	II	mW

Note 1: Rating applies for supply voltages above $\pm 15V$. For supplies less than $\pm 15V$, rating is equal to supply voltage.
Note 2: Rating applies for ELH0021K with $R_{SC} = 0\Omega$.
Note 3: Rating applies as long as package power rating is not exceeded.
Note 4: Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$.
Note 5: The ELH0021, like all Class B amplifiers, has a "dead band" when V_{OUT} is near 0V. Typical values for the "dead band" are in the 50 μV to 200 μV range. Open-loop gain is measured at V_{OUT} from ± 0.5 V_{DC} TO ± 10.0 V_{DC} which is out of the range of the "dead band".

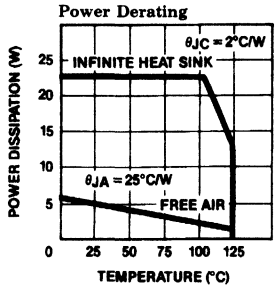
AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000$ pF

Parameter	Description	Test Conditions	ELH0021				ELH0021C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	$A_V = 1$, $R_L = 100\Omega$	1.5	3		I	1	3		I	V/μs
BW	Bandwidth	$R_L = 100\Omega$		20		V		20		V	kHz
t_r, t_f	Small Signal Rise or Fall Time			0.3	1	I		0.3	1.5	I	μs
	Small Signal Overshoot			5	20	I		10	30	I	%
t_S	Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = 1$		4		V		4		V	μs
	Overload Recovery Time			3		V		3		V	μs
HD	Harmonic Distortion	$f = 1$ kHz, $P_O = 0.5W$		0.2		V		0.2		V	%
e_n	Input Noise Voltage	$R_S = 50\Omega$, BW = 10 Hz to 10 kHz		5		V		5		V	μVrms
i_n	Input Noise Current	BW = 10 Hz to 10 kHz		0.05		V		0.05		V	nA_{rms}
C_{IN}	Input Capacitance			3		V		3		V	pF

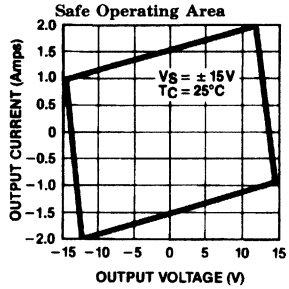
ELH0021/ELH0021C
1 Amp Power Operational Amplifier

Typical Performance Curves

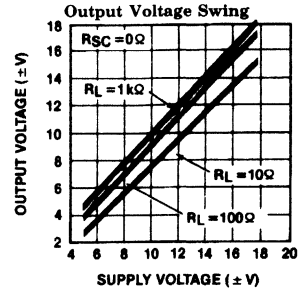
Power Derating



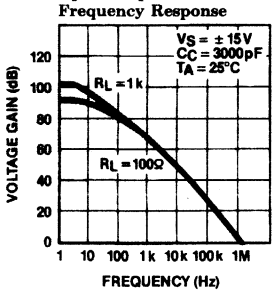
Safe Operating Area



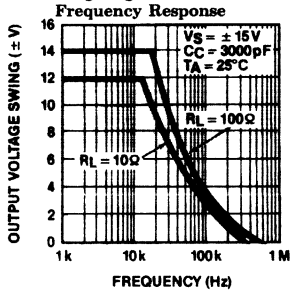
Output Voltage Swing



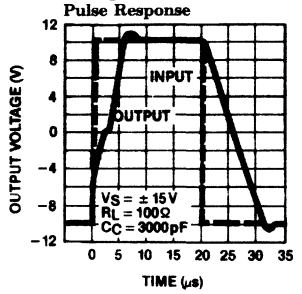
Open-Loop
Frequency Response



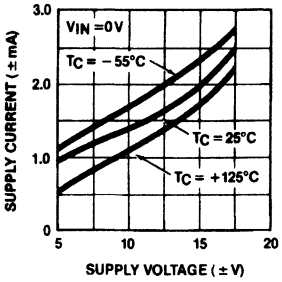
Large Signal
Frequency Response



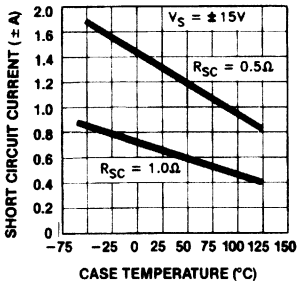
Voltage Follower
Pulse Response



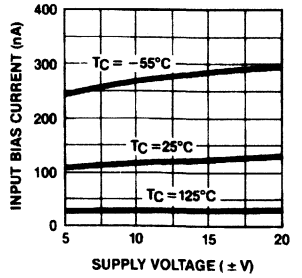
No Load Supply Current



Short Circuit Current
vs Temperature



Input Bias Current

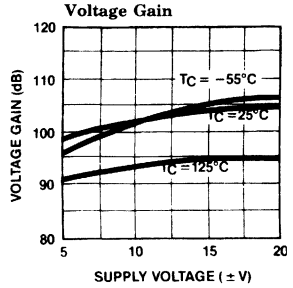


0021-3

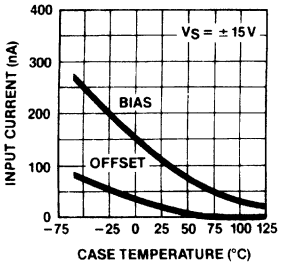
ELH0021/ELH0021C
1 Amp Power Operational Amplifier

Typical Performance Curves — Contd.

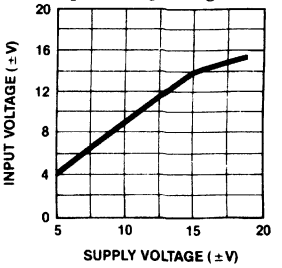
Voltage Gain



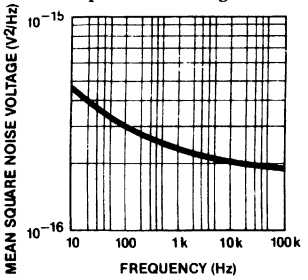
Input Current



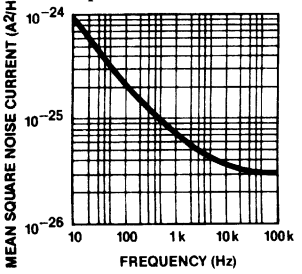
Input Voltage Range



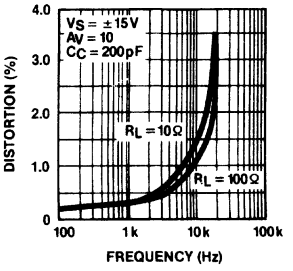
Input Noise Voltage



Input Noise Current



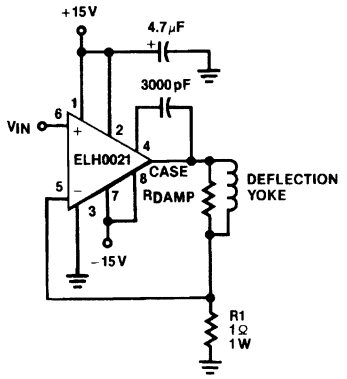
Distortion vs Frequency



0021-4

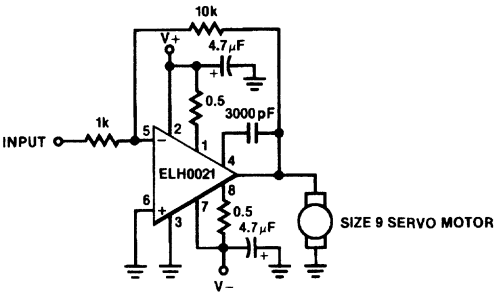
Typical Applications

CRT Deflection Yoke Driver



0021-5

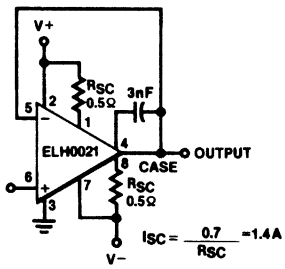
DC Servo Amplifier



0021-6

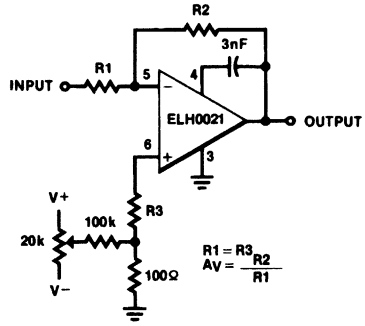
Typical Applications — Contd.

Unity Gain with Short Circuit Limiting



0021-7

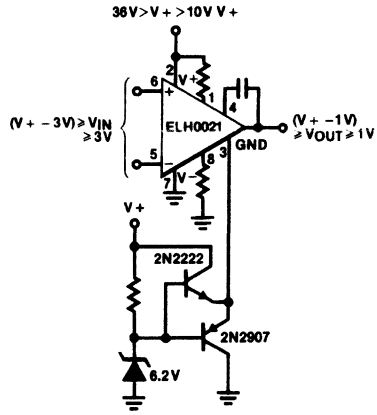
Offset Voltage Null Circuit



0021-8

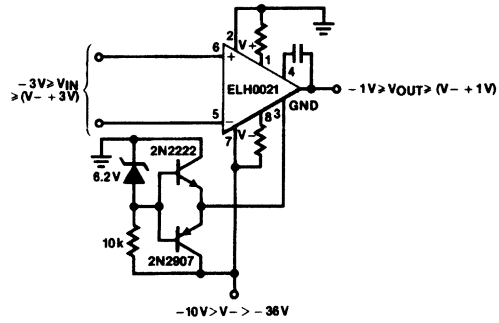
Operation from Single Supplies

Positive



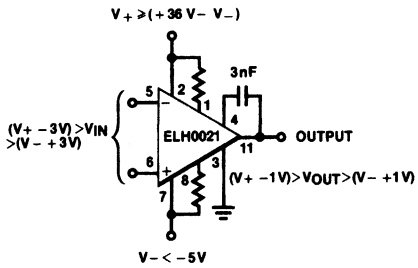
0021-9

Negative

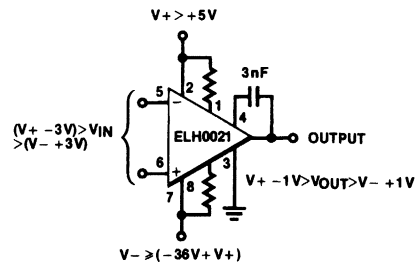


0021-10

Operation from Non-Symmetrical Supplies



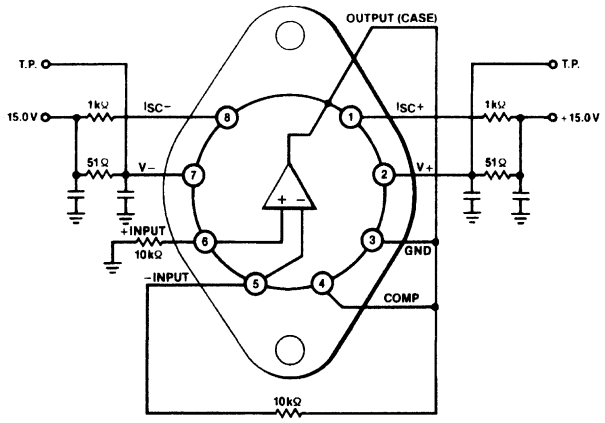
0021-11



0021-12

ELH0021/ELH0021C
1 Amp Power Operational Amplifier

Burn-In Circuit



0021-13

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0041/ELH0041C
0.1 Amp Power Operational Amplifier

Features

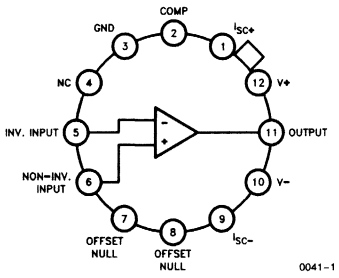
- High output current—200 mA
- Excellent open-loop gain—106 dB
- Low offset voltage—1 mV
- Wide full power bandwidth—20 kHz
- High slew rate—3 V/μs
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0041CG	−25°C to +85°C	TO-8	MDP002
ELH0041G	−55°C to +125°C	TO-8	MDP002
ELH0041G/883B	−55°C to +125°C	TO-8	MDP002

8508701ZX is the DESC version of this device.

Connection Diagram



Top View

General Description

The ELH0041/ELH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC op amps; the ELH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. These devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

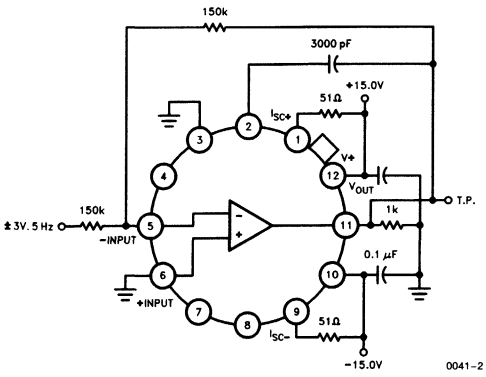
For applications requiring output currents in excess of 1A, see the ELH0021 data sheet.

The excellent input characteristics and high output capability of the ELH0041 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

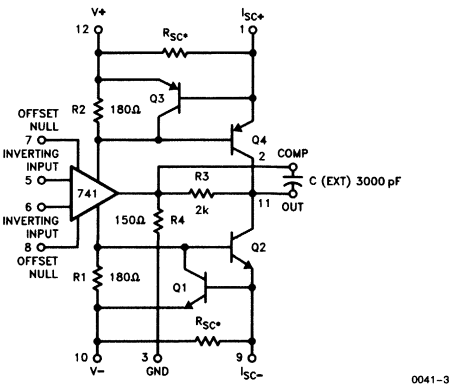
The ELH0041 is particularly suited for applications such as torque drivers for inertial guidance systems, diddle yoke drivers for alphanumeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Burn-In Circuit



Equivalent Schematic



ELH0041/ELH0041C
0.1 Amp Power Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage (Note 1)	±15V		ELH0041	−55°C to +125°C
P_D	Power Dissipation (See curves)			ELH0041C	−25°C to +85°C
	Differential Input Voltage	±30V	T_{ST}	Storage Temperature	−65°C to +150°C
	Peak Output Current (Note 2)	0.5A		Lead Temperature	
	Output Short Circuit			(Soldering, 10 seconds)	300°C
	Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, C_C = 3000 pF

Parameter	Description	Test Conditions	ELH0041				ELH0041C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$, T_A = 25°C (Note 4)		1	3	I		3	6	I	mV
		$R_S \le 100\Omega$ (Note 4)			5	I			7.5	III	mV
$\Delta V_{OS}/\Delta T$	Voltage Drift with Temperature	$R_S \le 100\Omega$		3		V		5		V	µV/°C
	Offset Voltage Drift with Time	T_A = 25°C		5		V		5		V	$\mu V/\sqrt{wk}$
$\Delta V_{OS}/\Delta P$	Offset Voltage Change with Output Power			15		V		15		V	µV/W
	Offset Voltage Adjustment Range			20		V		20		V	mV
I_{OS}	Input Offset Current	T_A = 25°C (Note 4)		30	100	I		50	200	I	nA
		(Note 4)			300	I			500	III	nA
	Offset Current Drift with Temperature			0.1	1	IV		0.2	1	IV	nA/°C
	Offset Current Drift with Time	T_A = 25°C		2		V		2		V	$nA/\sqrt{wk}$
I_B	Input Bias Current	T_A = 25°C (Note 4)		100	300	I		200	500	I	nA
		(Note 4)			1	I			1	III	µA
R_{IN}	Input Resistance	T_A = 25°C	0.3	1		I	0.3	1		I	MΩ

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$, $C_C = 3000\ pF$ — Contd.

Parameter	Description	Test Conditions	ELH0041				ELH0041C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio	$R_S \le 100\Omega$, $V_{CM} = \pm 10V$	70	90		I	70	90		II	dB
V_{INCM}	Input Voltage Range		±12			IV	±12			IV	V
PSRR	Power Supply Rejection Ratio	$R_S \le 100\Omega$, $V_S = \pm 5V$ to $\pm 15V$	80	96		I	70	90		II	dB
A_V	Voltage Gain (Note 5)	$V_O = \pm 10V$, $R_L = 1\ k\Omega$, $T_A = 25°C$	100	200		I	100	200		I	V/mV
		$V_O = \pm 10V$, $R_L = 100\Omega$	25			I	20			II	V/mV
V_O	Output Voltage Swing	$R_L = 100\Omega$	±13	14		I	±13	±14		II	V
I_{SC}	Output Short Circuit Current	$T_A = 25°C$, $R_{SC} = 3.3\Omega$		200	300	I		200	300	I	mA
I_S	Supply Current	$V_{OUT} = 0V$		2.5	3.5	I		3	4	II	mA
P_C	Power Consumption	$V_{OUT} = 0V$		75	105	I		90	120	II	mW

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G with $R_{SC} = 0\Omega$.

Note 3: Rating applies as long as package power rating is not exceeded.

Note 4: Specifications apply for $\pm 5V \le V_S \le 18V$.

Note 5: The ELH0041, like all Class B amplifiers, has a "dead band" when V_{OUT} is near zero volts. Typical values for the "dead band" are in the 50 μV to 200 μV range. Open-loop gain is measured at V_{OUT} from ±0.5 V_{DC} to ±10 V_{DC} which is out of the range of the "dead band".

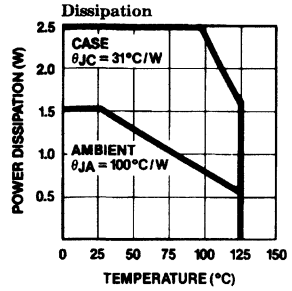
AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\ pF$

Parameter	Description	Test Conditions	ELH0041				ELH0041C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	$A_V = 1$, $R_L = 100\Omega$	1.5	3		I	1	3		I	V/μs
BW	Bandwidth	$R_L = 100\Omega$		20		V		20		V	kHz
t_r, t_f	Small Signal Rise or Fall Time			0.3	1	I		0.3	1.5	I	μs
	Small Signal Overshoot			5	20	I		10	30	I	%
t_S	Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = 1$		4		V		4		V	μs
	Overload Recovery Time			3		V		3		V	μs
HD	Harmonic Distortion	$f = 1\ kHz$, $P_O = 0.5W$		0.2		V		0.2		V	%
E_N	Input Noise Voltage	$R_S = 50\Omega$, BW = 10 Hz to 10 kHz		5		V		5		V	μV_{rms}
I_N	Input Noise Current	BW = 10 Hz to 10 kHz		0.05		V		0.05		V	nA_{rms}
C_{IN}	Input Capacitance			3		V		3		V	pF

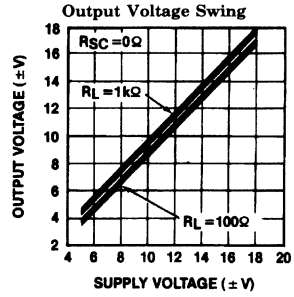
ELH0041/ELH0041C
0.1 Amp Power Operational Amplifier

Typical Performance Curves

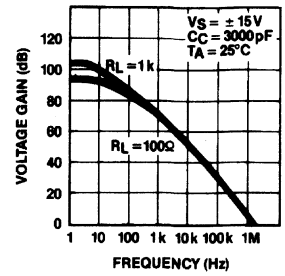
Maximum Power Dissipation



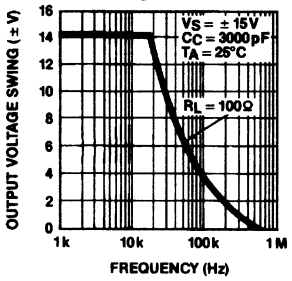
Output Voltage Swing



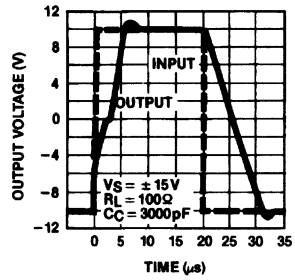
Open-Loop Frequency Response



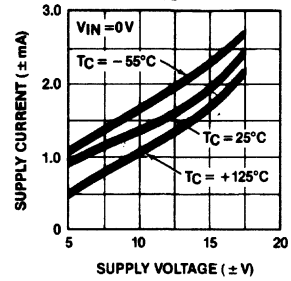
Large Signal Pulse Response



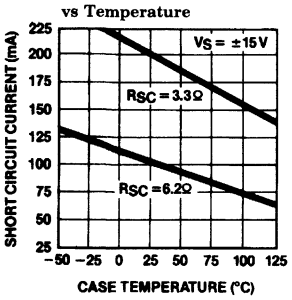
Voltage Follower Pulse Response



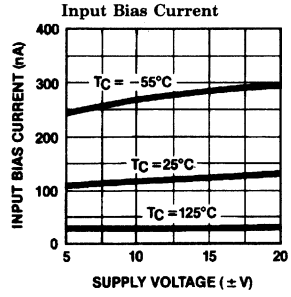
No Load Supply Current



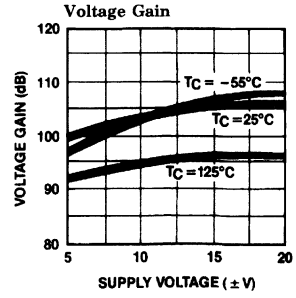
Short Circuit Current vs Temperature



Input Bias Current



Voltage Gain

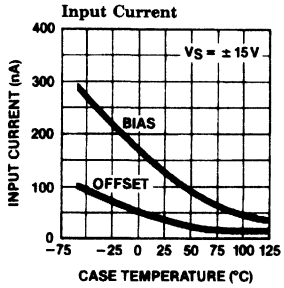


0041-4

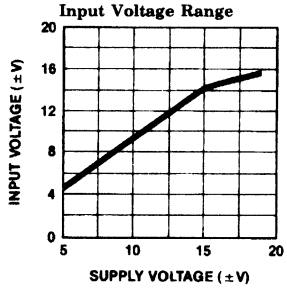
ELH0041/ELH0041C
0.1 Amp Power Operational Amplifier

Typical Performance Curves — Contd.

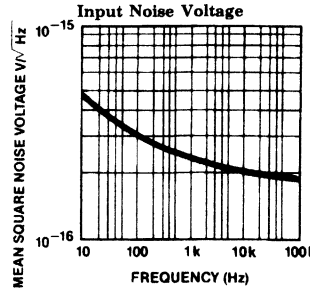
Input Current



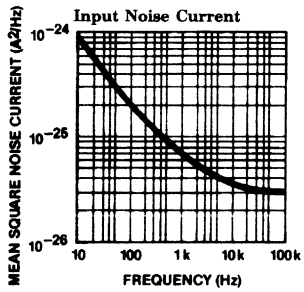
Input Voltage Range



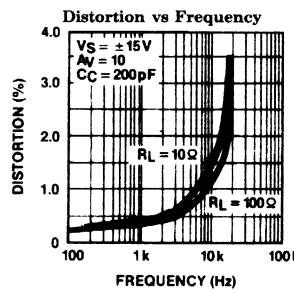
Input Noise Voltage



Input Noise Current



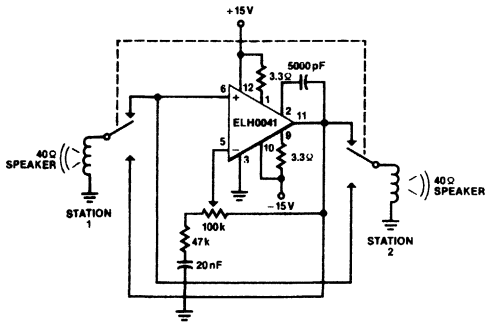
Distortion vs Frequency



0041-5

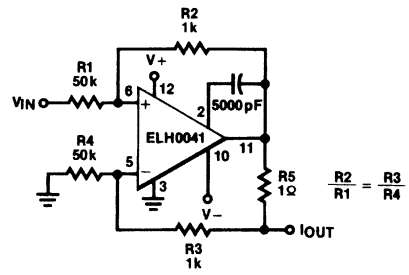
Typical Applications

Two Way Intercom



0041-6

Programmable High Current Source/Sink



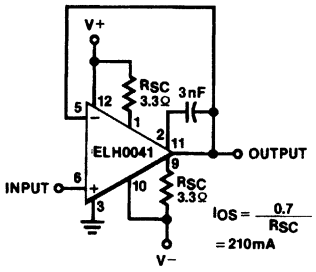
0041-7

$$I_{OUT} = \frac{V_{IN}}{R5}\left(\frac{R2}{R1}\right) + \frac{V_{OUT}}{R1 + R2} = 20\ mA/V_{IN}$$

ELH0041/ELH0041C
0.1 Amp Power Operational Amplifier

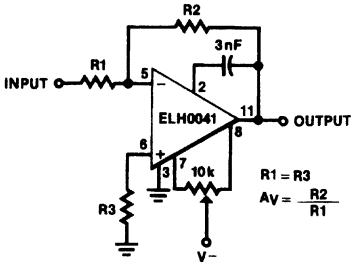
Typical Applications — Contd.

Unity Gain with Short Circuit Limiting



0041-8

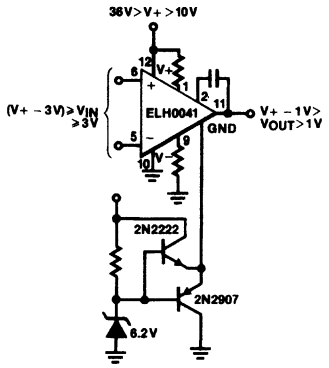
Offset Voltage Null Circuit



0041-9

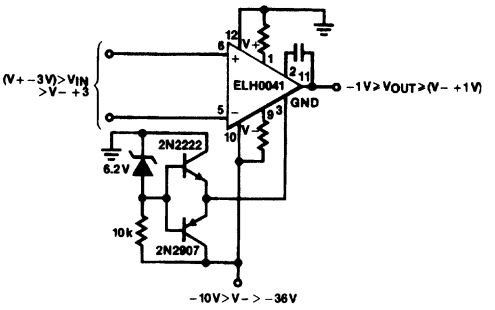
Operation from Single Supplies

Positive



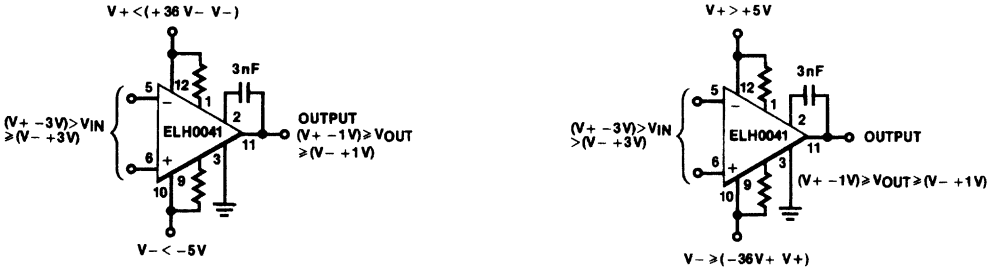
0041-10

Negative



0041-11

Operation from Non-Symmetrical Supplies



0041-12

0041-13

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0101/ELH0101A
Power Operational Amplifier

Features

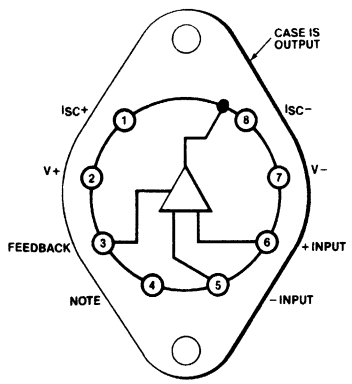
- 5A peak, 2A continuous output current
- 10 V/μs slew rate
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Package	Outline #
ELH0101ACK	−25°C to +85°C	TO-3	MDP0003
ELH0101AK	−55°C to +125°C	TO-3	MDP0003
ELH0101AK/883B	−55°C to +125°C	TO-3	MDP0003
ELH0101CK	−25°C to +85°C	TO-3	MDP0003
ELH0101K	−55°C to +125°C	TO-3	MDP0003
ELH0101K/883B	−55°C to +125°C	TO-3	MDP0003

8508901YX and 8508902YX are the DESC versions of this device.

Connection Diagram



0101-1

Top View

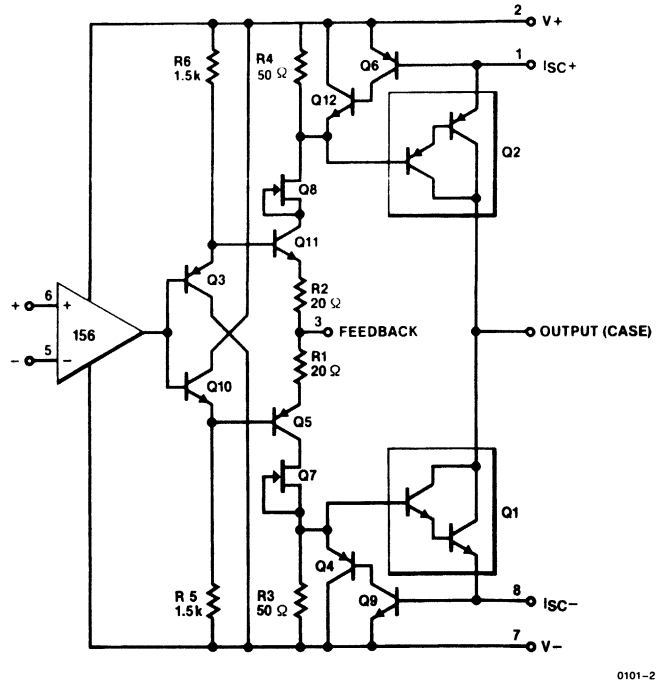
Note: Electrically connected internally. No connection should be made to pin.

General Description

The ELH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the ELH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drivers, programmable power supplies, and disk head positioner amplifiers.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Equivalent Schematic



0101-2

ELH0101/ELH0101A
Power Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage		V_{IN}	Input Voltage Range	
	ELH0101C, ELH0101AC	±18V		ELH0101C, ELH0101AC	±15V but < $\pm V_S$
	ELH0101, ELH0101A	±22V		ELH0101, ELH0101A	±20V but < $\pm V_S$
P_D	Power Dissipation at T_A = 25°C	5W		Peak Output Current (50 ms pulse)	5A
	Derate linearly at 25°C/W to zero at 150°C			Output Short Circuit Duration (within rated power dissipation, R_{SC} = 0.35Ω, T_A = 25°C)	Continuous
P_D	Power Dissipation at T_C = 25°C	62W	T_A	Operating Temperature Range:	
	Derate linearly at 2°C/W to zero at 150°C			ELH0101C, ELH0101AC	−25°C to +85°C
	Differential Input Voltage			ELH0101, ELH0101A	−55°C to +125°C
	ELH0101C, ELH0101AC	±30V but < $\pm V_S$	T_J	Maximum Junction Temperature	150°C
	ELH0101, ELH0101A	±40V but < $\pm V_S$	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (Note 1) V_S = ±15V, T_A = 25°C, V_{CM} = 0V

Parameter	Description	Test Conditions	ELH0101A, AC				ELH0101, C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage			1	3	I		5	10	I	mV
		$T_{MIN} \le T_A \le T_{MAX}$, ELH0101, A			7	I			15	I	mV
		$T_{MIN} \le T_A \le T_{MAX}$, ELH0101C, AC			7	III			15	III	mV
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with Dissipated Power	(Note 2)		150		V		300		V	µV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with Temperature			10		V		10		V	µV/°C
I_B	Input Bias Current				300	I			1000	I	pA
		$T_A \le T_{MAX}$, ELH0101C, AC			60	III			60	III	nA
		$T_A \le T_{MAX}$, ELH0101, A			300	I			1000	I	nA

DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ — Contd.

Parameter	Description	Test Conditions	ELH0101A, AC				ELH0101, C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
I_{OS}	Input Offset Current				75	I			250	I	pA
		$T_A \leq T_{MAX}$, ELH0101C, AC			15	III			15	III	nA
		$T_A \leq T_{MAX}$, ELH0101, A			75	I			250	I	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10\Omega$	50	200		I	50	200		I	V/mV
V_O	Output Voltage Swing	$R_{SC} = 0\Omega$, $A_V = 1$, $R_L = 100\Omega$ (Note 3)	±11.7	±12.5		I	±11.7	±12.5		I	V
		$R_{SC} = 0\Omega$, $A_V = 1$, $R_L = 10\Omega$ (Note 3)	±11	±11.6		I	±11	±11.6		I	V
		$R_{SC} = 0\Omega$, $A_V = 1$, $R_L = 5\Omega$ (Note 3)	±10.5	±11		I	±10.5	±11		I	V
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	85	100		I	85	100		I	dB
PSRR	Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq \pm 15V$	85	100		I	85	100		I	dB
		$+5V \leq V_S(+) \leq +15V$, $V_S(-) = -15V$	80	110		I	80	110		I	dB
		$-5V \geq V_S(-) \geq -15V$, $V_S(+) = +15V$	80	95		I	80	95		I	dB
I_S	Supply Current			28	35	I		28	35	I	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = T_C = T_J = 25°C$

Parameter	Description	Test Conditions	ELH0101A, AC				ELH0101, C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
e_n	Equivalent Input Noise Voltage	f = 1 kHz		25		V		25		V	$nV/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 1 MHz		3		V		3		V	pF
PBW	Power Bandwidth, −3 dB	$R_L = 10\Omega$, $A_V = 1$		300		V		300		V	kHz
SR	Slew Rate	$R_L = 10\Omega$, $A_V = 1$	7.5	10		I		10		V	V/μs
t_r, t_f	Small Signal Rise or Fall Time	$R_L = 10\Omega$, $A_V = 1$		200		V		200		V	ns
	Small Signal Overshoot	$R_L = 10\Omega$, $A_V = 1$		10		V		10		V	%

ELH0101/ELH0101A
Power Operational Amplifier

AC Electrical Characteristics $V_S = \pm 15V, T_A = T_C = T_J = 25°C$

Parameter	Description	Test Conditions	ELH0101A, AC				ELH0101, C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
GBW	Gain-Bandwidth Product	$R_L = \infty, A_V = 1$	4	5		I		5		V	MHz
t_S	Large Signal Settling Time (0.01%)	$R_L = \infty, A_V = 1$		2		V		2		V	μs
THD	Total Harmonic Distortion	$f = 1$ kHz, $P_O = 0.5$W, $R_L = 10\Omega$		0.008		V		0.008		V	%

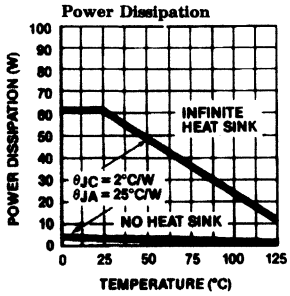
Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heatsinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to I_B vs. temperature and power dissipation graphs for expected values.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heatsink.

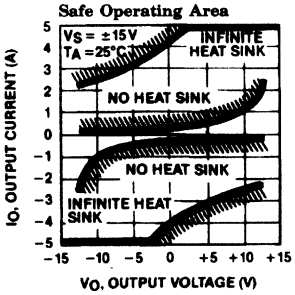
Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation. R_{SC} is the current sense resistor.

Typical Performance Curves

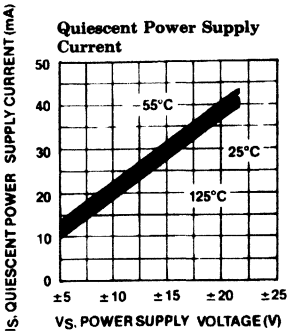
Power Dissipation



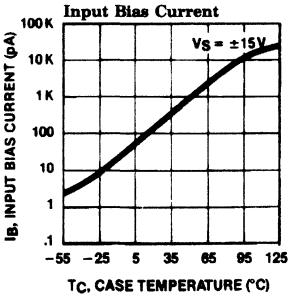
Safe Operating Area



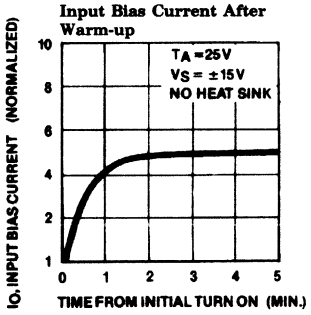
Quiescent Power Supply Current



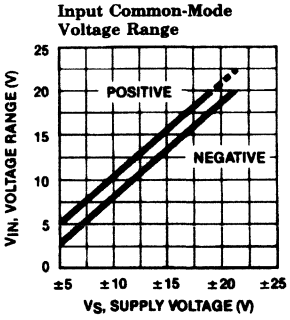
Input Bias Current



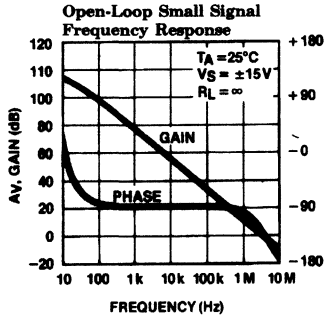
Input Bias Current After Warm-up



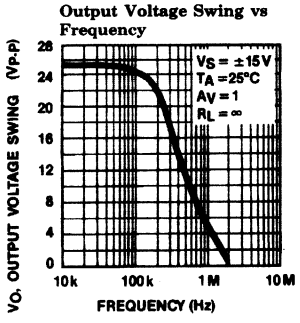
Input Common-Mode Voltage Range



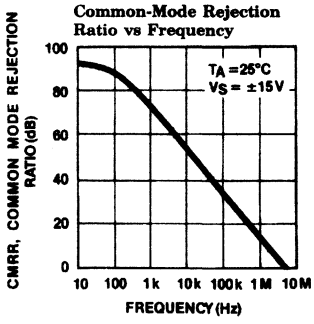
Open-Loop Small Signal Frequency Response



Output Voltage Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency

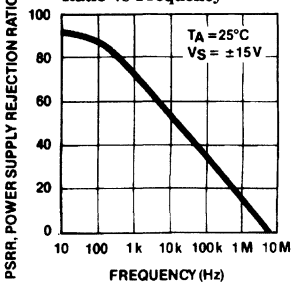


0101-3

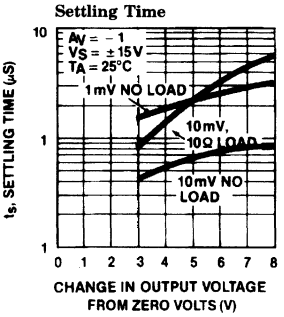
ELH0101/ELH0101A
Power Operational Amplifier

Typical Performance Curves — Contd.

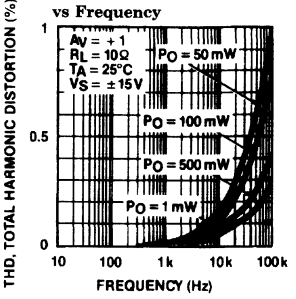
Power Supply Rejection Ratio vs Frequency



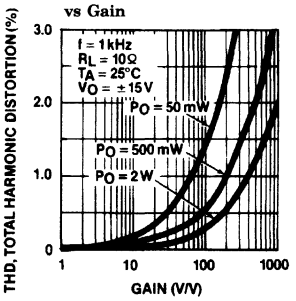
Settling Time



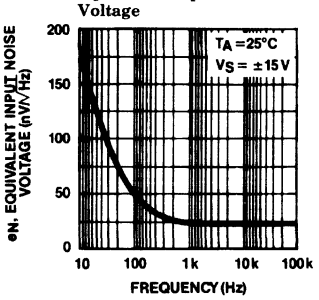
Total Harmonic Distortion vs Frequency



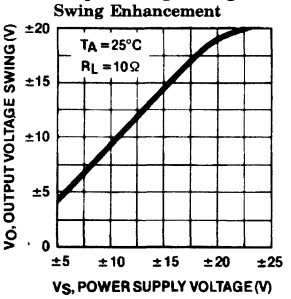
Total Harmonic Distortion vs Gain



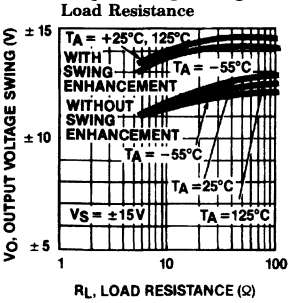
Equivalent Input Noise Voltage



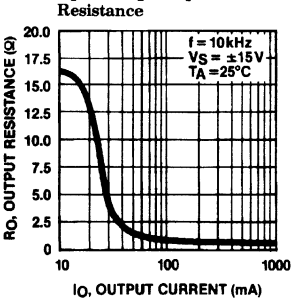
Output Voltage Swing with Swing Enhancement



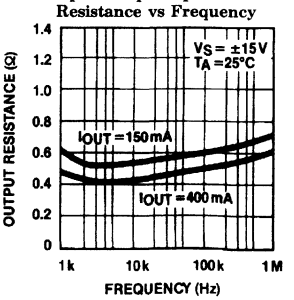
Output Voltage Swing vs Load Resistance



Open-Loop Output Resistance



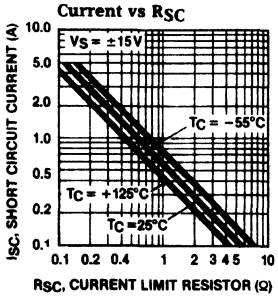
Open-Loop Output Resistance vs Frequency



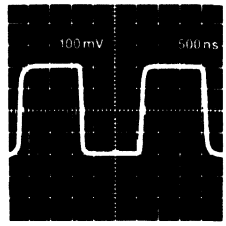
0101-4

Typical Performance Curves — Contd.

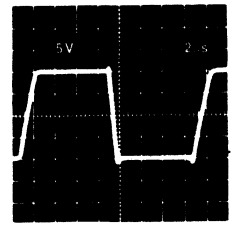
Short Circuit Current vs R_{SC}



Small Signal Pulse Response



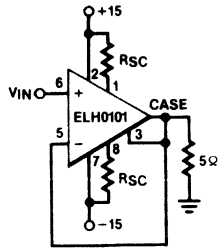
Large Signal Pulse Response



0101-5

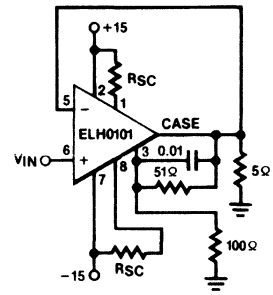
Typical Applications

High Power Voltage Follower



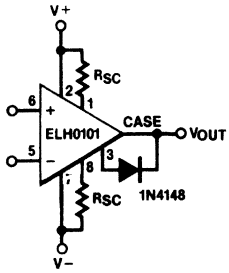
0101-6

High Power Voltage Follower with Swing Enhancement



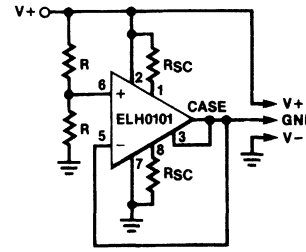
0101-7

Restricting Outputs to Positive Voltage Only



0101-8

Generating a Split Supply from a Single Voltage Supply

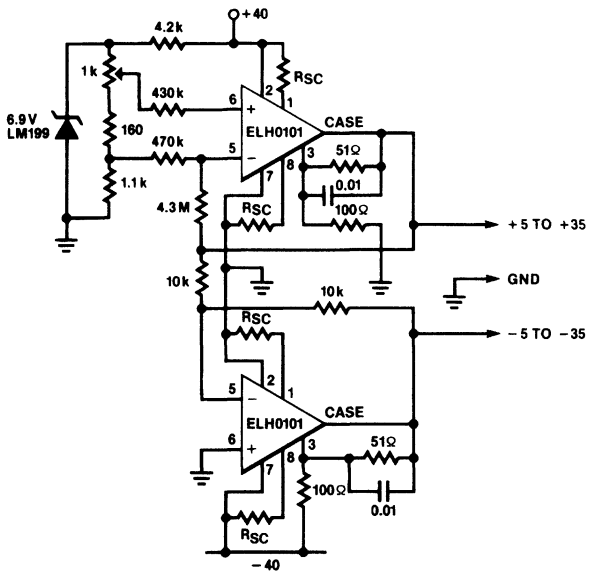


0101-9

ELH0101/ELH0101A
Power Operational Amplifier

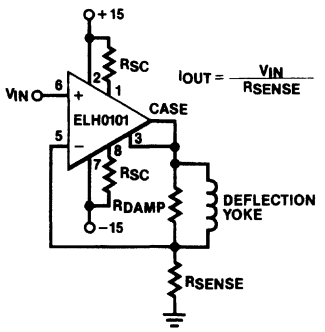
Typical Applications — Contd.

±5 to ±35 Power Source or Sink



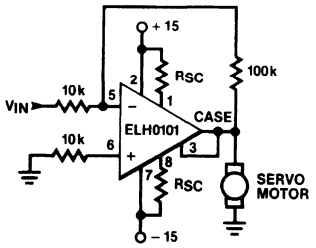
0101-10

CRT Deflection Yoke Driver



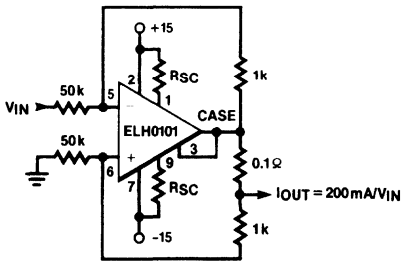
0101-11

DC Servo Amplifier



0101-12

High Current Source/Sink



0101-13

Applications Information

Input Voltages

The ELH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however; if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the ELH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply bus.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the ELH0101.

Layout Considerations

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

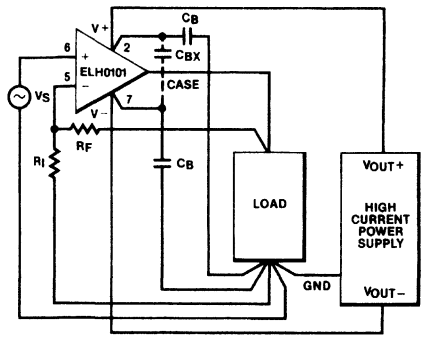
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the ELH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

ELH0101/ELH0101A
Power Operational Amplifier

Applications Information — Contd.

Every attempt should be made to achieve a single point ground system as shown in the figure below.



0101-14

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the ELH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit will be approximately 0.3%.

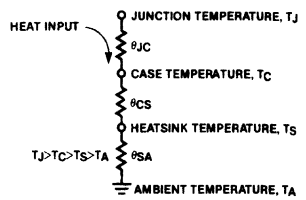
Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} °C/W \qquad (1)$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heatsink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures, T_J, T_C, and T_S, (no temperature distribution in junction, case, or heatsink). Nevertheless, this is a reasonable approximation of actual performance.



0101-15

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

The junction-to-case thermal resistance, θ_{JC}, specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heatsink thermal resistance, θ_{CS}, depends on the mounting of the device to the heatsink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5°C/W to 0.7°C/W, and 0.3°C/W to 0.5°C/W using silicone grease.

The heatsink to ambient thermal resistance, θ_{SA}, depends on the quality of the heatsink and the ambient conditions.

Application Information — Contd.

Cooling is normally required to maintain the worst case operating junction temperature, T_J, of the device below the specified maximum value, $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting equation (1), we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} °C/W$$

$$T_J = T_A + P_D\theta_{JA} °C$$

Where: $P_D = (V_S - V_{OUT})\, I_{OUT} + |V\pm (V-)|I_Q$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and
V_S = Supply Voltage

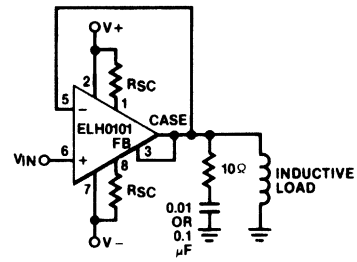
θ_{JC} for the ELH0101 is typically 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

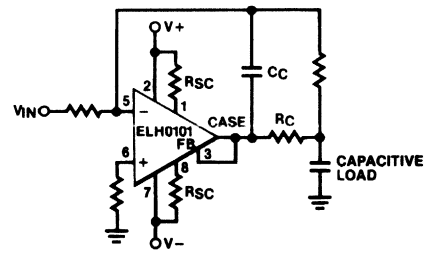
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Some inductive loads may cause output stage oscillation. A 0.01 μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.



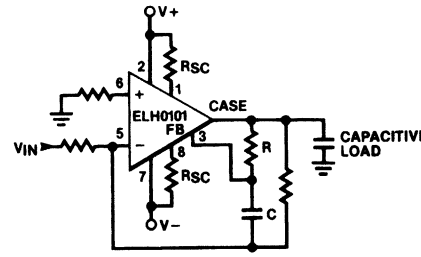
0101-16

Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley.)



0101-17

A similar but alternative technique may be used for the ELH0101.



0101-18

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec Disk Drive Servo Amplifiers

Elantec Part Number	Description	Continuous Output Current Drive	Voltage Swing Across Load	Power Supply Voltage Range	Operating Mode	Packages
ELH0021	Hybrid Power Operational Amplifier	1.1A Min	±13.5V Min (+15V Supply)	±5V to ±18V	Linear	8-Pin TO-3
ELH0041	Hybrid Power Operational Amplifier	200 mA Typ	±13V Min (+15V Supply)	±5V to ±18V	Linear	12-Pin TO-8
ELH0101	Hybrid Power Operational Amplifier	2.1A Min	±11.7V Min (+15V Supply)	±5V to ±22V	Linear	8-Pin TO-3
EL2036	Monolithic Voice Coil Driver with Auto Head Park—3½" Drives	25 mA Min (Drive for External Transistors)	±10V Min (+12V Supply)	−0.3V to +18V	Linear Class A, B	20-Pin P-DIP 20-Pin SO
EL2037	Monolithic Voice Coil Driver with Auto Head Park—5¼" Drives	25 mA Min (Drive for External Transistors)	±10V Min (+12V Supply)	−0.3V to +18V	Linear Class A, B	20-Pin P-DIP 20-Pin SO

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2036C/EL2037C
Servo Motor Drivers

Features

- No crossover distortion
- Low output offset current
- Maximum output swing
- Short circuit protected
- Programmable park voltage
- Programmable transconductance
- Programmable bandwidth
- Chip enable function
- Drive low cost bipolar transistors
- Single sense resistor
- Minimum external components
- Small surface mount package

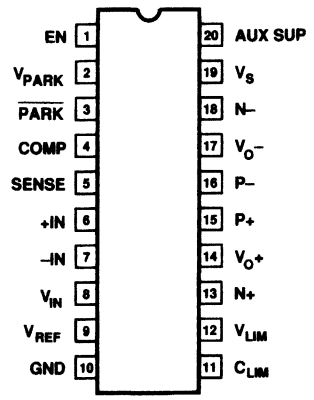
Applications

- Voice coil motor servo systems
- Winchester disk drives
- Optical disk drives
- Super floppy drives
- DC motor control

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2036CM	−25°C to +85°C	SOIC	MDP0027
EL2036CN	−25°C to +85°C	PDIP	MDP0031
EL2037CM	−25°C to +85°C	SOIC	MDP0027
EL2037CN	−25°C to +85°C	PDIP	MDP0008

Connection Diagram



2036-1

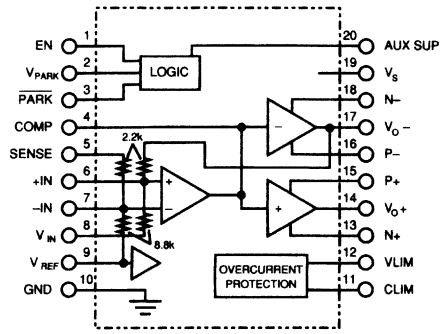
General Description

The EL2036C and EL2037C are servo motor driver circuits designed to drive voice coil motors in disk drive applications. These second generation circuits contain more features, have improved accuracy, and are lower in cost compared to earlier generation circuits. The EL2036C/EL2037C drive an H bridge consisting of four low-cost external bipolar power transistors for maximum output swing. Crossover distortion is eliminated by Class AB biasing of the output devices with a unique patent pending temperature-stable circuit that never needs adjustment. The EL2036C/EL2037C protect the output transistors from short circuits by powering down for a programmed delay time when a fault occurs. When the fault is removed, the circuit returns to normal mode. This type of short circuit protection eliminates excessive power dissipation during faults and prevents overheating.

System accuracy is improved by using one external current sense resistor in series with the motor. Compared to conventional grounded resistor circuits, the EL2036C/EL2037C have inherent positive to negative gain matching and no gain error due to transistor alpha. All of the critical bias voltages use the same V_{REF} voltage. This reduces the output offset current to less than 5 mA.

In addition to an enable logic input, a "park" logic input has been provided which programs a voltage across the motor to park the head when power is removed. The power for this function comes from a separate supply generated by the back EMF of the spindle motor used as a generator. The EL2036C requires back EMF of 2.5V minimum, while the EL2037C requires back EMF of 3.5V minimum.

Block Diagram



2036-2

EL2036C/EL2037C
Servo Motor Drivers

Absolute Maximum Ratings

V_S	Supply Voltage, Pin 19	−0.3V to +18V
V_{AUX}	Auxiliary Supply Voltage, Pin 20	V_S −1V to +18V
V_{LIM}	Short Circuit Limit Sense Voltage	V_S −0.3V to +18V
V_{IN}	Logic Inputs, Pins 1 and 3	−0.3V to +7V
	Signal Inputs, Pins 8 and 9	−0.3V to +7V
I_{IN}	Input Current, Pins 1, 3, 8, and 9	10 mA
T_J	Junction Temperature	150°C
T_A	Operating Temperature Range	−25°C to +85°C
	Lead Temperature	
	DIP Package	300°C
	SOL Package	
	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
T_{ST}	Storage Temperature	−65°C to +150°C
P_D	Power Dissipation, T_A = 25°C	
	DIP Package	1.80W
	SOL Package	1.50W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = 12V$, $V_{REF} = 5V$, $R_s = 0.25\Omega$, Load = 10Ω. See test circuits

Parameter	Description	Min	Typ	Max	Test Level	Units
Enabled Mode, Pin 1 = H. Pin 3 = H. (Note 1)						
I_{OS}	Output Offset Current	−5	0.6	5	I	mA
G_{M1}	Transconductance, I_{OUT} = ±100 mA	0.95	1	1.05	I	A/V
G_{M2}	Transconductance, I_{OUT} = ±1A	0.93	1	1.07	I	A/V
I_{ST}	Quiescient Supply Current, Total		20		V	mA
I_{Q1}	Quiescient Supply Current, Pin 12 + 19	6	10	14	I	mA
I_{Q2}	Auxiliary Supply Quiescient Current, Pin 20	1	5	7	I	mA
I_{QE}	External Transistor Quiescient Current	2	8	12	I	mA
I_{DN}	NPN Drive Current, Pin 13 or 18	25	35		I	mA
I_{DP}	PNP Drive Current, Pin 15 or 16	25	35		I	mA
I_{IB}	Input Bias Current. $V_{IN} = V_{REF}$ = 2.5V, 6.5V	−250	50	250	I	µA
I_{IA}	Active Input Current. V_{IN} = 0.5V, V_{REF} = 2.5V	−1.5	−1.1		I	mA
I_{IA}	Active Input Current. V_{IN} = 4.5V, V_{REF} = 2.5V		0.4	0.7	I	mA
I_{RB}	Reference Bias Current. $V_{IN} = V_{REF}$ = 2.5V, 6.5V	−250	50	250	I	µA
I_{RA}	Active Reference Current. V_{IN} = 0.5V, V_{REF} = 2.5V	−1.5	−0.9		I	mA
I_{RA}	Active Reference Current. V_{IN} = 4.5V, V_{REF} = 2.5V		0.2	0.5	I	mA
V_S	Supply Voltage Range, Pin 19	11	12	13	IV	V
VRR	Reference Voltage Range, Pin 9	2.5		6.5	I	V
RRR	Reference Voltage Rejection, 2.5V to 6.5V		0.3	1	I	mA/V
PSR	Power Supply Rejection, 11V to 13V		0.3	1	I	mA/V
THD	Total Harmonic Distortion, V_{IN} = 20 mV_{PP}, 1 kHz		0.5	1	I	%

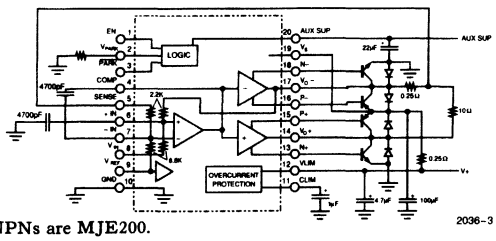
Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = 12V$, $V_{REF} = 5V$, $R_s = 0.25\Omega$, Load = 10Ω. See test circuits — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
Park Mode. Pin 1 = H. Pin 3 = L. Aux Supply (Pin 20) = 6V (Note 1) R_{PARK} = 1.5k, EL2036C, R_{PARK} = 3k, EL2037C						
V_{P1}	V_{OUT} ($V_{O+} - V_{O-}$)	−0.3	−0.45	−0.55	I	V
V_{AR}	Aux Supply Range, EL2036C (−0.25V ≤ V_{OUT} ≤ −0.65V)	2.5	6	12	I	V
V_{AR}	Aux Supply Range, EL2037C (−0.25V ≤ V_{OUT} ≤ −0.65V)	3.5	6	12	I	V
I_{PD}	NPN Drive. Pin 13	2	3		I	mA
I_{AUX}	Short Circuit Maximum Current (Pin 17 = 0V)		250		V	mA
Disabled Mode. Pin 1 = L. Pin 3 = H. (Note 1)						
I_{OD}	Output Current	−200	10	200	I	µA
R_{OD}	Output Resistance. I_{OUT} ±1 mA	1	3		I	kΩ
I_{SD}	Total Supply Current, Pin 12, 19, and 20 + Transistors		10	14	I	mA
Short Circuit Protection						
V_{TR}	Trip Voltage. Pin 12–Pin 19	340	425	510	I	mV
I_C	Capacitor Charging Current	20	35	50	I	µA
I_D	Capacitor Discharge Current	1	3	10	I	mA
V_C	Capacitor Quiescent Voltage	8	9	10	I	V
Logic Inputs						
V_{IL}	Low Level Input Voltage for a Valid Low			0.8	I	V
I_{IL}	Low Level Input Current, Logic = 0V	−10	0	10	I	µA
V_{IH}	High Level Input Voltage for a Valid High	2			I	V
I_{IH}	High Level Input Current, Logic = 5V	−100	10	100	I	µA
Individual Amplifiers						
A_V	Power Amplifier Voltage Gain	9.5	10.7	12	I	V/V

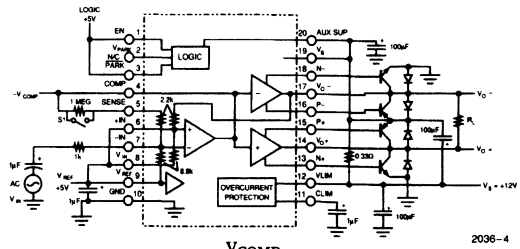
Note 1: Logic Level L = 0.8V, Logic Level H = 2.0V

DC and Closed Loop AC Test Circuit



NPNs are MJE200.
PNPs are MJE210.
Diodes are 1 Amp IN4000.

Open Loop AC Test Circuit



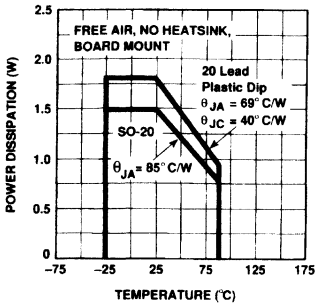
Op Amp Gain—S1 Open, $A_V = \frac{V_{COMP}}{V_{IN}}$

Power Amp Gain—S1 Closed, $A_V = \frac{(V_{O+})-(V_{O-})}{V_{COMP}}$

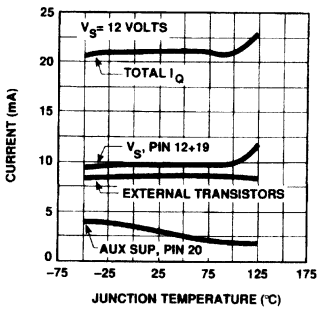
EL2036C/EL2037C
Servo Motor Drivers

Typical Performance Curves

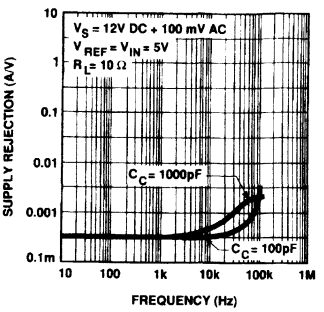
Maximum Power Dissipation vs Ambient Temperature



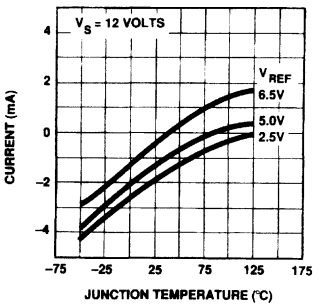
Quiescent Current vs Temperature



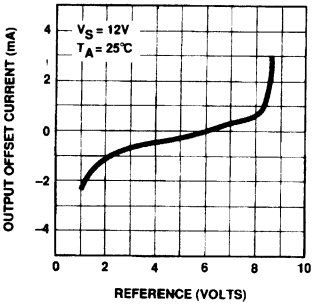
Supply Rejection vs Frequency



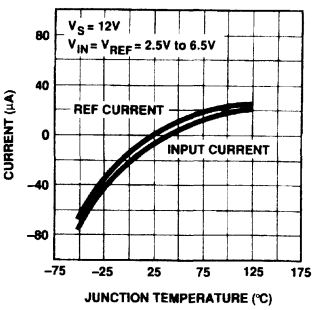
Output Offset Current vs Temperature



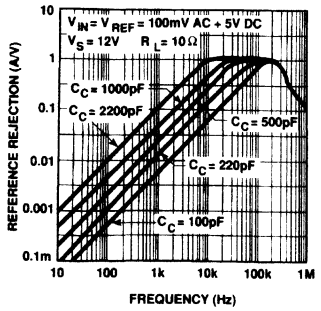
Output Offset Current vs Reference Voltage— Typical Unit



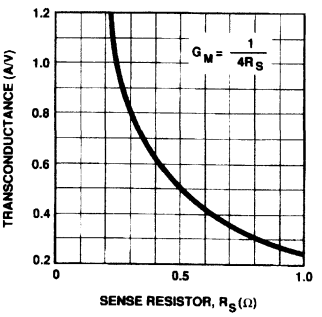
Reference and Input Bias Current vs Temperature



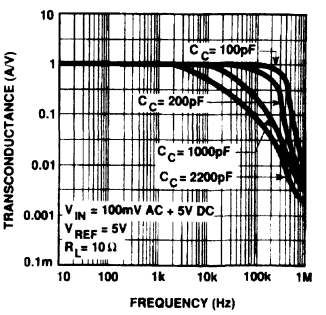
Reference Voltage Rejection vs Frequency



Transconductance vs Sense Resistor



Transconductance vs Frequency



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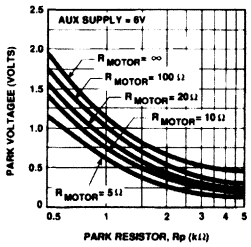
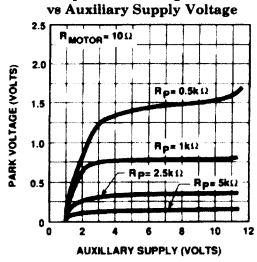
Typical Performance Curves — Contd.

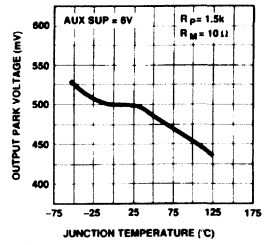
EL2036C
Output Park Voltage
vs Park Resistor



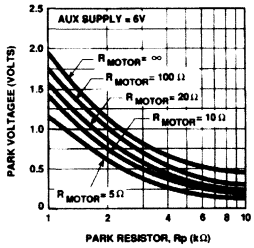
EL2036C
Output Park Voltage
vs Auxiliary Supply Voltage



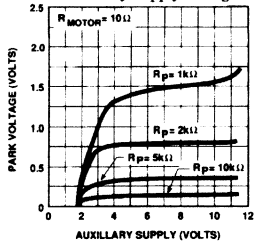
EL2036C
Output Park Voltage
vs Temperature



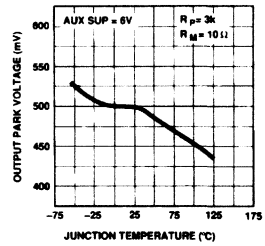
EL2037C
Output Park Voltage
vs Park Resistor



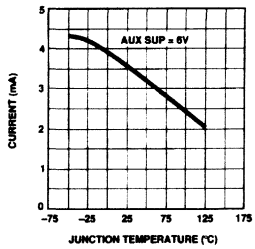
EL2037C
Output Park Voltage
vs Auxiliary Supply Voltage



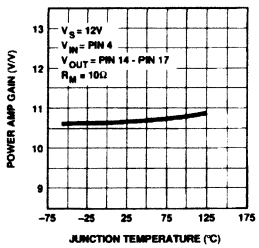
EL2037C
Output Park Voltage
vs Temperature



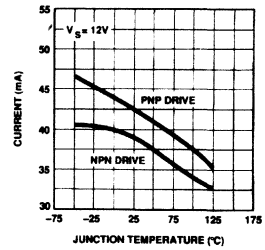
NPN Base Drive During
Park vs Temperature



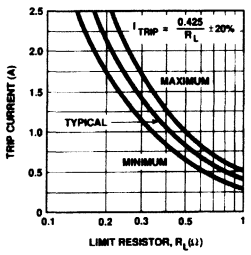
Power Amplifier Gain
vs Temperature



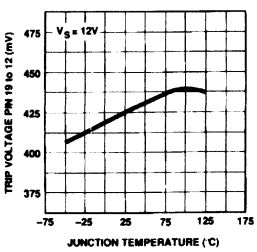
Power Amplifier Drive
Current vs Temperature



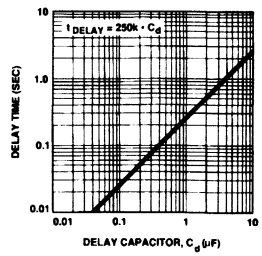
Protection Circuit Trip Current
vs Limit Sense Resistor



Protection Circuit Trip
Voltage vs Temperature



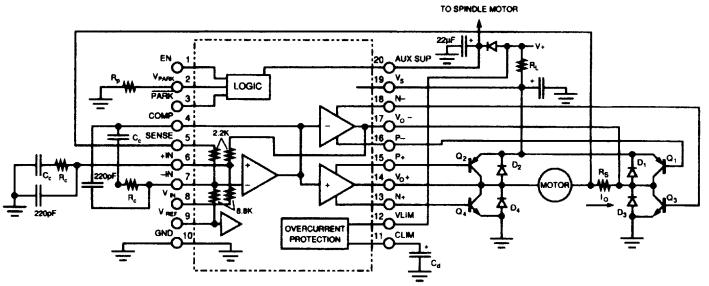
Protection Circuit Delay Time
vs Delay Capacitor



2036-6

EL2036C/EL2037C
Servo Motor Drivers

Typical Application



2036-7

External Components

Parameter	Description	Min	Typ	Max	Units	Typical ± % Tolerance
R_P	Sets the Motor Voltage During PARK Mode, EL2036C	0.5k	1.5k	Open	Ω	5
R_P	Sets the Motor Voltage During PARK Mode, EL2037C	1k	3k	Open	Ω	5
R_s	Current Sense Resistor	0.1	0.25	1	Ω	2
C_c	Loop Compensation. Sets dominant pole	100	2000	0.1 μF	pF	5
R_c	Loop Compensation. Makes a Zero, Equal to Motor Pole	0	10	200	kΩ	5
R_1	Short Circuit Sense Resistor	0	0.33	3	Ω	5
C_d	Short Circuit Delay Capacitor	0.05	1	100	μF	10
D1–4	Catch diodes, 1 amp	1N4000				
Q1, 2	PNP Power Transistors. Min H_{FE} = 40	MJE210 or D45H11				
Q3, 4	NPN Power Transistors. Min H_{FE} = 40	MJE200 or D44H11				
	$R_P \approx$ 0.7k/Park motor voltage (see the curves) for EL2036C and 1.4k/Park motor voltage for EL2037C					
	R_1 = 0.425/Trip current					
	C_d = Delay/250k					
	R_s = 1/(4*DC transimpedance)					

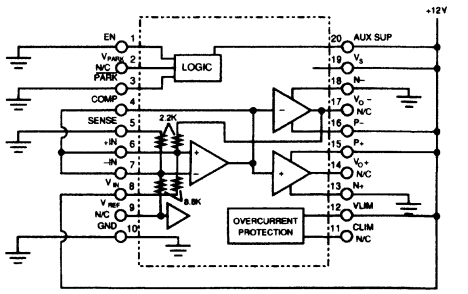
Truth Table

Enable (Pin 1)	Park (Pin 3)	V12 to V19	Output
>2.0V	>2.0V	<0.34V	Normal Operation
<0.8V	>2.0V	<0.34V	Disabled
X	<0.8V	<0.34V	Parking Mode
X	X	>0.52V	Disabled for Delay

$$C_c = \frac{4\,R_s}{800\,(R_m + R_s)\,2\,\text{pBandwidth}}$$

$$R_c = \frac{L_m}{C_c\,(R_m + R_s)}$$

Burn-In Circuit



2036-8

Circuit Description

The EL2036C/EL2037C are transconductance amplifiers especially well-suited to driving voice coil motors in disk drives. The EL2036C/EL2037C consist of five main blocks. These five functions are a low offset voltage operational amplifier, a single-ended input to differential output power amplifier, a short circuit protection circuit, a logic circuit and a park circuit.

The operational amplifier and power amplifier together with four well-matched internal resistors make the basic transconductance amplifier. The short circuit protection circuit senses the total supply current and shuts down the amplifiers if it exceeds a predetermined value. The logic circuit enables the amplifiers and the park circuit.

The Operational Amplifier

The operational amplifier is a low offset design with modest gain and excellent common mode rejection over a wide range that includes ground. This ensures proper operation when the motor voltage exceeds the supply or ground and is clamped by the catch diodes. The operational amplifier is internally compensated for stable operation at all times. The gain bandwidth product is 2 MHz and the phase margin is 60°C at unity gain. The operational amplifier has internal clamps to limit its output swing to about ±2V of the reference voltage. The clamps are not shown in the simplified schematic and their only function is to prevent overcharging of the compensation capacitor during transients. The operational amplifier output is disabled by the logic circuit when either pin 1 or pin 3 is low.

Op Amp Open Loop
Gain and Phase vs Frequency

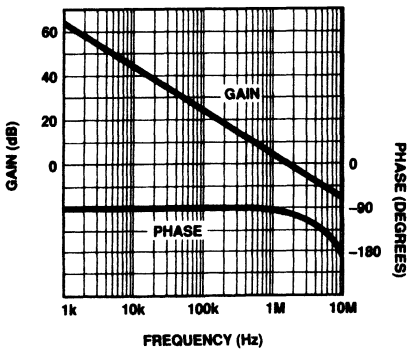


Figure 1

The Power Amplifier

The power amplifiers of the EL2036C/EL2037C are made of two identical stages that take a single-ended input and drive the motor differentially. The reference is buffered and the outputs of both stages are biased from the buffered reference voltage to reduce output offset current. Each stage has feedback for linearity and gain accuracy. One stage operates noninverting and the other inverting, resulting in a total gain of 11. The feedback is more complicated than shown in the simplified schematic, to ensure accurate gain even when one amplifier saturates before the other. The bandwidth of the power amplifier is about 500 kHz as shown below.

External power transistors deliver the power to the motor to optimize the output swing capability and eliminate power dissipation concerns. A unique biasing circuit eliminates low-level crossover distortion by biasing the transistors on at a few mA. The amplifier outputs are disabled when either pin 1 or pin 3 is low.

Power Amplifier Gain and
Phase vs Frequency

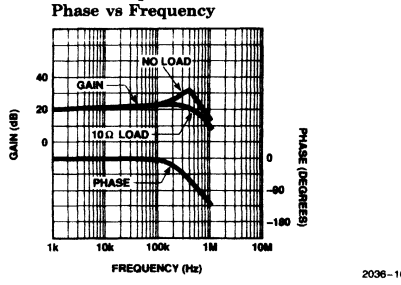


Figure 2

Short Circuit Protection Circuit

The short circuit protection circuit consists of a comparator, a floating reference, a flip flop and a one-shot. An external resistor, R_1 between pins 12 and 19 senses the total supply current the amplifiers pull from the supply. The floating reference subtracts 425 mV from the voltage sensed on pin 12 and the comparator trips when the voltage on pin 19 is at the same level. The net result is that when the drop across R_1 is 425 mV, the comparator trips. The output of the comparator sets a flip flop whose output disables the amplifiers and triggers the one-shot. When the one-shot starts timing, it resets the flip flop and the one-shot keeps the amplifiers off.

EL2036C/EL2037C
Servo Motor Drivers

Circuit Description — Contd.

The one-shot delay is set by an external capacitor, C_d. When the one-shot times out, the amplifiers are enabled again. If there is still a fault condition, the supply current rises until the comparator trips and the cycle repeats. Because the circuit is much faster than the one-shot delay time, the average power dissipation is very low. The circuit responds very quickly, in a few micro-seconds, so any current spike through R_1 will be detected and disable the amplifier for the delay time. The protection circuit will sometimes trip when there is a large, very fast, input signal. This is because there is a short but large spike of supply current. If this is a problem, the resistor R_1 should be bypassed with a large (about 100 μF) capacitor.

The Logic Circuit

The logic circuit operates from a separate supply called the auxiliary supply. In a typical disk drive application, the auxiliary supply is usually within a diode drop of the normal supply, except when the normal supply is interrupted. Then the auxiliary supply is generated from the back EMF of the spindle motor. By having two supplies, the logic circuit can operate for a while after the main power has been removed.

There are two external inputs to the logic circuit, and one internal. The external inputs are enable and park-bar; the internal input is from the short circuit protection. The external inputs are TTL compatible and can be driven by CMOS gates. The internal short circuit protection input overrides the two external inputs. The park-bar input overrides the enable input when it is low. Note that when left open, the external inputs generate a logic low. Therefore, if the logic inputs are removed, the EL2036C/EL2037C go into park mode.

The Park Circuit

When the park-bar logic input is high, the park circuit is disabled and has no effect on the motor. When the park-bar logic input is low, the amplifiers are disabled and the park circuit is activated. Like the logic circuit, the park circuit uses the auxiliary supply, not the main supply. The park circuit sets the base of Q65 (the transistor whose emitter is pin 2) to about 2V. The value of the external resistor from pin 2 to ground, R_P, determines the current in the collector of the Q65 transistor. That current is mirrored and generates a voltage as it flows through two diodes, an internal resistor and a saturated transistor, Q68. The voltage is applied to the base of a darlington that drives $V_{OUT}-$, pin 17. At the same time, a current is sent to the base of the opposite output NPN transistor, pin 13. This saturates the external output NPN transistor. The voltage across the motor is now independent of the auxiliary supply voltage at pin 20 and is an inverse function of the resistor R_P.

Applications Information

Transconductance

The DC transconductance of the EL2036C/EL2037C is set by one resistor, R_s, that senses the motor current. The input voltage is the difference between the voltage on pin 8 and 9. When pin 8 is more positive than pin 9, the input is said to be positive. When the input is positive, the voltage on pin 14 is more positive than pin 17 and the motor current is said to be positive. The DC transconductance is given by the simple equation:

$$G_{MO} = \frac{1}{4R_s} = \frac{I_O}{V_{IN}-V_{REF}}$$

For a transconductance of 1 Amp per volt, the sense resistor, R_s, should equal 0.25Ω. Because the sense resistor is very small, care should be taken to insure that the PC board trace resistance does not increase its value. The connections from pin 5 and 17 are the "sense" connections while the motor and transistor collectors are the "force" connections. Therefore, the connections from pin 5 and pin 17 should go directly to the sense resistor.

Source Impedance

The input and reference source impedances should be low to prevent gain and offset errors. The input current is determined by the internal feedback resistors and the input and output voltages. The worst case current flows when the reference is low and the input is lower and therefore the V_O- output is high. This condition is tested and the input and reference currents are guaranteed to be less than 1.5 mA. Therefore, the input and reference should be able to sink and source

Applications Information — Contd.

1.5 mA. For the typical case where the transconductance is 1 Amp per volt, a source impedance of less than 10Ω will generate less than 2.5 mA of additional output offset current and less than 1.5% gain error. Obviously, if the output of an operational amplifier drives the EL2036C/EL2037C there will be no errors due to source impedance. Be careful with some single supply operational amplifiers (324 and 358 types). They require output loading to ground to eliminate their high output impedance and crossover distortion.

Transistors

The EL2036C/EL2037C will drive almost any pair of complementary transistors. The output transistor drive is guaranteed to be 2.5 mA. The required maximum output current divided by 25 mA gives the minimum H_{FE} required. For 1 Amp output current, the minimum H_{FE} is 40.

The important specifications for the output devices are:

BV_{CEO}	Minimum 15V
H_{FE}	Minimum 40 at 1 Amp
f_t	40 MHz or more
$V_{CE}(SAT)$	As low as possible

The MJE200 and MJE210 series are excellent with minimum H_{FE} of 45 and saturation voltages of only 300 mV at 1 Amp. The D44H11 and D45H11 series have even lower saturation voltages and a higher H_{FE} of 60. Both types are available in surface mount from Motorola, SGS and others.

Motor Characterization

The formulas for the compensation of the EL2036C/EL2037C are based on the electrical characteristics of the motor. For most high-performance voice coil motors, the effective impedance is a function of frequency that can not be modeled over a large frequency range with a simple resistor and inductor. Fortunately, for the compensation equations to work, it is only necessary to model the motor at the bandwidth frequency.

The easiest way to determine the resistance and inductance of a motor is to use an RLC meter that reads the inductance and resistance at the bandwidth frequency. If such a meter is not available, a network analyzer and a current probe will give the impedance versus frequency. From the magnitude and phase at the bandwidth frequency, the real and imaginary impedance can be calculated (and the imaginary part converted to inductance). Some network analyzers will even give the real and imaginary impedances directly.

The setup below was used to generate the following curve of impedance versus frequency on a real motor. At 10 kHz the impedance is 13Ω at 52°. This is 8Ω real and 10.25Ω reactive. Notice that the DC resistance is much less than the impedance at 10 kHz. The equivalent inductance is 163 μH.

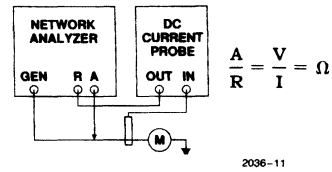


Figure 3. Motor Characterization Setup

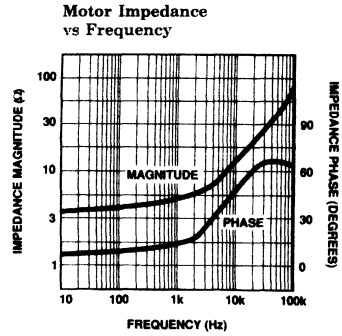


Figure 4

Compensation

The compensation components, C_c and R_c, are calculated to give the desired transconductance bandwidth. The equivalent motor resistance and inductance, R_m and L_m, the value of the sense resistor, R_s, and the bandwidth, BW, are used to compute C_c and R_c. The EL2036C/EL2037C require two identical networks for compensation. Each network is a series connection of a resistor, R_c, and a capacitor, C_c. The matching of the components is not critical, standard five percent tolerance is sufficient. The derivation of the fol-

EL2036C/EL2037C
Servo Motor Drivers

Applications Information — Contd.

lowing equations is in the AC Response Section.

$$C_c = \frac{4\,R_s}{800\,(R_m + R_s)\,2\pi\,BW}$$

$$R_c = \frac{L_m}{(R_m + R_s)\,C_c}$$

To compensate the motor described in the previous section for a 10 kHz bandwidth and a transconductance of 1 Amp per volt we substitute

$R_s = 0.25$ $L_m = 160\ \mu H$
$R_m = 8\Omega$ $BW = 10$ kHz

into the above equations.

$$C_c = \frac{4\,(0.25)}{800(8+0.25)(2)(3.14)(10\ kHz)} = 2400\ pF$$

use 2200 pF

$$R_c = \frac{160\ mH}{(8+0.25)(2200\ pF)} = 8800$$

use 10k.

Two 220 pF capacitors between pin 4 and pin 7, and between pin 6 and Ground (as shown in the Typical Application drawing on page 6) smooth fast rising input signals to ensure that the operational amplifier will not slew rate limit. Both capacitors can be eliminated if the slew rate of the input signal does not exceed 0.5 V/μs.

Park Function

The EL2036C/EL2037C will force a constant voltage across the motor when pin 3, park-bar, is open or low. The output voltage is negative; pin 14 if forced to about zero volts and pin 17 to the constant voltage determined by the resistor R_P from pin 2 to ground. This voltage drive produces a constant velocity that is used to park the heads. The power to drive the motor is supplied from an auxiliary supply (Aux Sup) on pin 20. Usually this auxiliary supply is the normal supply reduced by a diode drop. The spindle motor also is tied to the auxiliary supply. Once the normal supply drops, the spindle motor back EMF acts as a generator and holds the voltage up long enough for the drive to park the heads. An external bypass capacitor is needed on pin 20 to filter the ripple. To determine the value of the resistor required from pin 2 to ground use the curve of Output Park Voltage versus Park Resistor (page 5).

Protection Circuit

The EL2036C/EL2037C have a protection circuit that prevents damage if either of the motor terminals is shorted to ground. The circuit senses the total supply current with a resistor, R_1, and disables the amplifiers during over-current conditions. The curve of Protection Circuit Trip Current versus Limit Sense Resistor (page 5) should be used to select the proper resistor. For a typical 1 Amp output current the resistor should equal 0.33Ω.

AC Response

The AC response of the EL2036C/EL2037C is set by the motor electrical time constant and the compensation impedance $Z(s)$. The actual circuit is quite difficult to analyze due to the differential techniques used to improve accuracy. To simplify the analysis, a single-ended system can be modeled with a summer, a forward path, the motor electrical elements and a feedback path. The forward path has a gain that includes the compensation components, and the feedback includes the current sense resistor, R_S. In this way we can solve for the response in terms of the actual EL2036C/EL2037C external component values.

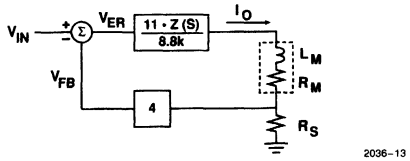


Figure 5. The Servo Motor Loop Equivalent Circuit

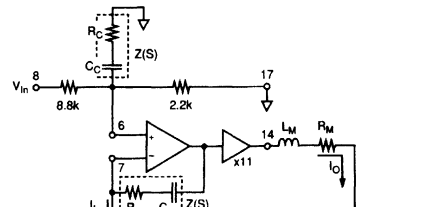


Figure 6. The Servo Motor Control Equivalent Circuit

AC Response — Contd.

The forward path gain of this circuit is the output current divided by the input voltage without any feedback.

$$A = \frac{I_o}{V_{IN}} = \frac{11Z(s)}{8.8K\,(sL_m + R_m + R_s)}$$

The feedback path is the feedback voltage divided by the output current.

$$b = \frac{V_{FB}}{I_O} = 4\,R_s$$

The closed loop response is therefore:

$$A_{CL} = \frac{A}{1 + A\beta} = \frac{\frac{1}{\beta}}{1 + \frac{1}{A\beta}}$$

$$= \frac{\frac{1}{4\,R_s}}{1 + \frac{800}{4\,R_s}\left(\frac{s\,L_m}{R_m + R_s} + 1\right)\left(\frac{R_m + R_s}{Z(s)}\right)}$$

The compensation network Z(s) is usually a series resistor and capacitor, R_c and C_c. That is to say

$$Z(s) = R_c + \frac{1}{s\,C_c} = \frac{s\,R_c\,C_c + 1}{s\,C_c}$$

Substituting this into the closed loop equation gives

$$A_{CL} = \frac{\frac{1}{4\,R_s}}{1 + \frac{800}{4\,R_s}\left(\frac{s\,L_m}{R_m + R_s} + 1\right)\frac{(R_m + R_s)\,s\,C_c}{(s\,R_c\,C_c + 1)}}$$

There are many ways to analyze this for the desired response. Bode plots, Nyquist plots and root locus techniques can all be used to determine the values of R_c and C_c for a particular motor. The simplest way to obtain the values of R_c and C_c is to make the zero due to them equal to the motor pole.

$$R_c\,C_c = \frac{L_m}{R_m + R_s}$$

Substituting this constraint into the closed loop equation results in a single pole system. The equation is:

$$A_{CL} = \frac{\frac{1}{4\,R_s}}{\frac{800}{4\,R_s}(R_m + R_s)\,s\,C_c + 1}$$

The closed loop −3 dB bandwidth (BW) is where the magnitude of the real and imaginary parts of the denominator are equal. We therefore can say, in terms of bandwidth in Hertz, that

$$\frac{800}{4\,R_s}(R_m + R_s)\,2\pi \bullet BW \bullet C_c = 1$$

Solving these for C_c and R_c gives:

$$C_c = \frac{4\,R_s}{800\,(R_m + R_s)\,2\,pBW}$$

$$R_c = \frac{L_m}{(R_m + R_s)\,C_c}$$

Simplified Schematic

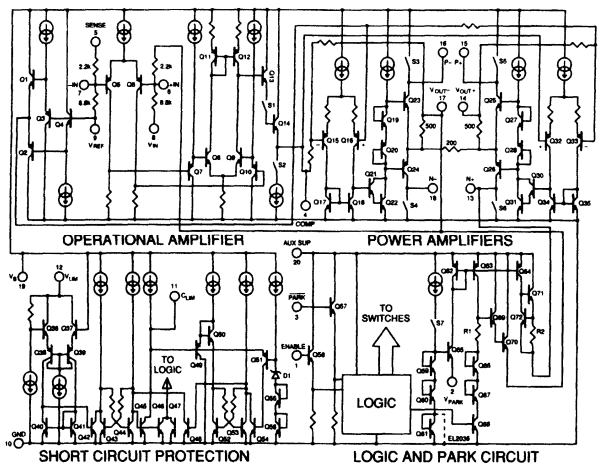


Figure 7

Buffers

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec Buffers

ELANTEC Part Number	Description	Warmed Up Input Current (Input Impedance)	Continuous Output Current Drive (Peak Output Current)	−3 dB Bandwidth (Risetime)	Typical Slew Rate	Supply Current	Packages
EL2031	500 MHz, 5000 V/μs FET Input, Internal Bypass Cap. Hybrid, Next Generation EL2004	2.5 nA Max (1000 MΩ Min)	±100 mA	550 MHz Typ (650 pS into 100Ω Load)	7000 V/μs	26 mA Max	12-Pin TO-8 CAN
EL2004	350 MHz FET INPUT BUFFER, Improved ELH0033, Hybrid	2.5 nA Max (10,000 MΩ Min)	±90 mA Min (±250 mA)	350 MHz Typ (1 ns)	2500 V/μs	24 mA Max	12-Pin TO-8 CAN 52-Pin LCC
EL2002	Monolithic, Low Cost 180 MHz BW, 5 mA Supply, 100 mA Out, Current Limited	6 μA Typ (1 MΩ Typ)	±100 mA Min Current Limits at ±130 mA Typical	180 MHz Typ	2000 V/μs	5 mA Typ	8-Pin CerDIP 8-Pin P-DIP 20-Pad LCC 20-Lead SOL
EL2005	PRECISION FET INPUT BUFFER, Improved ELH0033, Hybrid	1 nA Max (10,000 MΩ Min)	±90 mA Min (±250 mA)	140 MHz Typ	1500 V/μs	24 mA Max	12-Pin TO-8 CAN
ELH0033	Hybrid "Industry Standard" Pinout, See Also EL2004, EL2005	2.5 nA Max (10,000 MΩ Min)	±100 mA Min (±250 mA)	100 MHz Typ	1500 V/μs	24 mA Max	12-Pin TO-8 CAN
EL2003	Monolithic Excellent Video Buffer. Improved ELH0002, HA2-5002 & HA4-5002	25 μA Max (1 MΩ Min)	±105 mA Min (±230 mA)	100 MHz Typ (4 ns)	1200 V/μs	15 mA Max	TO-99 CAN 8-Pin CerDIP 8-Pin P-DIP 20-Pad LCC 20-Lead SOL
EL2033	Improved Pin for Pin with DIP HA-5033 and HA-5002. Monolithic, DI	25 μA Max (1 MΩ Min)	±105 mA Min (±230 mA)	100 MHz Typ (4 ns)	1200 V/μs	15 mA Max	8-Pin P-DIP 8-Pin CerDIP
EL2009	Monolithic, 90 MHz, 1A Out Video Buffer	±125 μA Max (250 kΩ Min)	±1A Min	90 MHz (7 ns)	3000 V/μs	65 mA Max	TO-220
EL2001	Monolithic, Low Cost 70 MHz BW, 1 mA Supply, 100 mA Out, Current Limited	2 μA Typ (1 MΩ Typ)	±100 mA Min Current Limits at ±130 mA Typical	70 MHz Typ	2000 V/μs	1.3 mA Typ	8-Pin CerDIP 8-Pin P-DIP 20-Pad LCC 20-Lead SOL
EL2008	Monolithic, 55 MHz, 1A Out Video Buffer	±35 μA Max (500 kΩ Min)	±1A Min	55 MHz (7 ns)	2500 V/μs	22 mA Max	TO-220
ELH0002	Hybrid "Industry Standard" Pinout, See Also EL2003	±10 μA Max (180 kΩ Min)	±100 mA Min (±400 mA)	30 MHz Typ (12 ns)	200 V/μs	10 mA Max	8-Pin TO-5 CAN

ELH0002/ELH0002C
Current Amplifier

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Features

- 400 mA pulsed output current
- DC to 30 MHz bandwidth
- 200 V/μs slew rate
- Low harmonic distortion
- High input impedance—400 kΩ
- Low output impedance—6Ω
- High power efficiency
- Operation from ±5V to ±20V
- Output voltage swing approaches supply voltage
- MIL-STD-883 devices manufactured in U.S.A.

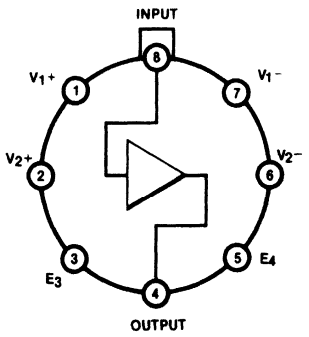
Applications

- Line driver
- 30 MHz buffer
- High-speed D/A conversion
- Instrumentation buffer
- Precision current source

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0002CH	−25°C to +85°C	TO-5	MDP0001
ELH0002H	−55°C to +125°C	TO-5	MDP0001
ELH0002H/883B	−55°C to +125°C	TO-5	MDP0001

7801301XX is the DESC version of this device.



Top View

Case is electrically isolated.

General Description

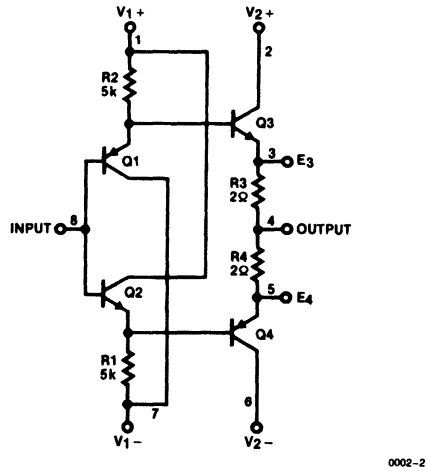
The ELH0002/ELH0002C is a general purpose hybrid current amplifier buffer that is built on a single substrate.

The ELH0002 is ideal for current buffering operational amplifiers without changing the characteristics of the Op. Amp. The ELH0002 uses a completely symmetrical circuit to provide a low output impedance when both sourcing and sinking current. This means the output will drive coaxial cables and other capacitive loads with equivalent rise and fall times.

The ELH0002 is specified for operation over the −55°C to +125°C military temperature range. The ELH0002C is specified for operation over the −25°C to +85°C temperature range.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Equivalent Schematic



ELH0002/ELH0002C
Current Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±22V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	±22V		ELH0002	−55°C to +125°C
P_D	Power Dissipation Ambient	600 mW		ELH0002C	−25°C to +85°C
T_{ST}	Storage Temperature	−65°C to +150°C		Steady State Current	±100 mA
				Pulsed Output Current (50 ms On/1 second Off)	±400 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±12V, $T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	ELH0002				ELH0002C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	R_S = 300Ω, R_L = 1 kΩ		±10	±30	I		±10	±30	II	mV
A_V	Voltage Gain	R_S = 10 kΩ, R_L = 1 kΩ, V_{IN} = ±10 V_{dc}	0.95	0.97		I	0.95	0.97		II	V/V
R_{IN}	Input Impedance	R_S = 200 kΩ, V_{IN} = ±1 V_{dc}, R_L = 1 kΩ	180	400		I	180	400		II	kΩ
R_{OUT}	Output Impedance	R_S = 50Ω, V_{IN} = ±1 V_{dc}, R_S = 10 kΩ		6	10	I		6	10	II	Ω
V_O	Output Voltage Swing	V_{IN} = ±12V, R_L = 1 KΩ	±10	±11		I	±10	±11		II	V
		V_S = ±15V, V_{IN} = ±12V, R_S = 50Ω, R_L = 100Ω, T_A = 25°C	±10			I	±10			I	V
I_B	Input Current	R_S = 10 kΩ, R_L = 1 kΩ		±6	±10	I		±6	±10	II	μA
I_S+	Positive Supply Current	R_S = 10 kΩ, R_L = 1 kΩ		6	10	I		6	10	II	mA
I_S-	Negative Supply Current	R_S = 10 kΩ, R_L = 1 kΩ		−6	−10	I		−6	−10	II	mA

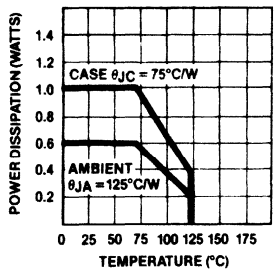
Note 1: Elantec's ELH0002H/200 is tested to the ELH0002 DC limits at −25°C, +25°C and +125°C, and the AC limits at 25°C. In addition, the parts are also tested to the DC limits for V_{OS}, A_{VOL} with R_L = 1 kΩ, I_{IN}, I_S+ and I_S- at 200°C.

AC Electrical Characteristics $V_S = \pm 12V$, $T_A = 25°C$

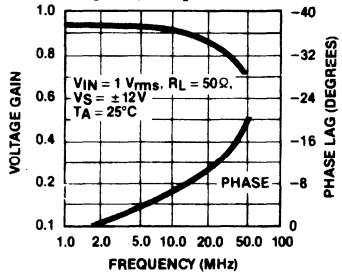
Parameter	Description	Test Conditions	ELH0002				ELH0002C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
A_V	Voltage Gain	R_S = 10 kΩ, R_L = 1 kΩ V_{IN} = 3 V_{P-P}, f = 1 kHz	0.95	0.97		I	0.95	0.97		II	V/V
A_I	Current Gain	V_{IN} = 1 V_{RMS}, f = 1 kHz		40		V		40		V	A/mA
R_{IN}	Input Impedance	R_S = 200 kΩ, V_{IN} = 1 V_{RMS}, R_L = 1 kΩ, f = 1 kHz	180	400		I	180	400		II	kΩ
R_{OUT}	Output Impedance	R_L = 50Ω, V_{IN} = 1 V_{RMS}, R_S = 10 kΩ, f = 1 kHz		6	10	I		6	10	II	Ω
HD	Harmonic Distortion	V_{IN} = 5 V_{RMS}, f = 1 kHz		0.1		V		0.1		V	%
t_r	Rise Time	R_L = 50Ω, ΔV_{IN} = 100 mV		7	12	III		7	12	III	ns

Typical Performance Curves

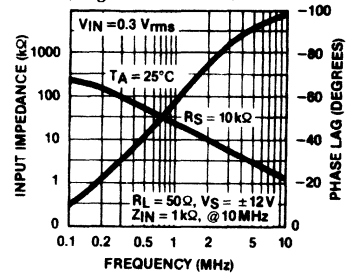
Maximum Power Dissipation



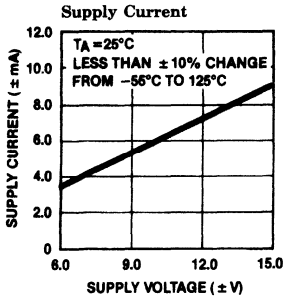
Frequency Response



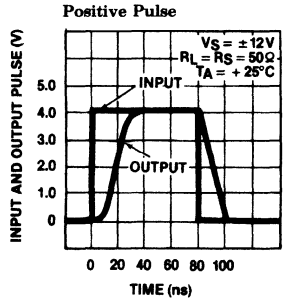
Input Impedance (Magnitude & Phase)



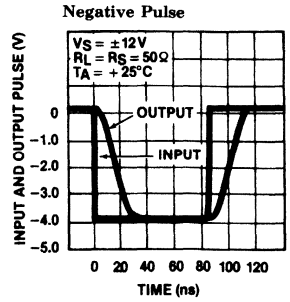
Supply Current



Positive Pulse



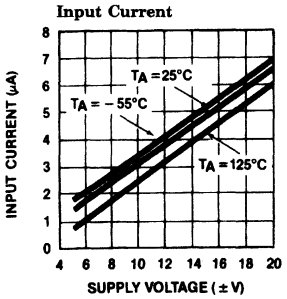
Negative Pulse



0002-3

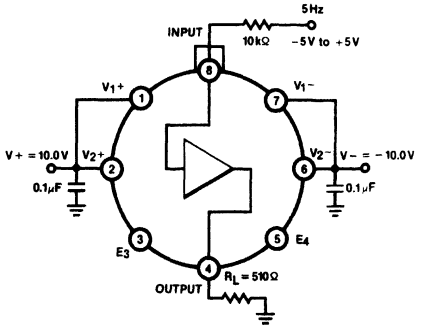
ELH0002/ELH0002C
Current Amplifier

Typical Performance Curves — Contd.



0002-4

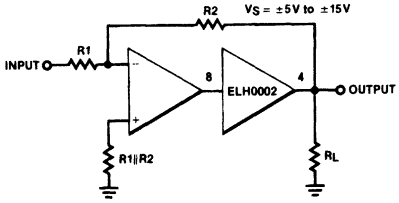
Burn-In Circuit



0002-5

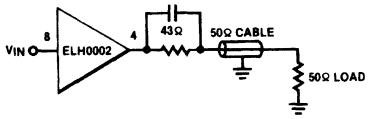
Typical Applications

High Current Operational Amplifier



0002-6

Line Driver



0002-7

Select capacitor to adjust time response of pulse.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0033/ELH0033C
Fast Buffer Amplifier

Features

- Slew rate—1500 V/μs
- Output drive—100 mA
- Rise and fall times—2.9 ns
- Input resistance—$10^{11}\Omega$
- Power bandwidth—100 MHz
- MIL-STD-883 devices 100% manufactured in U.S.A.

Advantages

- Excellent phase linearity
- Driver cables and other capacitive loads
- Wide supply range, single or split

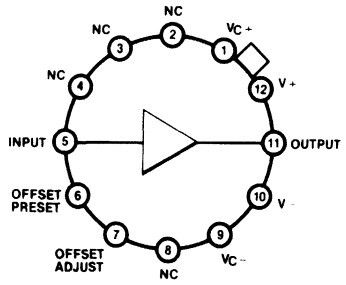
Ordering Information

Part No.	Temp. Range	Package	Outline #
ELH0033CG	−25°C to +85°C	TO-8	MDP0002
ELH0033G	−55°C to +125°C	TO-8	MDP0002
ELH0033G/883B	−55°C to +125°C	TO-8	MDP0002

8001401ZX is the DESC version of this device.

Connection Diagram

8-Pin TO-8



Top View

Note: Case is electrically isolated.

General Description

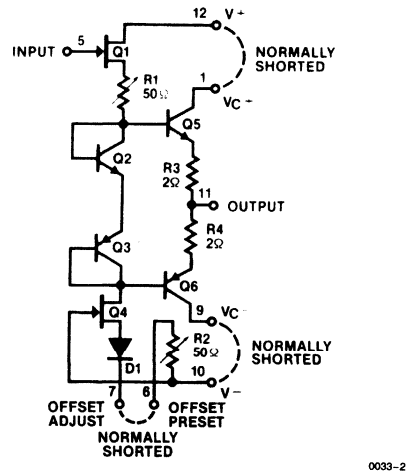
The ELH0033 is a high-speed, FET input voltage follower buffer designed to provide high output currents from DC to over 100 MHz. The ELH0033 slews at 1500 V/μs and will drive 100Ω loads. Phase linearity is excellent to 20 MHz, allowing the buffer to be included in op amp loops.

The ELH0033 is intended to fulfill a wide range of buffer applications such as high-speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high-speed A to D's and comparators.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The ELH0033 is specified for operation from −55°C to +125°C; the ELH0033C is specified from −25°C to +85°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Equivalent Schematic



ELH0033/ELH0033C
Fast Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		ELH0033	−55°C to +125°C
P_D	Power Dissipation (See Curves)	1.5W		ELH0033C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, V_{IN} = 0V, $T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	ELH0033				ELH0033C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le 100$ kΩ, T_J = 25°C (Note 1)		5	10	I		12	20	I	mV
		$R_S \le 100$ kΩ			15	I			25	III	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Offset Voltage	R_S = 100Ω		50		V		50		V	µV/°C
I_B	Input Bias Current	T_J = 25°C (Note 1)			250	I			500	I	pA
		T_A = 25°C (Note 2)			2.5	IV			5	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			20	III	nA
A_V	Voltage Gain	R_S = 100Ω, R_L = 1 kΩ, V_{IN} = ±10V	0.97	0.98	1.00	I	0.96	0.98	1.00	II	V/V
R_{IN}	Input Impedance	R_L = 1 kΩ	10^{10}	10^{11}		IV	10^{10}	10^{11}		IV	Ω
		T_J = 25°C (Note 1), R_L = 1 kΩ	10^{10}	10^{11}		I	10^{10}	10^{11}		I	Ω
R_O	Output Impedance	R_L = 1 kΩ, V_{IN} = ±1V		6	10	I		6	10	II	Ω
V_O	Output Voltage Swing	V_{IN} = ±14V, R_L = 1 kΩ	±12			I	±12			II	V
		V_{IN} = ±10.5V, R_L = 100Ω, T_A = 25°C	±9			I	±9			I	V
I_S	Supply Current		14.5	20	22	I		21	24	II	mA
	Power Consumption			600	660	I		630	720	II	mW

Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25°C. When supply voltages are ±15V, no-load operating junction temperature may rise 40°C–60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

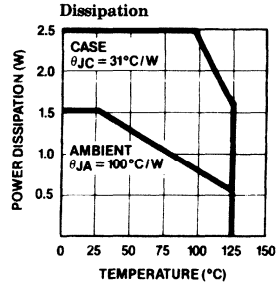
Note 2: Measured in still air 7 minutes after application of power.

AC Electrical Characteristics $T_C = 25°C, V_S = \pm 15V, R_S = 50\Omega, R_L = 1\ k\Omega$

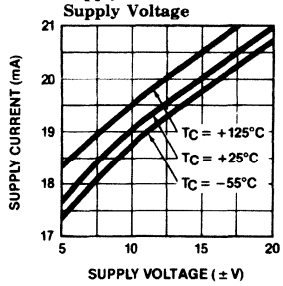
Parameter	Description	Test Conditions	ELH0033				ELH0033C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	$V_{IN} = \pm 10V$	1000	1500		III	1000	1400		III	V/μs
BW	Bandwidth	$V_{IN} = 1\ V_{rms}$		100		V		100		V	MHz
	Phase Non-Linearity	BW = 1 MHz to 20 MHz		2		V		2		V	°
t_r	Rise Time	$\Delta V_{IN} = 0.5V$		2.9		V		3.2		V	ns
t_p	Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2		V		1.5		V	ns
HD	Harmonic Distortion	f > 1 kHz		<0.1		V		<0.1		V	%
A_V	Voltage Gain	$R_S = 100\Omega$, $V_{IN} = 1\ V_{rms}$, f = 1 kHz	0.97	0.98	1.00	I	0.96	0.98	1.00	II	V/V
R_O	Output Impedance	$V_{IN} = 1\ V_{rms}$, f = 1 kHz		6	10	I		6	10	II	Ω

Typical Performance Curves

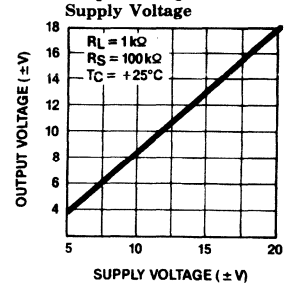
Maximum Power Dissipation



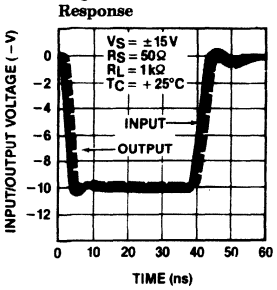
Supply Current vs Supply Voltage



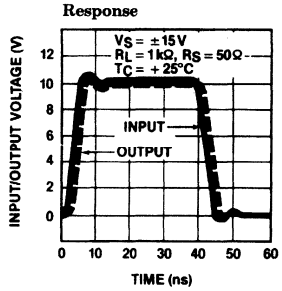
Output Voltage vs Supply Voltage



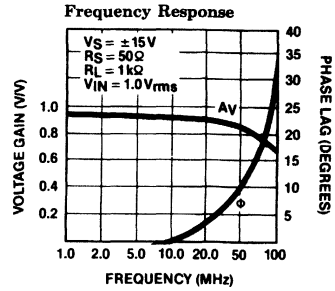
Negative Pulse Response



Positive Pulse Response



Frequency Response

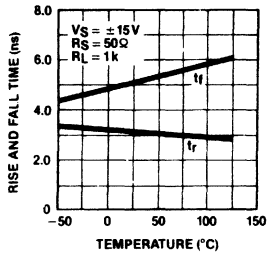


0033-3

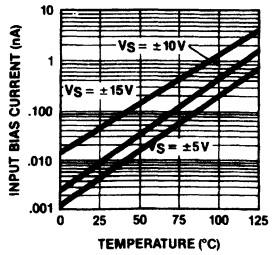
ELH0033/ELH0033C
Fast Buffer Amplifier

Typical Performance Curves — Contd.

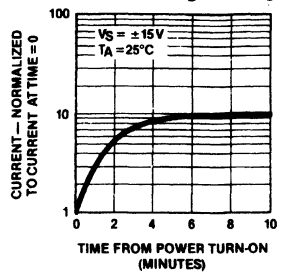
Rise and Fall Time vs Temperature



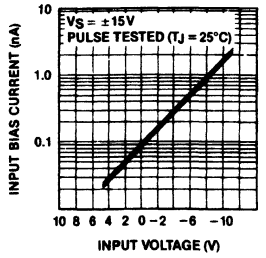
Input Bias Current vs Temperature



Normalized Input Bias Current During Warm-up



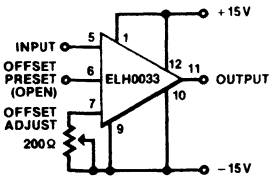
Input Bias Current vs Input Voltage



0033-4

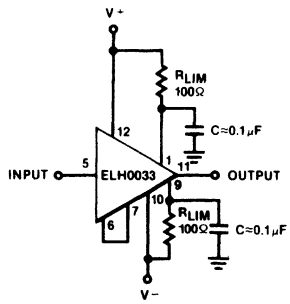
Typical Applications

Offset Zero Adjust



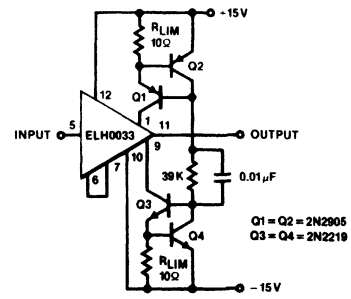
0033-5

Using Resistor Current Limiting



0033-6

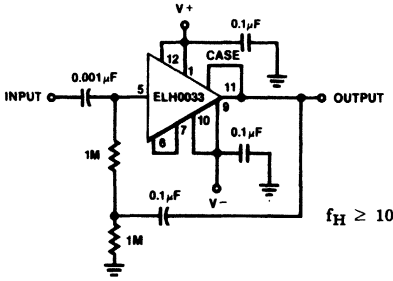
Current Limiting Using Current Sources



0033-7

Typical Applications — Contd.

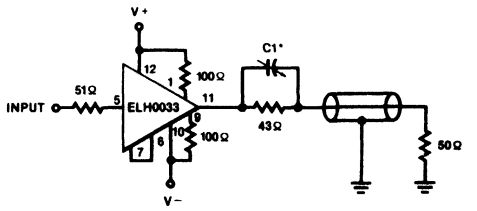
High Input Impedance AC Coupled Amplifier



$f_H \geq 100$ MHz

0033-8

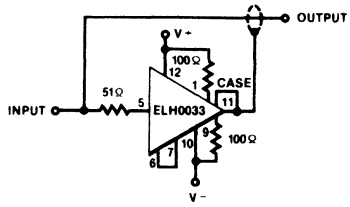
Coaxial Cable Driver



0033-9

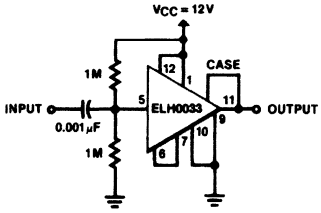
*Select C1 for optimum pulse response

Instrumentation Shield/Line Driver



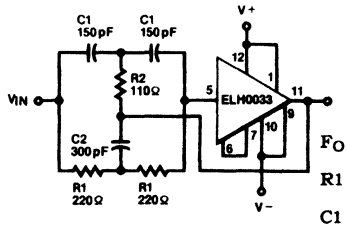
0033-10

Single Supply AC Amplifier



0033-11

4.5 MHz Notch Filter



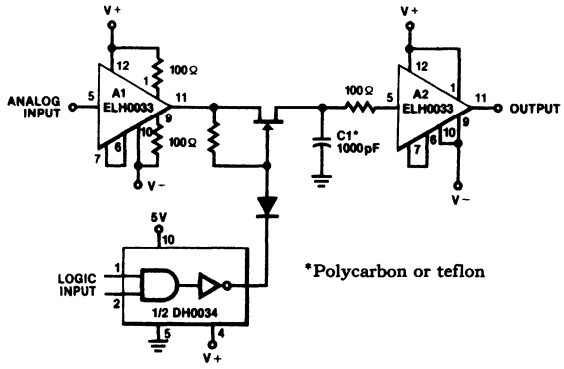
$$F_O = \frac{1}{2\pi R1C1}$$

$$R1 = 2\ R2$$

$$C1 = \frac{C2}{2}$$

0033-12

High-Speed Sample and Hold



*Polycarbon or teflon

0033-13

ELH0033/ELH0033C
Fast Buffer Amplifier

Applications Information

Recommended Layout Precautions

RF/video printed circuit board layout rules should be followed when using the ELH0033 since it will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment

The ELH0033's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. The pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω between the offset adjust pin and $V-$.

Operation from Single or Asymmetrical Power Supplies

This device type may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005\,(V^+ - V^-)$$

where: A_V = No load voltage gain, typically 0.99
V^+ = Positive supply voltage
V^- = Negative supply voltage

For the above example, ΔV_O would be -35 mV. This may be adjusted to zero as described in Section 2. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection

In order to optimize transient response and output swing, output current limit has been omitted from the ELH0033. Short circuit protection may be added by inserting appropriate value resistors between $V+$ and V_C+ pins and $V-$ and V_C- pins. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for ELH0033

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing uses current sources which are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

$$R_{LIM} \cong \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

Capacitive Loading

The ELH0033 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times d_v/d_t)$ should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\frac{\Delta V_{IN}}{\Delta t} \times C_L \leq I_{OUT} \leq \pm 250\text{ mA}$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the total package power rating:

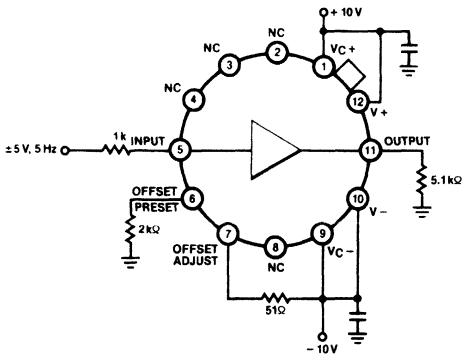
$$P_D \text{ pkg} \geq P_{DC} + P_{AC}$$
$$P_D \text{ pkg} \geq (V^+ - V^-) \times I_S + P_{AC}$$
$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

where: V_{P-P} = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

Operation within an Op Amp Loop

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as the ELH0032 and HA2500 and HA2600 series. An isolation resistor of 47Ω should be used between the op amp output and the input of ELH0033. The wide bandwidth and high slew rates of the ELH0033 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Burn-In Circuit



0033-14

Hardware

In order to utilize the full drive capabilities of the ELH0033, it should be mounted with a heatsink, particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

IMPORTANT!

Power supply bypassing is necessary to prevent oscillation with the ELH0033 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2001/EL2001C
Low Power, 70 MHz Buffer Amplifier

Features
- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 1 μA typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

Applications
- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2001ACJ	0°C to +75°C	CerDIP	MDP0010
EL2001ACN	0°C to +75°C	P-DIP	MDP0006
EL2001AJ	−55°C to +125°C	CerDIP	MDP0010
EL2001AJ/883B	−55°C to +125°C	CerDIP	MDP0010
EL2001AL	−55°C to +125°C	20-Pad LCC	MDP0007
EL2001AL/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EL2001CJ	0°C to +75°C	CerDIP	MDP0010
EL2001CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2001CN	0°C to +75°C	P-DIP	MDP0006
EL2001J	−55°C to +125°C	CerDIP	MDP0010
EL2001J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2001L	−55°C to +125°C	20-Pad LCC	MDP0007
EL2001L/883B	−55°C to +125°C	20-Pad LCC	MDP0007

Manufactured under U.S. Patent No. 4,833,424

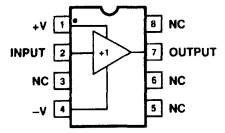
General Description
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patents pending buffer has a −3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing, Monolithic Integrated Circuits.*

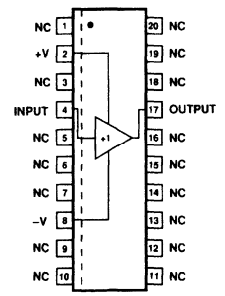
Connection Diagrams

EL2001 DIP Pinout



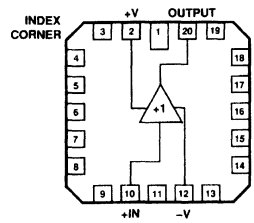
Top View

EL2001 SOL Pinout



Top View

EL2001 LCC Pinout



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage (Note 1)	±15V or V_S		Ceramic Packages	175°C
I_{IN}	Input Current (Note 1)	±50 mA		Plastic Packages	150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
	Output Short Circuit			Lead Temperature	
	Duration (Note 3)	Continuous		DIP Package (Soldering, < 10 seconds)	300°C
T_A	Operating Temperature Range			SOL Package	
	EL2001A/EL2001	−55°C to +125°C		Vapor Phase (60 seconds)	215°C
	EL2001AC/EL2001C	0°C to +75°C		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2001A EL2001	EL2001AC EL2001C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	Test Level	
V_{OS}	Offset Voltage EL2001A/EL2001AC	0	∞	25°C	−10	2	+10	I	I	mV
				T_{MIN}, T_{MAX}	−15		+15	I	III	mV
	EL2001/EL2001C	0	∞	25°C	−30	2	+30	I	I	mV
				T_{MIN}, T_{MAX}	−40		+40	I	III	mV
I_{IN}	Input Current EL2001A/EL2001AC	0	∞	25°C	−3	1	+3	I	I	μA
				T_{MIN}, T_{MAX}	−6		+6	I	III	μA
	EL2001/EL2001C	0	∞	25°C	−5	1	+5	I	I	μA
				T_{MIN}, T_{MAX}	−10		+10	I	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°	3	8		I	I	MΩ
				T_{MIN}, T_{MAX}	1			I	III	MΩ

EL2001/EL2001C
Low Power, 70 MHz Buffer Amplifier

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2001A EL2001	EL2001AC EL2001C	Units
		V_{in}	Load	Temp	Min	Typ	Max	Test Level	Test Level	
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	I	V/V
				T_{MIN}, T_{MAX}	0.985			I	III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.83	0.93		I	I	V/V
				T_{MIN}, T_{MAX}	0.80			I	III	V/V
A_{V3}	Voltage Gain with $V_S = \pm 5V$	±3V	100Ω	25°C	0.82	0.89		I	I	V/V
				T_{MIN}, T_{MAX}	0.79			I	III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	I	V
				T_{MIN}, T_{MAX}	±9.5			I	III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		10	15	I	I	Ω
				T_{MIN}, T_{MAX}			18	I	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±100	±160		I	I	mA
				T_{MIN}, T_{MAX}	±95			I	III	mA
I_S	Supply Current	0	∞	25°C		1.3	2.0	I	I	mA
				T_{MIN}, T_{MAX}			2.5	I	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	I	dB
				T_{MIN}, T_{MAX}	50			I	III	dB
t_r	Rise Time	0.5V	100Ω	25°C		4.2		V	V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		2.0		V	V	ns
SR	Slew Rate, (Note 6)	±10V	100Ω	25°C	1200	2000		IV	IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

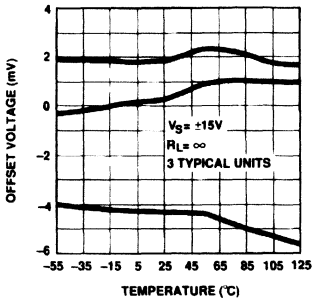
Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and at $V_S+ = +18V$, $V_S- = +18V$. Both supplies are changed simultaneously.

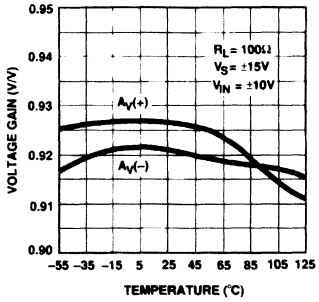
Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

Typical Performance Curves

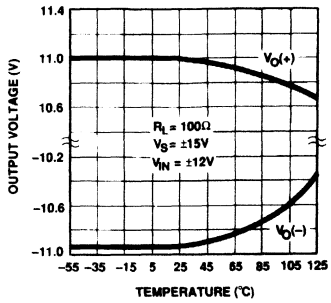
Offset Voltage vs Temperature



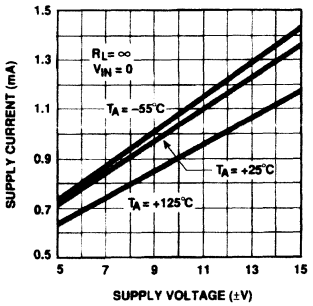
Voltage Gain vs Temperature



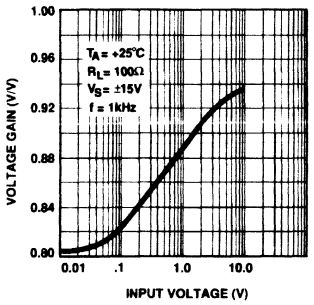
Output Voltage Swing vs Temperature



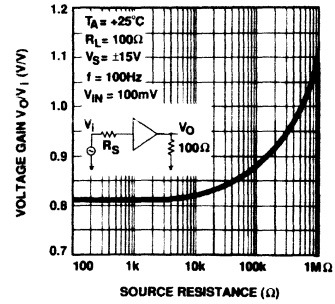
Supply Current vs Supply Voltage



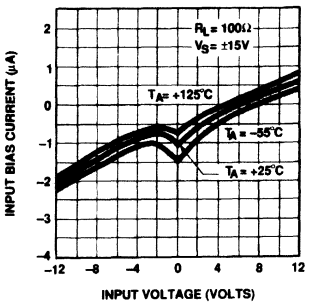
Voltage Gain vs Input Voltage



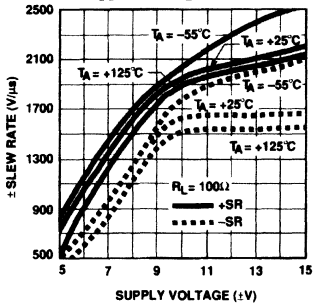
Voltage Gain vs Source Resistance



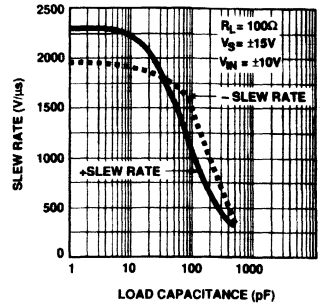
Input Bias Current vs Input Voltage



±Slew Rate vs Supply Voltage



±Slew Rate vs Capacitive Load



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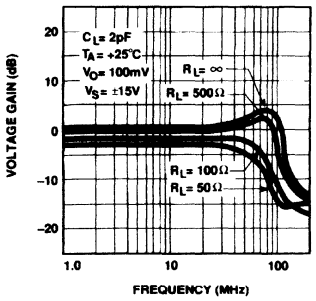
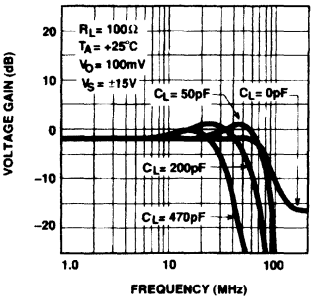
EL2001/EL2001C
Low Power, 70 MHz Buffer Amplifier

Typical Performance Curves — Contd.

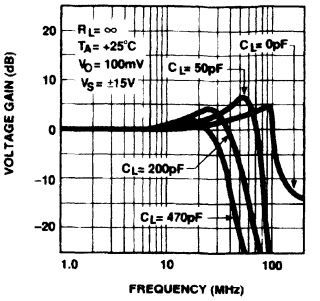
Voltage Gain vs Frequency for Various Resistive Loads



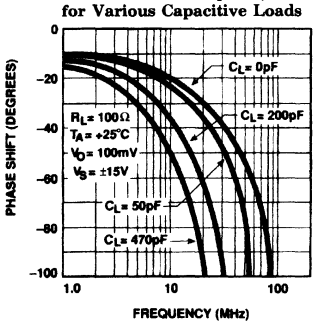
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100Ω



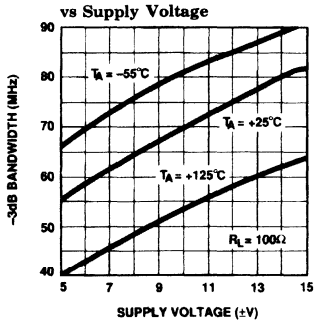
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



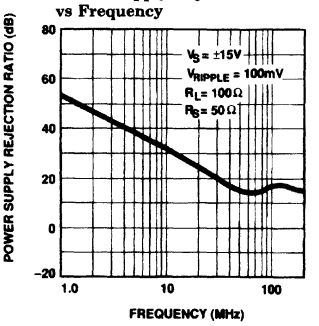
Phase Shift vs Frequency for Various Capacitive Loads



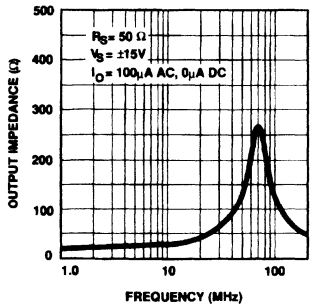
−3 dB Bandwidth vs Supply Voltage



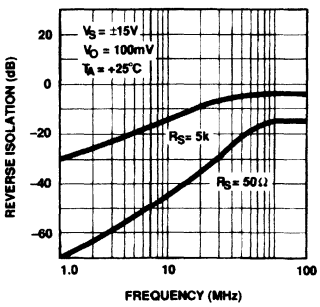
Power Supply Rejection Ratio vs Frequency



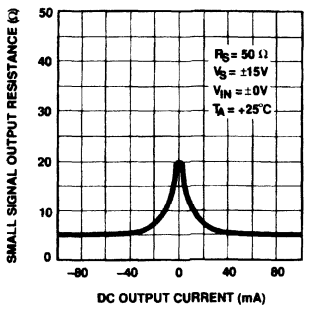
Output Impedance vs Frequency



Reverse Isolation vs Frequency



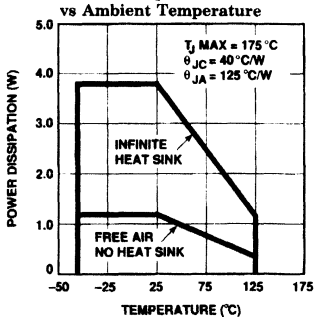
Small Signal Output Resistance vs Output Current



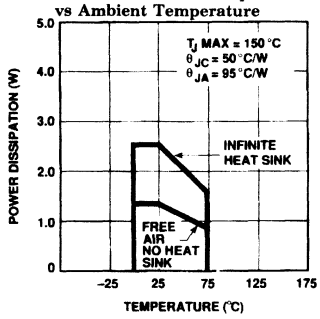
2001-5

Typical Performance Curves — Contd.

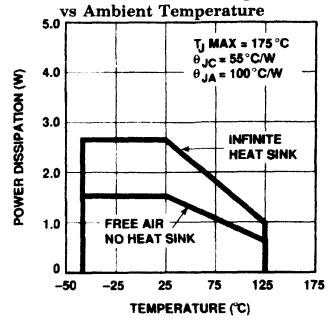
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



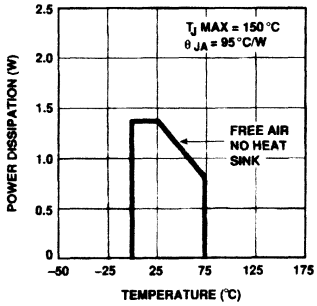
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



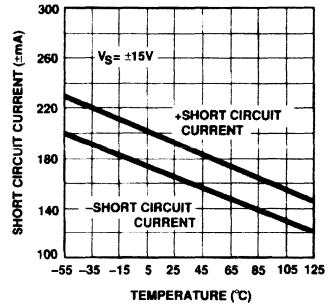
20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature

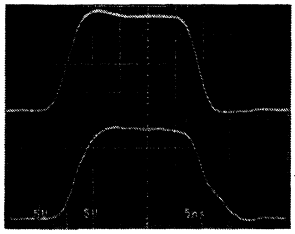


Short Circuit Current vs Temperature



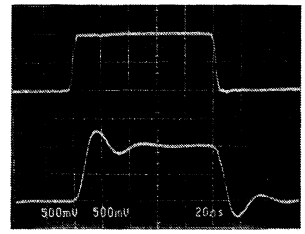
2001-6

Large Signal Response



2001-7

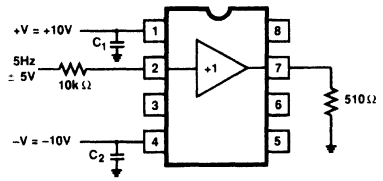
Small Signal Response



2001-8

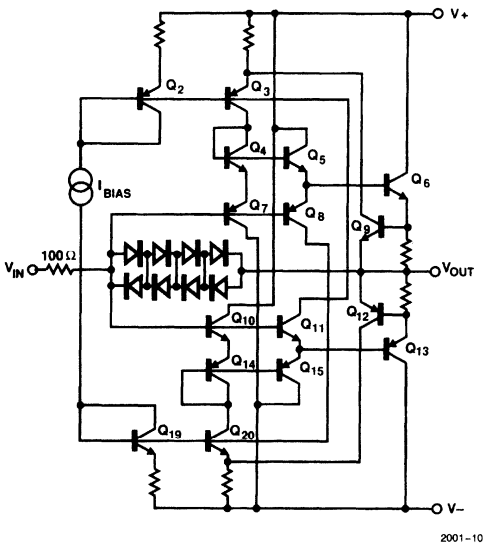
EL2001/EL2001C
Low Power, 70 MHz Buffer Amplifier

Burn-In Circuit



2001-9

Simplified Schematic



2001-10

Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

Source Impedance

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capactive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2002/EL2002C
Low Power, 180 MHz Buffer Amplifier

Features

- 180 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 3 μA typical
- 100 mA output current
- 5 mA supply current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Isolation buffer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2002ACJ	0°C to +75°C	CerDIP	MDP0010
EL2002ACN	0°C to +75°C	P-DIP	MDP0031
EL2002AJ	−55°C to +125°C	CerDIP	MDP0010
EL2002AJ/883B	−55°C to +125°C	CerDIP	MDP0010
EL2002AL	−55°C to +125°C	20-Pad LCC	MDP0007
EL2002AL/883B	−55°C to +125°C	20-Pad LCC	MDP0007
EL2002CJ	0°C to +75°C	CerDIP	MDP0010
EL2002CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2002CN	0°C to +75°C	P-DIP	MDP0006
EL2002J	−55°C to +125°C	CerDIP	MDP0010
EL2002J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2002L	−55°C to +125°C	20-Pad LCC	MDP0007
EL2002L/883B	−55°C to +125°C	20-Pad LCC	MDP0007

General Description

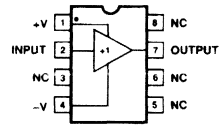
The EL2002 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantic monolithic Complementary Bipolar process, this patent pending buffer has a −3 dB bandwidth of 180 MHz, and delivers 100 mA, yet draws only 5 mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. Typical examples include fast op-amp output current boosters, coaxial cable drivers and A/D converter input buffers.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing, Monolithic Integrated Circuits.*

Connection Diagrams

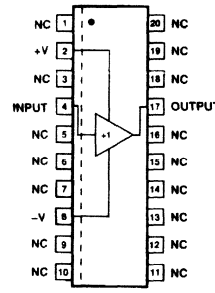
EL2002 DIP Pinout



2002-1

Top View

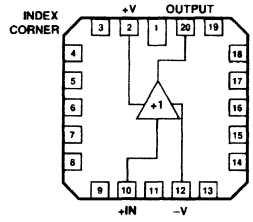
EL2002 SOL Pinout



2002-2

Top View

EL2002 LCC Pinout



2002-3

Top View

Manufactured Under U.S. Patent No. 4,833,424

EL2002/EL2002C
Low Power, 180 MHz Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage ($V^+ - V^-$)	±18V or 36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
P_D	Power Dissipation (Note 2)	See Curves
	Output Short Circuit Duration (Note 3)	Continuous
T_A	Operating Temperature Range:	
	EL2002A/EL2002	−55°C to +125°C
	EL2002AC/EL2002C	0°C to +75°C
T_J	Operating Junction Temperature	
	Ceramic Packages	175°C
	Plastic Packages	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature	
	DIP Package (soldering, <10 seconds)	300°C
	SOL Package	
	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2002A EL2002	EL2002AC EL2002C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	Test Level	
V_{OS}	Offset Voltage EL2002A/EL2002AC	0	∞	25°C	−15	5	+15	I	I	mV
				T_{MIN}, T_{MAX}	−20		+20	I	III	mV
	EL2002/EL2002C	0	∞	25°C	−40	10	+40	I	I	mV
				T_{MIN}, T_{MAX}	−50		+50	I	III	mV
I_{IN}	Input Current EL2002A/EL2002AC	0	∞	25°C	−10	3	+10	I	I	μA
				T_{MIN}, T_{MAX}	−15		+15	I	III	μA
	EL2002/EL2002C	0	∞	25°C	−15	5	+15	I	I	μA
				T_{MIN}, T_{MAX}	−20		+20	I	III	μA
R_{IN}	Input Resistance	+12V	100Ω	25°C	1	3		I	I	MΩ
				T_{MIN}, T_{MAX}	0.1			I	III	MΩ
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	I	V/V
				T_{MIN}, T_{MAX}	0.985			I	III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.85	0.93		I	I	V/V
				T_{MIN}, T_{MAX}	0.83			I	III	V/V

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2002A EL2002	EL2002AC EL2002C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	Test Level	
A_{V3}	Voltage Gain with $V_S = \pm 5V$	$\pm 3V$	100Ω	25°C	0.83	0.91		I	I	V/V
				T_{MIN}, T_{MAX}	0.80			I	III	V/V
V_O	Output Voltage Swing	$\pm 12V$	100Ω	25°C	± 10	± 11		I	I	V
				T_{MIN}, T_{MAX}	± 9.5			I	III	V
R_{OUT}	Output Resistance	$\pm 2V$	100Ω	25°C		8	13	I	I	Ω
				T_{MIN}, T_{MAX}			15	I	III	Ω
I_{OUT}	Output Current	$\pm 12V$	(Note 4)	25°C	+100	+160		I	I	mA
				T_{MIN}, T_{MAX}	± 95			I	III	mA
I_S	Supply Current	0	∞	25°C		5	7.5	I	II	mA
				T_{MIN}, T_{MAX}			10	I	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	I	dB
				T_{MIN}, T_{MAX}	50			I	III	dB
t_r	Rise Time	0.5V	100Ω	25°C		2.8		V	V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		1.5		V	V	ns
SR	Slew Rate, (Note 6)	$\pm 10V$	100Ω	25°C	1200	2000		IV	IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds $\pm 7.5V$ then the input current must be limited to ± 50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to $+12V$ and the output to $+10V$ and measure the output current. Repeat with -12 V_{IN} and $-10V$ on the output.

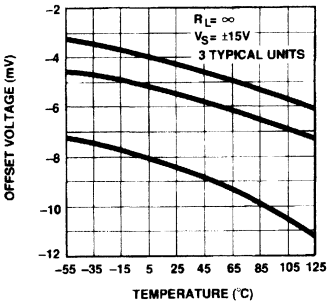
Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and $V_S+ = +18V$, $V_S- = 18V$. Both supplies are changed simultaneously.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

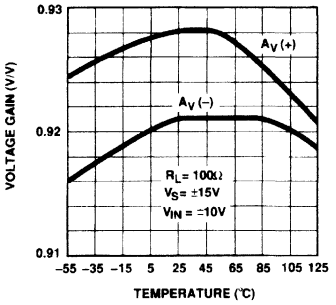
EL2002/EL2002C
Low Power, 180 MHz Buffer Amplifier

Typical Performance Curves

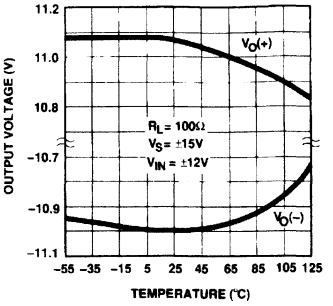
Offset Voltage vs Temperature



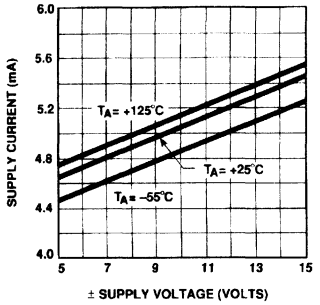
Voltage Gain vs Temperature



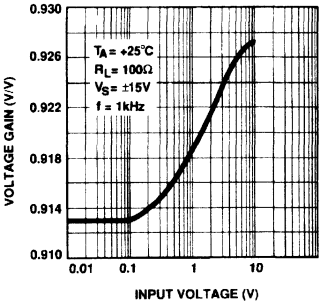
Output Voltage Swing vs Temperature



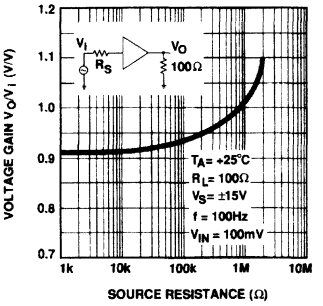
Supply Current vs Supply Voltage



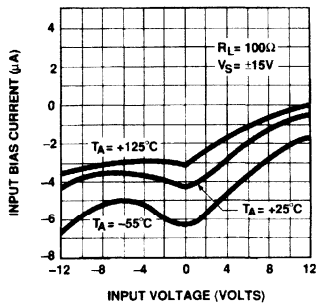
Voltage Gain vs Input Voltage



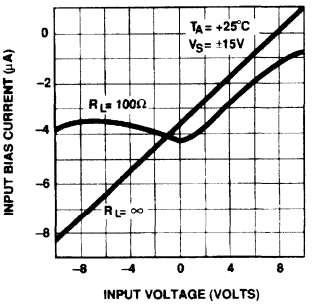
Voltage Gain vs Source Resistance



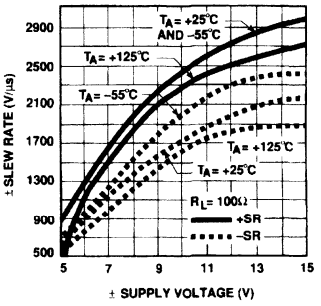
Input Bias Current vs Input Voltage at Various Temperatures



Input Bias Current vs Input Voltage



±Slew Rate vs Supply Voltage



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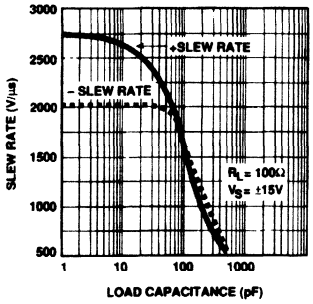
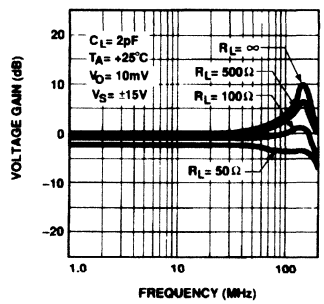
Typical Performance Curves — Contd.

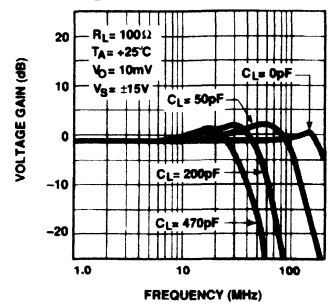
Slew Rate vs Load Capacitance



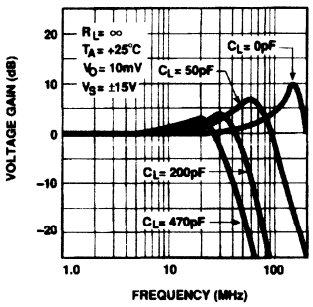
Voltage Gain vs Frequency for Various Resistive Loads



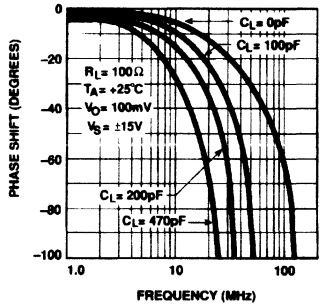
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100Ω



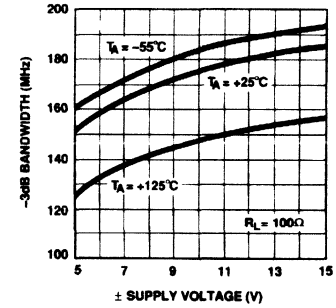
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



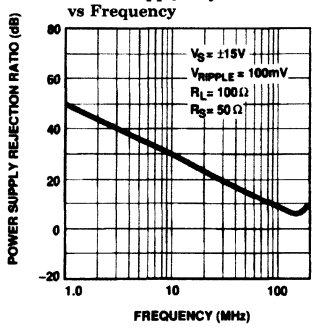
Phase Shift vs Frequency for Various Capacitive Loads



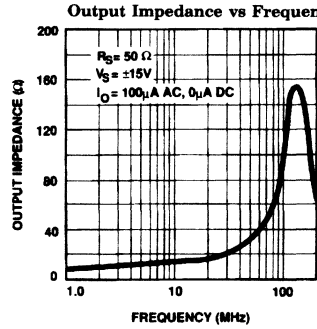
−3 dB Bandwidth vs Supply Voltage



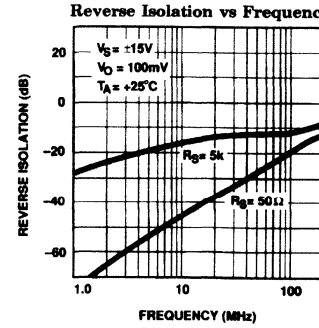
Power Supply Rejection Ratio vs Frequency



Output Impedance vs Frequency



Reverse Isolation vs Frequency



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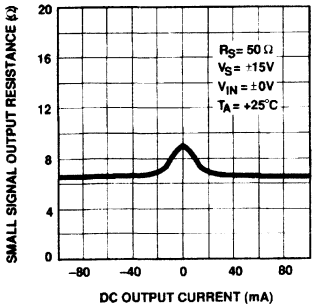
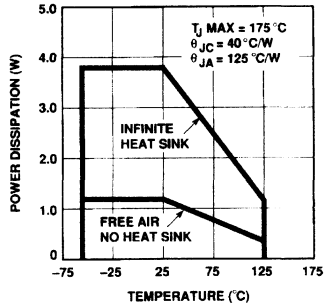
EL2002/EL2002C
Low Power, 180 MHz Buffer Amplifier

Typical Performance Curves — Contd.

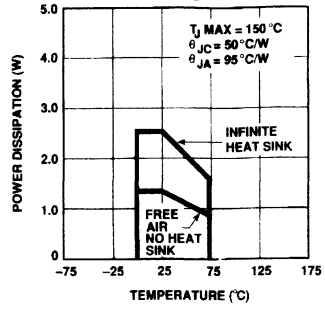
Small Signal Output Resistance vs Output Current



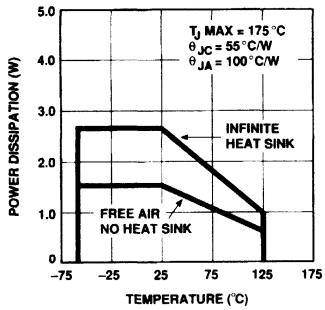
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



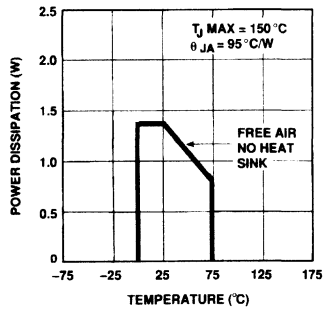
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



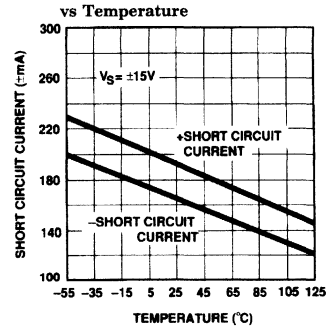
20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



Short Circuit Current vs Temperature



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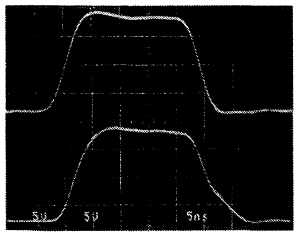
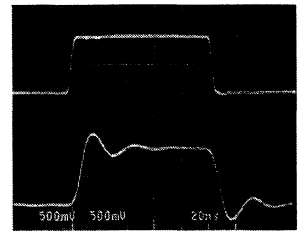
Large Signal Response



2002-8

Small Signal Response



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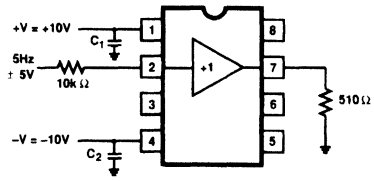
Burn-In Circuit



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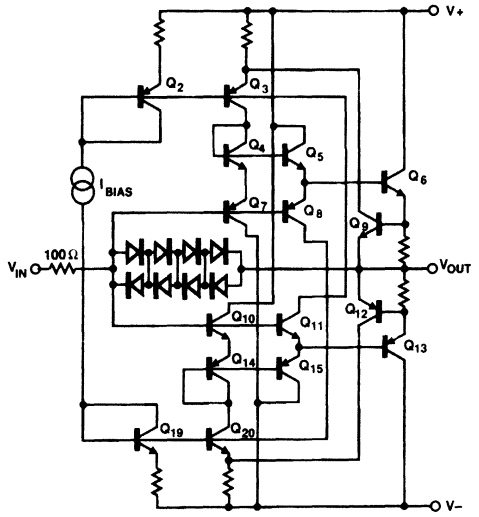
Simplified Schematic



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Application Information

The EL2002 is a monolithic buffer amplifier built on Elantec's proprietary Complementary Bipolar process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2002 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2002's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2002 may be operated with single or split supplies with total voltage difference between 10V ($\pm$5V) and 36V ($\pm$18V). It is not necessary to use equal split value supplies. For example $-$5V and $+$12V would be excellent for signals from $-$2V to $+$9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2002 looks like a resistance in parallel with about 3.5 pF in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about $\pm$2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above $\pm$7.5V differential input to output, additional series resistance should be added.

Source Impedance

The EL2002 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resisitive sources up to 1 MHz present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Features

- Differential gain 0.1%
- Differential phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- EL2003—Pin compatible with LH0002CN, LH0002H, HA2-5002
- EL2033—Pin compatible with HA3-5002, HA7-5002, HA3-5033, HA7-5033

Applications

- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2003CJ	0°C to +75°C	CerDIP	MDP0010
EL2003CN	0°C to +75°C	P-DIP	MDP0031
EL2003CH	0°C to +75°C	TO-99	MDP0004
EL2003CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2003H	−55°C to +125°C	TO-99	MDP0004
EL2003H/883B	−55°C to +125°C	TO-99	MDP0004
EL2003J	−55°C to +125°C	CerDIP	MDP0010
EL2003J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2003L	−55°C to +125°C	20-PAD LCC	MDP0007
EL2003L/883B	−55°C to +125°C	20-PAD LCC	MDP0007
EL2033CN	0°C to +75°C	P-DIP	MDP0031
EL2033CJ	0°C to +75°C	CerDIP	MDP0010
EL2033J	−55°C to +125°C	CerDIP	MDP0010
EL2033J/883B	−55°C to +125°C	CerDIP	MDP0010

General Description

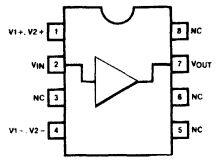
The EL2003/EL2033 are general purpose monolithic unity gain buffers featuring 100 MHz, −3 dB bandwidth and 4 ns small signal rise time. These buffers are capable of delivering a ±100 mA current to a resistive load and are oscillation free into capacitive loads. In addition, the EL2003/EL2033 have internal output short circuit current limiting which will protect the devices under both a DC fault condition and AC operation with reactive loads. The extremely fast slew rate of 1200 V/μs, wide bandwidth, and high output drive make the EL2003/EL2033 ideal choices for closed loop buffer applications with wide band op amps. These same characteristics and excellent DC performance make the EL2003/EL2033 excellent choices for open loop applications such as driving coaxial and twisted pair cables.

The EL2003/EL2033 are constructed using Elantec's proprietary dielectric isolation process that produces PNP and NPN transistors with essentially identical AC and DC characteristics.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

EL2003, N, J Packages



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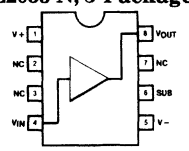
Top View

EL2033 N, J Packages



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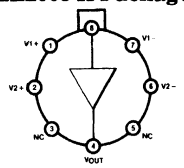
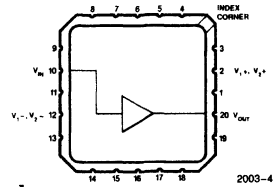
Top View

EL2003 H Package



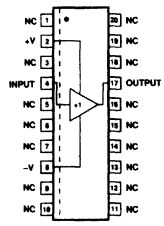
2003-3

EL2003 L Package



2003-4

EL2003 M Package



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Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage (Note 1)	±15V or V_S		Metal Can, CerDIP	175°C
I_{IN}	Input Current (Note 1)	±50 mA		Plastic	150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
	Output Short Circuit			Lead Temperature	
	Duration (Note 3)	Continuous		(Soldering, <10 seconds)	300°C
T_A	Operating Temperature Range				
	EL2003/2033	−55°C to +125°C			
	EL2003C/2033C	0°C to +75°C			

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω

Parameter	Description	Test Conditions			Limits			Test Level		Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003 2033	2003C 2033C	
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	5	40	I	I	mV
				T_{MIN}, T_{MAX}	−50		50	I	III	mV
I_{IN}	Input Current	0	∞	25°C, T_{MAX}	−25	−5	25	I	II	μA
				T_{MIN}	−50		50	I	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°C, T_{MAX}	1	2		I	II	MΩ
				T_{MIN}	0.1			I	III	MΩ
A_{V1}	Voltage Gain	±12V	1 kΩ	25°C	0.98	0.99		I	I	V/V
				T_{MIN}, T_{MAX}	0.97			I	III	V/V
A_{V2}	Voltage Gain	±6V	50Ω	25°C	0.83	0.90		I	I	V/V
				T_{MIN}, T_{MAX}	0.80			I	III	V/V
A_{V3}	Voltage Gain with V_S = ±5V	±3V	50Ω	25°C	0.82	0.89		I	I	V/V
				T_{MIN}, T_{MAX}	0.79			I	III	V/V
V_{O1}	Output Voltage Swing	±14V	1 kΩ	25°C	±13	±13.5		I	I	V
				T_{MIN}, T_{MAX}	±12.5			I	III	V
V_{O2}	Output Voltage Swing	±12V	100Ω	25°C	±10.5	±11.3		I	I	V
				T_{MIN}, T_{MAX}	±10			I	III	V

EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Electrical Characteristics $V_S = \pm 15V, R_S = 50\Omega$ — Contd.

Parameter	Description	Test Conditions			Limits			Test Level		Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003 2033	2003C 2033C	
R_{OUT}	Output Resistance	±2V	50Ω	25°C		7	10	I	I	Ω
				T_{MIN}, T_{MAX}			12	I	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±105	±230		I	I	mA
				T_{MIN}, T_{MAX}	±100			I	III	mA
I_S	Supply Current	0	∞	25°C, T_{MAX}		10	15	I	II	mA
				T_{MIN}			20	I	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	80		I	I	dB
				T_{MIN}, T_{MAX}	50			I	III	dB
SR1	Slew Rate, (Note 6)	±10V	1 kΩ	25°C	600	1200		I	I	V/μs
SR2	Slew Rate, (Note 7)	±5V	50Ω	25°C	200	400		I	I	V/μs
THD	Distortion @ 1 kHz	4 V_{rms}	50Ω	25°C		0.2	1	I	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

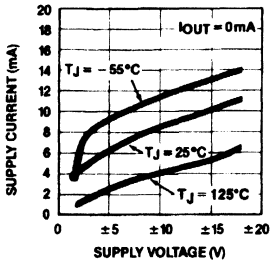
Note 5: $V_S = \pm 4.5V$ to ±18V.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and −5V.

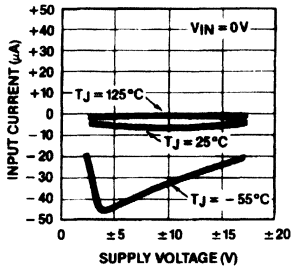
Note 7: Slew rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

Typical Performance Curves

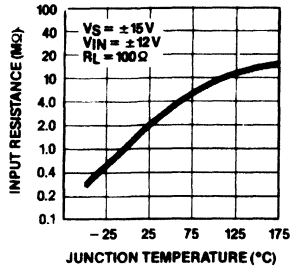
Quiescent Supply Current vs Supply Voltage



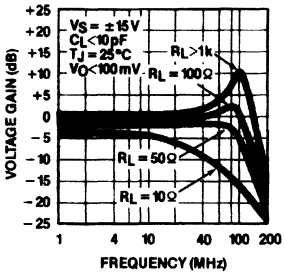
Input Current vs Supply Voltage



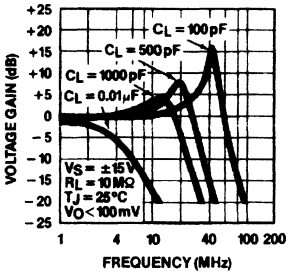
Input Resistance vs Temperature



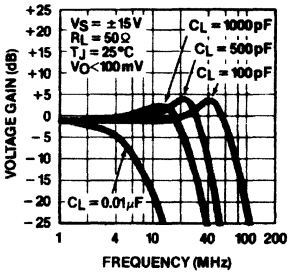
Voltage Gain vs Frequency Various Resistive Loads



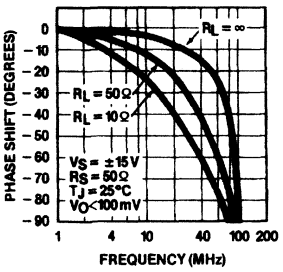
Voltage Gain vs Frequency No Resistive Load Various Capacitive Loads



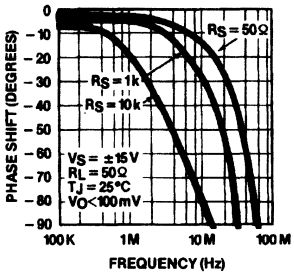
Voltage Gain vs Frequency 50Ω Resistive Load Various Capacitive Loads



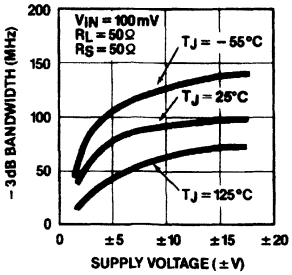
Phase Shift vs Frequency Various Resistive Loads



Phase Shift vs Frequency Various Source Resistors



−3 dB Bandwidth vs Supply Voltage



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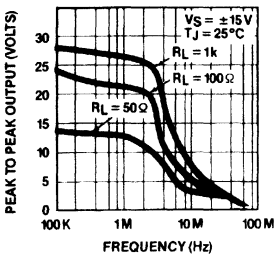
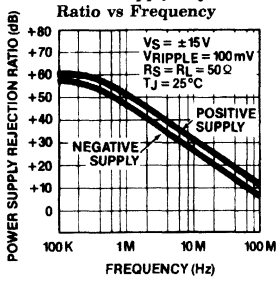
EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Typical Performance Curves — Contd.

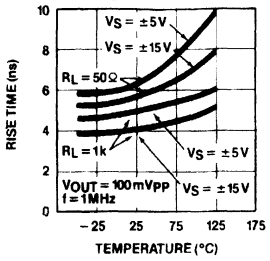
Maximum Undistorted Output Voltage vs Frequency



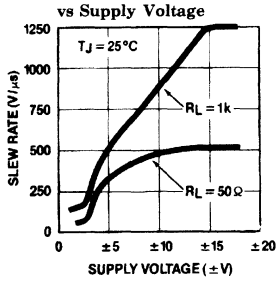
Power Supply Rejection Ratio vs Frequency



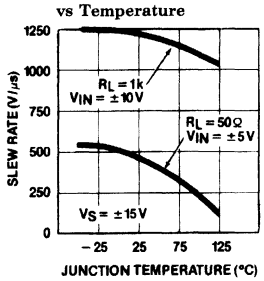
Rise Time vs Temperature



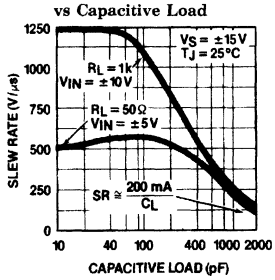
Slew Rate vs Supply Voltage



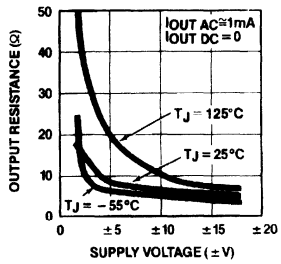
Slew Rate vs Temperature



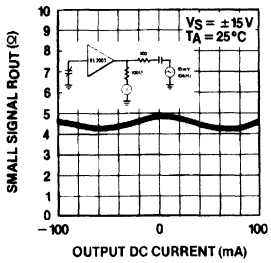
Slew Rate vs Capacitive Load



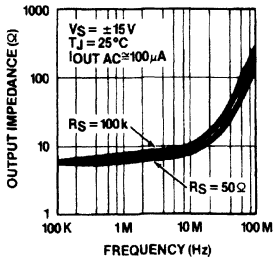
Output Resistance vs Supply Voltage



Small Signal Output Resistance vs DC Output Current



Output Impedance vs Frequency



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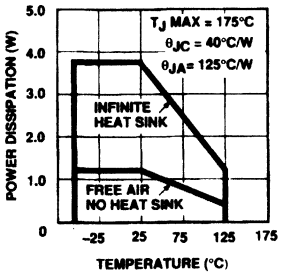
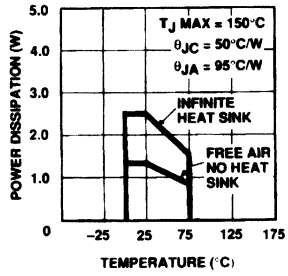
Typical Performance Curves — Contd.

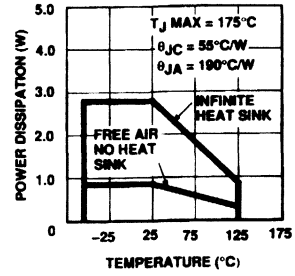
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



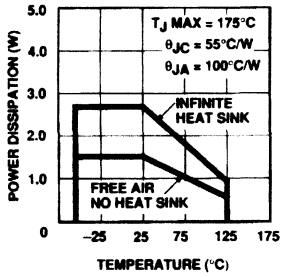
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



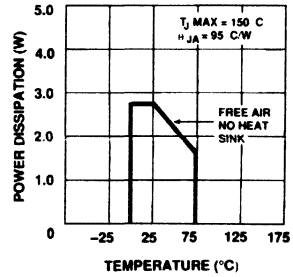
8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



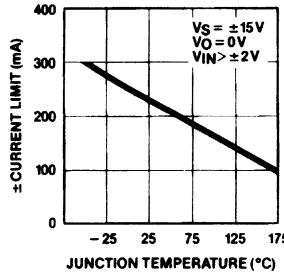
20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



Current Limit vs Temperature



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EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Applications Hints

The EL2003/EL2033 are monolithic buffer amplifiers built with Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The circuits are connection of symmetrical common collector transistors that provide both sink and source current capability independent of output voltage while maintaining constant output and input impedances. The high slew rate and wide bandwidth of the EL2003 and EL2033 make them useful beyond video frequencies.

Power Supplies

The EL2003/EL2033 may be operated with single or split supplies as low as ±2.5V (5V total) to as high as ±18V (36V total). However, the bandwidth, slew rate and output impedance degrade significantly for supply voltages less than ±5V (10V total) as shown in the characteristic curves. It is not necessary to use equal value split supplies, for example −5V and +12V would be excellent for 0V to 1V video signals.

Bypass capacitors from each supply pin to a ground plane are recommended. The EL2003/EL2033 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate a supply ringing and the interference it can cause, a 10 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rates and longer settling times.

The EL2003 metal can package has the collectors of the output transistors brought out separately from the input supplies for pin compatibility with the ELH0002H. If the collectors operate on lower supplies than the input stage, the internal power dissipation can be reduced. However, the output transistors can be driven into hard saturation when the input voltage exceeds the collector supply voltage. The recovery time to come out of saturation will be 2 μs or 3 μs and the output may oscillate during this recovery period.

Input Range

The input to the EL2003/EL2033 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit. However, there are clamp diodes from the input to the output that protect the transistor base emitter junctions. These diodes start to conduct at about ±9.5V input to output differential voltage. Of course the input resistance drops dramatically when the diodes start conducting; the diodes are rated at ±50 mA.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However, if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2003/EL2033 have excellent input-output isolation and are very tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources can cause oscillations; a 1 kΩ resistor in series with the buffer input lead will usually eliminate problems without sacrificing too much speed. An unterminated cable or other resonant source can also cause oscillations. Again, an isolating resistor will eliminate the problem.

Current Limit

The EL2003/EL2033 have internal current limits that protect the output transistors. The current limit goes down with junction temperature rise as shown in the characteristic curves. At a junction temperature of +175°C the current limits are at about 100 mA. If the EL2003 or EL2033 output is shorted to ground when operating on ±15V supplies, the power dissipation will be greater than 1.5W. A heat sink is required in order for the EL2003 or EL2033 to survive an indefinite short. Recovery time to come out of current limit is about 250 ns.

Applications Hints — Contd.

Heat Sinking

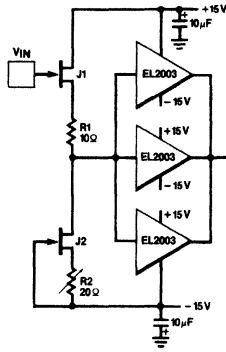
When operating the EL2003/EL2033 in elevated ambient temperatures and/or high supply voltages and low impedance loads, the internal power dissipation can force the junction temperature above the maximum rating (175°C for the metal can package and 150°C for the plastic DIP). Also, an indefinite short of the output to ground will cause excessive power dissipation.

The thermal resistance junction to case is 45°C per Watt for the metal can package and 50°C/W for the plastic DIP. A suitable heat sink will increase the power dissipation capability significantly beyond that of the package alone. Several companies make standard heat sinks for both packages. Aavid and Thermalloy heat sinks have been used successfully.

Parallel Operation

If more than 100 mA output is required or if heat management is a problem, several EL2003s or EL2033s may be paralleled together. The result is as though each device was driving only part of the load. For example, if two units are paralleled then a 50Ω load looks like 100Ω to each EL2003. Parallel operation results in lower input and output impedances, increased bias current but no increase in offset voltage. An example showing three EL2003s in parallel and also the addition of a FET input buffer stage is shown below. By using a dual FET the circuit complexity is minimal and the performance is excellent. Take care to minimize the stray capacitance at the input of the EL2003s for maximum slew rate and bandwidth.

FET Input Buffer with High Output Currents



Parallel Operation
$I_{OUT} \geq \pm 300$ mA
$R_{OUT} \cong 2\Omega$
BW ≅ 100 MHz
SR = 1000 V/µs

J1, J2 2N5911 Dual FET
R1, R2 Offset Adjust

2003-9

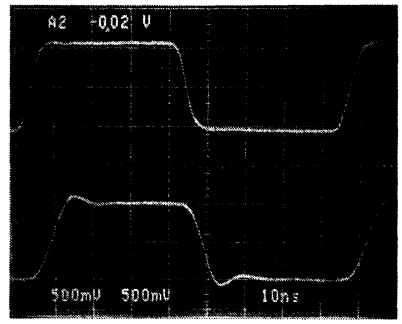
Resistive Loads

The DC gain of the EL2003/EL2033 is the product of the unloaded gain (0.995) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.995 * R_L/(R_L + R_{OUT})$$

The high frequency response of the EL2003/EL2033 varies with the value of the load resistance as shown in the characteristic curves. If the 100 MHz peaking is undesirable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from the output to ground. The snubber circuit works by presenting a high frequency load resistance of less than 50Ω while having no loading effect at low frequencies.

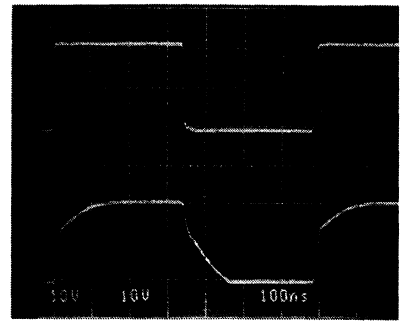
Small Signal Response



$R_L = 50\Omega$, $C_L = 10$ pF, $V_S = \pm 15$V
Top is V_{IN}, Bottom is V_{OUT}

2003-10

Large Signal Response



$R_L = 100\Omega$, $C_L = 10$ pF, $V_S = \pm 15$V
Top is V_{IN}, Bottom is V_{OUT}

2003-11

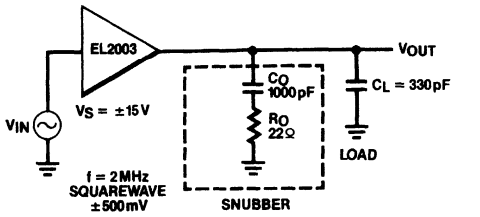
EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Applications Hints — Contd.

Capacitive Loads

The EL2003/EL2033 are stable driving any type of capacitive load. However, when driving a pure capacitance of less than a thousand picofarads the frequency response has excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and will ring for several hundred ns.

If the peaking and ringing cause system problems they can be eliminated with an RC snubber circuit from the output to ground. The values can be found empirically by observing a squarewave or the frequency response. First just put the resistor alone from output to ground until the desired response is obtained. Of course the gain will be reduced due to R_{OUT}. Then put capacitance in series with the resistor to restore the gain at low frequencies. Start with a small capacitor and increase until the response is optimum. Too large a capacitor will roll the gain off prematurely and result in a longer settling time. The figure below shows an example of an EL2003 driving a 330 pF load, which is similar to the input of a flash converter.



2003-12

Driving a Pure Capacitance

Top Trace is without Snubber.
Bottom Trace is with Snubber Circuit.

2003-13

Inductive Loads

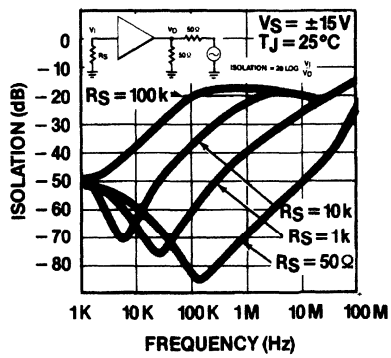
The EL2003/EL2033 can drive small motors, solenoids, LDT's and other inductive loads. Foldback current limiting is NOT used in the EL2003 or EL2033 and current limiting into an inductive load does NOT in and of itself cause spikes or kickbacks. However, if the EL2003 or EL2033 is in current limit and the input voltage is changing quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltage. Motors are also able to generate kickbacks when the EL2003 or EL2033 is in current limit.

To prevent damage to the EL2003/EL2033 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Reverse Isolation

The EL2003/EL2033 have excellent output to input isolation over a wide frequency range. This characteristic is very important when the buffer is used to drive signals between different equipment over cables. Often the cable is not perfect or the termination is improper and reflections occur that act like a signal source at the output of the buffer. Worst case the cable is connected to a source instead of where it is supposed to go. In both situations the buffer must keep these signals from its input. The following curve shows the reverse isolation of the EL2003/EL2033 verses frequency for various source resistors.

Reverse Isolation vs. Frequency



2003-14

Applications Hints — Contd.

Driving Cables

There are at least three ways to use the EL2003 and EL2033 to drive cables, as shown in the adjacent figure. The most obvious is to directly connect the cable to the output of the buffer. This results in a gain determined by the output resistance of the EL2003 or EL2033 and the characteristic impedance of the cable, assuming it is properly terminated. For RG-58 into 50Ω the gain is about −1 dB, exclusive of cable losses. For optimum response and minimum reflections it is important for the cable to be properly terminated.

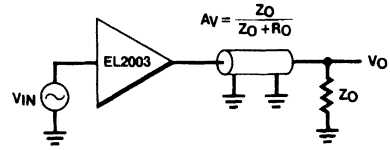
Double termination of a cable is the cleanest way to drive it since reflections are absorbed on both ends of the cable. The cable source resistor is equal to the characteristic impedance of the cable less the output resistance of the EL2003/EL2033. The gain is −6 dB exclusive of the cable attenuation.

Back matching is the last and most interesting way to drive a cable. The cable source resistor is again the characteristic impedance less the output resistance of the EL2003/EL2033; the termination resistance is now much greater than the cable impedance. The gain is 0 dB and DC levels waste no power.

An additional EL2033 or EL2033 make a good receiver at the terminating end. Because an unterminated cable looks like a resonant circuit, the receiving EL2003 or EL2033 should have an isolating resistor in series with its input to prevent oscillations when the cable is not connected to the driver. Of course if the cable is always connected to the back match, no resistor is necessary.

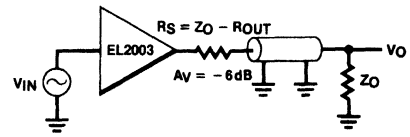
WARNING: ONE END OF A CABLE MUST BE PROPERLY TERMINATED. If neither end is terminated in the cable characteristic impedance, the cable will have standing waves that appear as resonances in the frequency response. The resonant frequencies are a function of the cable length and even relatively short cables can cause problems at frequencies as low as 1 MHz. Longer cables should be terminated on both ends.

Direct Drive



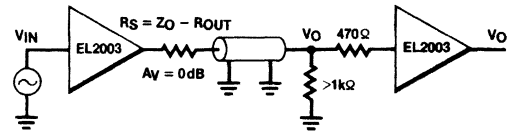
2003-15

Double Matched



2003-16

Back Matched

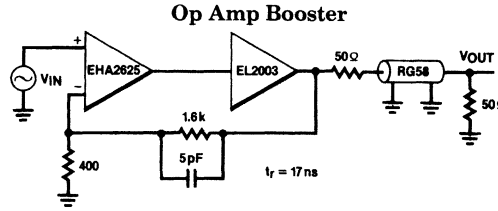


2003-17

Op Amp Booster

The EL2003 or EL2033 can boost the output drive of almost any monolithic op amp. Because the phase shift in the EL2003/EL2033 is low at the op amp's unity gain frequency, no additional compensation is required. By following an op amp with an EL2003 or EL2033, the buffered op amp can drive cables and other low impedance loads directly. Even decompensated high speed op amps can take advantage of the EL2003's or EL2033's 100 mA drive.

Op Amp Booster



2003-18

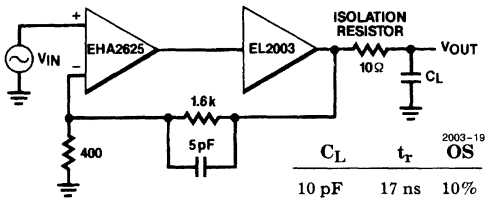
EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Applications Hints — Contd.

Driving capacitive loads with any closed loop amplifier creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The output impedance of the EL2003 or EL2033 is less than 10Ω from DC to about 10 MHz, but a capacitive load of 1000 pF will generate about 45 degrees phase shift at 10 MHz and make high speed op amps unstable. Obviously more capacitance will cause the same problem but at lower frequencies, and slower op amps as well would become unstable.

The easiest way to drive capacitive loads is to isolate them from the feedback with a series resistor. Ten to twenty ohms is usually enough but the final value depends on the op amp used and the range of load capacitance.

Op Amp Booster with Capacitive Load



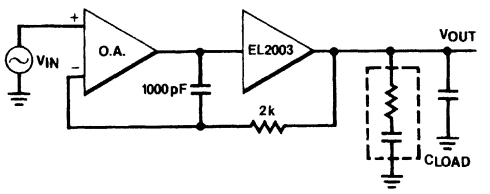
2003-19

C_L	t_T	OS
10 pF	17 ns	10%
470 pF	20 ns	50%
0.001 μF	30 ns	35%
0.005 μF	80 ns	0
0.01 μF	220 ns	0
0.05 μF	1.1 μs	0
0.1 μF	2.2 μs	0

10Ω is enough isolation and speed is determined by the isolation resistor and capacitive load time constant.

If the system requirements will not tolerate the isolation resistor, then additional high frequency feedback from the op amp output (the buffer input) and an isolating resistor from the buffer output is required. This requires that the op amp be unity gain stable.

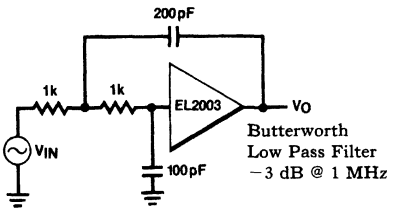
Complex Feedback with the Buffer to Drive Capacitive Loads



2003-20

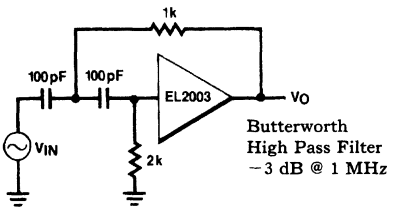
This works with any unity gain stable OA. Snubber Circuit (51Ω 470 pF) is optional.

Typical Applications



Butterworth Low Pass Filter −3 dB @ 1 MHz

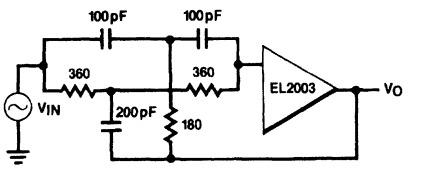
2003-21



Butterworth High Pass Filter −3 dB @ 1 MHz

2003-22

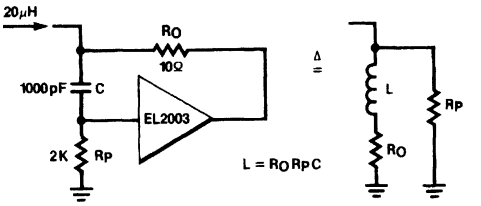
High Q Notch Filter



2003-23

$$f_O = \frac{1}{2\pi\,(100\text{ pF})\,(360)} \approx 4.4\text{ MHz}$$

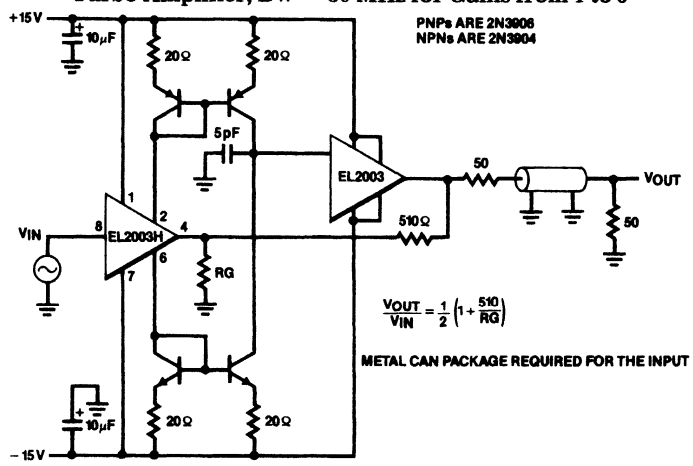
Simulated Inductor



2003-24

Typical Applications — Contd.

Turbo Amplifier, BW = 30 MHz for Gains from 1 to 5

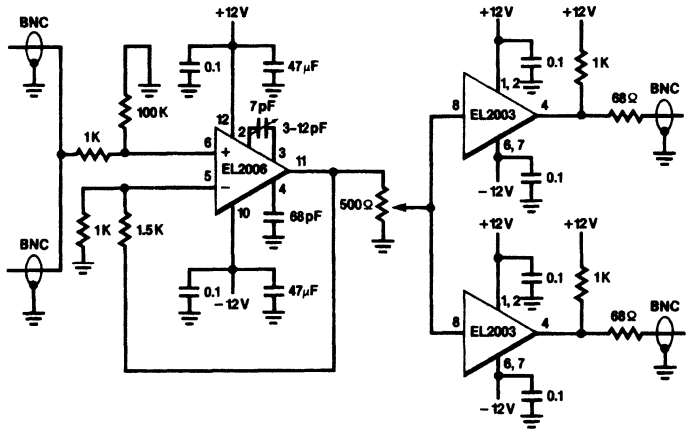


2003-25

Video Distribution Amplifier

In this broadcast quality circuit, the EL2006 FET input amplifier provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The EL2006 provides a voltage gain of 2.5 while the potentiometer allows the overall gain to be adjusted to drive the standard signal levels into the back matched 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated. The 1k pull up resistors reduce the differential gain error from 0.15% to less than 0.1%.

Video Distribution Amplifier

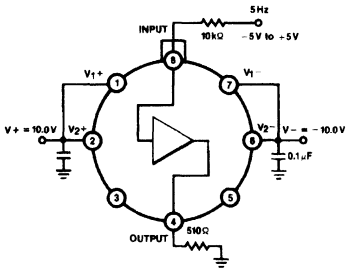


2003-26

EL2003/2003C/2033/2033C
100 MHz Video Line Driver

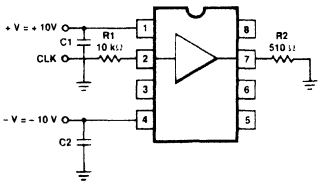
Burn-In Circuits

EL2003 Metal Can



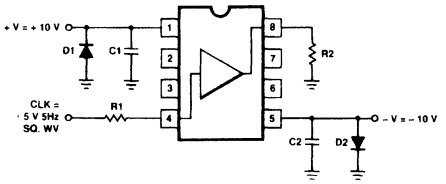
2003-27

EL2003 DIP



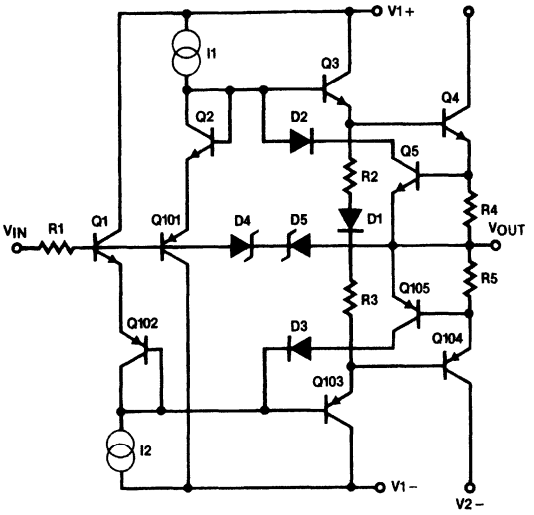
2003-28

EL2033 DIP



2003-29

Simplified Schematic



2003-30

EL2004/EL2004C
350 MHz FET Buffer

Features

- Slew rate—2500 V/μs
- Rise time—1 ns
- Bandwidth—350 MHz
- ELH0033—pin compatible
- ±5 to ±15V operation
- 100 mA output current
- MIL-STD-883B Rev. C devices manufactured in U.S.A.

Applications

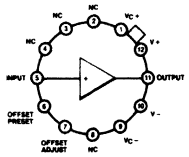
- Coaxial cable driver
- Fast op amp booster
- Flash converter driver
- Video line driver
- High-speed sample and hold
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2004CG	−25°C to +85°C	TO-8	MDP0002
EL2004G	−55°C to +125°C	TO-8	MDP0002
EL2004G/883B	−55°C to +125°C	TO-8	MDP0002
EL2004L	−55°C to +125°C	52-Pad LCC	MDP0013
EL2004L/883B	−55°C to +125°C	52-Pad LCC	MDP0013

Connection Diagrams

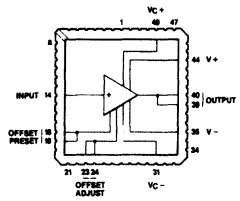
Case is Electrically Isolated



2004-1

Top View

L Package



2004-2

Top View

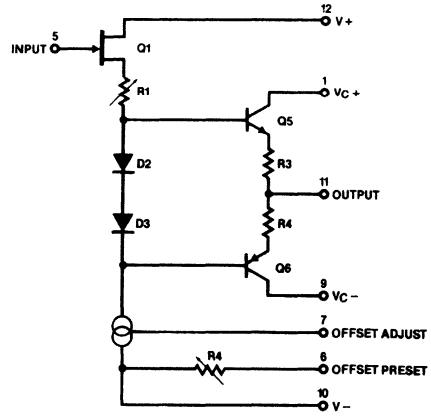
General Description

The EL2004 is a very high-speed, FET input buffer/line driver designed for unity gain applications at both high current (up to 100 mA) and at frequencies up to 350 MHz. The 2500 V/μs slew rate and wide bandwidth ensures the stability of the circuit when the EL2004 is used inside op amp feedback loops.

Applications for the EL2004 include line drivers, video buffers, wideband instrumentation, and high-speed drivers for inductive and capacitive loads. The performance of the EL2004 makes it an ideal buffer for video applications including input buffers for flash A/D converters, and output buffers for video DACs. Its excellent phase linearity is particularly advantageous in digital signal processing applications.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



2004-3

EL2004/EL2004C
350 MHz FET Buffer

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		EL2004	−55°C to +125°C
P_D	Power Dissipation (See curves)	1.5W		EL2004C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

±15V DC Electrical Characteristics

V_S = ±15V, $T_{MIN} < T_A < T_{MAX}$, V_{IN} = 0V, R_L = 1 kΩ unless otherwise specified (Note 1)

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le 100$ kΩ, T_J = 25°C		5	10	I		12	20	I	mV
		$R_S \le 100$ kΩ			15	I			25	III	mV
A_V	Voltage Gain	V_{IN} = ±10V	0.97	0.98	1.0	I	0.96	0.98	1.0	II	V/V
		R_L = 100Ω, V_{IN} = ±10V	0.92	0.95	0.98	I	0.90	0.95	0.98	II	V/V
R_{IN}	Input Impedance	T_J = 25°C, V_{IN} = ±1V	10^8	10^{11}		I	10^8	10^{11}		I	Ω
R_{OUT}	Output Impedance	V_{IN} = ±1 V_{DC}, ΔR_L = 100Ω to Infinity		4	8	I		4	10	II	Ω
V_O	Output Voltage Swing	V_{IN} = ±14V	±12	±13		I	±12	±13		II	V
		V_{IN} = ±10.5V, R_L = 100Ω T_A = 25°C	±9	±9.8		I	±9	±9.8		I	V
I_{IN}	Input Current	T_J = 25°C (Note 2)			0.25	I			2.0	I	nA
		T_A = 25°C (Note 3)			2.5	IV			20	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			50	III	nA
		V_{IN} = −10V		20		V		20		V	nA
I_S	Supply Current			20	24	I		20	24	II	mA

±5V DC Electrical Characteristics

$V_S = \pm 5V$, $T_{MIN} < T_A < T_{MAX}$, $V_{IN} = 0V$, $R_L = 50\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \leq 100\ k\Omega$, $T_J = 25°C$		10	30	I		10	30	I	mV
		$R_S \leq 100\ k\Omega$			35	I			35	III	mV
A_V	Voltage Gain	$V_{IN} = \pm 1V$, $R_L = 1\ k\Omega$	0.90	0.95	1.0	I	0.90	0.95	1.0	II	V/V
		$V_{IN} = \pm 1V$	0.80	0.88	0.95	I	0.80	0.88	0.95	II	V/V
R_{IN}	Input Impedance	$T_J = 25°C$, $V_{IN} = \pm 1V$	10^8	10^{11}		I	10^{10}	10^{11}		I	Ω
R_{OUT}	Output Impedance	$V_{IN} = \pm 1\ V_{DC}$, $\Delta R_L = 50\Omega$ to Infinity		4	8	I		4	10	II	Ω
V_O	Output Voltage Swing	$V_{IN} = \pm 4V$	±2.0	±2.9		I	±2.0	±2.9		III	V
I_{IN}	Input Current	$T_J = 25°C$ (Note 2)			250	I			500	I	pA
		$T_A = 25°C$ (Note 3)			2.5	IV			5	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			20	III	nA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$, $R_L = 1\ k\Omega$		60		V		60		V	dB
I_S	Supply Current	$R_L = 1\ k\Omega$		17.5	20	I		17.5	20	II	mA

Note 1: When operating at elevated temperatures the power dissipation of the EL2004 must be limited to the values shown in the typical performance curve "Maximum Power Dissipation vs Temperature". Junction to case thermal resistance is 31°C/W when dissipation is spread among the transistors in a normal AC steady-state condition. In special conditions where heat is concentrated in one output device, junction temperature should be calculated using a thermal resistance of 70°C/W.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperatures may rise 40°C to 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_{IN} will change significantly during warm-up. Refer to I_{IN} vs Temperature graph for expected values.

Note 3: Measured in still air seven minutes after application of power. See graph of Input Current During Warm-up for further information.

Note 4: Bandwidth is calculated from the rise time. The EL2004 has a single pole gain and phase response up to the −3 dB frequency.

Note 5: Slew rate is measured between $V_{OUT} = +2.5V$ and $-2.5V$ for this test.

Note 6: Slew rate is measured between $V_{OUT} = +1V$ and $-1V$ for this test. Pulse repetition rate is <50 MHz.

±15V AC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 1\ k\Omega$, $R_S = 50\Omega$, $T_J = 25°C$ unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
BW	Bandwidth	(Note 4)	200	350		I	200	350		I	MHz
		$R_L = 50\Omega$	140	200		I	140	200		I	MHz
t_s	Settling Time to 1%	$\Delta V_{IN} = 1V$, $t_r = 3\ ns$		6		V		6		V	ns
C_{in}	Input Capacitance			3		V		3		V	pF

EL2004/EL2004C
350 MHz FET Buffer

±15V AC Electrical Characteristics

V_S = ±15V, R_L = 1 kΩ, R_S = 50Ω, T_J = 25°C unless otherwise specified — Contd.

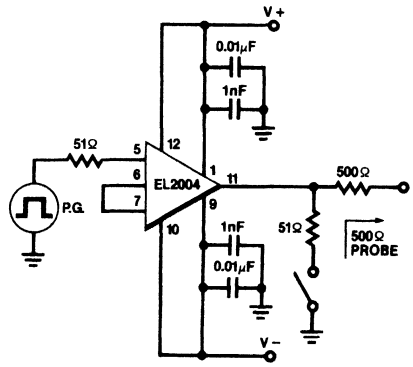
Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	V_{IN} = ±5V (Note 5)	2000	2500		I	2000	2500		I	V/µs
		C_L = 100 pF, V_{IN} = ±5V (Note 5)		1200		V		1200		V	V/µs
t_r	Rise Time Note: See Test Figure	ΔV_{IN} ∿ 0.6V		1.0	1.7	I		1.0	1.7	I	ns
		ΔV_{IN} ∿ 0.6V, R_L = 50Ω		1.7	2.5	I		1.7	2.5	I	ns
t_p	Propagation Delay Note: See Test Figure	ΔV_{IN} ∿ 0.6V		1.0	2.0	I		1.0	2.0	I	ns
R_{OUT}	Output Impedance	f = 1 MHz, V_{IN} = 1 V_{RMS} ΔR_L = 100Ω to Infinity		4		V		4		V	Ω
+PSRR	Power Supply Rejection Ratio	ΔV_S+ = ±1.5 V_{peak} f = 1 kHz		40		V		40		V	dB
−PSRR	Power Supply Rejection Ratio	ΔV_S− = ±1.5 V_{peak} f = 1 kHz		40		V		40		V	dB

±5V AC Electrical Characteristics

V_S = ±5V, R_L = 50Ω, R_S = 50Ω, T_J = 25°C unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
BW	Bandwidth	R_L = 1 kΩ	175	220		I	175	220		I	MHz
		(Note 4)	125	150		IV	125	150		IV	MHz
t_s	Settling Time to 1%	ΔV_{IN} = 1V, t_r = 3 ns		8		V		8		V	ns
C_{in}	Input Capacitance			3		V		3		V	pF
SR	Slew Rate	V_{IN} = ±2V (Note 6)	900	1200		I	900	1200		I	V/µs
		C_L = 100 pF, V_{IN} = ±2V R_L = 1 kΩ (Note 6)		500		V		500		V	V/µs
t_r	Rise Time Note: See Test Figure	R_L = 1 kΩ, ΔV_{IN} ∿ 0.6V		1.6	2.0	I		1.6	2.0	I	ns
		R_L = 50Ω, ΔV_{IN} ∿ 0.6V		2.3	2.8	IV		2.3	2.8	IV	ns
t_p	Propagation Delay Note: See Test Figure	R_L = 1 kΩ, ΔV_{IN} ∿ 0.6V		1.2	2.4	I		1.2	2.4	I	ns
R_{OUT}	Output Impedance	f = 1 MHz, V_{IN} = 1 V_{RMS} ΔR_L = 100Ω to Infinity		4		V		4		V	Ω
+PSRR	Power Supply Rejection Ratio	ΔV_S− = ±0.5 V_{peak} f = 1 kHz		30		V		30		V	dB
−PSRR	Power Supply Rejection Ratio	ΔV_S+ = ±0.5 V_{peak} f = 1 kHz		30		V		30		V	dB

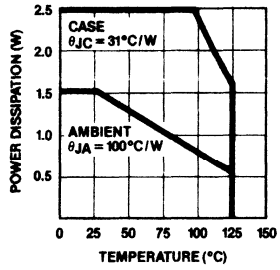
AC Test Circuit



2004-4

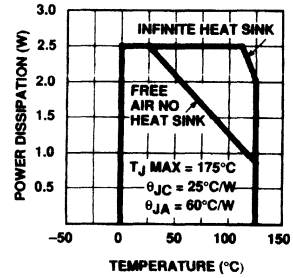
Typical Performance Curves

TO-8
Maximum Power
Dissipation



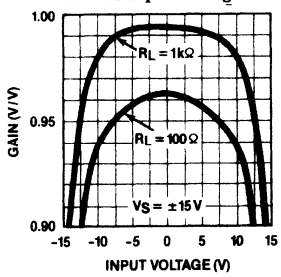
2004-5

52-Pad LCC
Maximum Power Dissipation
vs Ambient Temperature

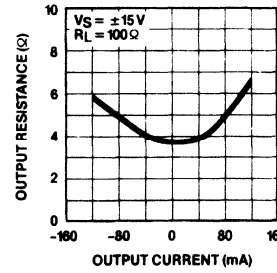


2004-6

Gain vs Input Voltage



Output Resistance vs
Output Current

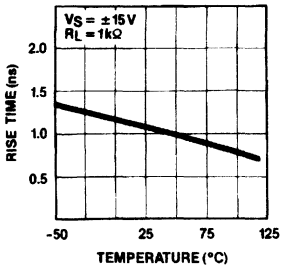


2004-7

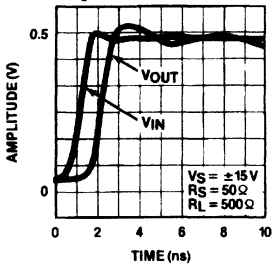
EL2004/EL2004C
350 MHz FET Buffer

Typical Performance Curves — Contd.

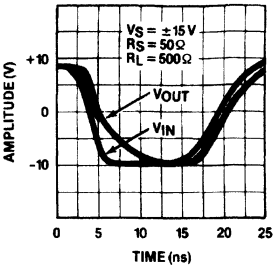
Rise Time vs Temperature



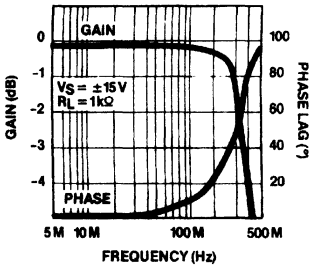
Small Signal Pulse Response



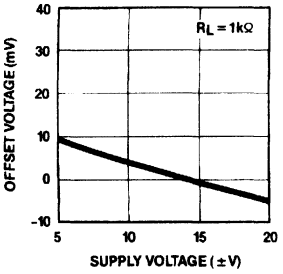
Large Signal Pulse Response



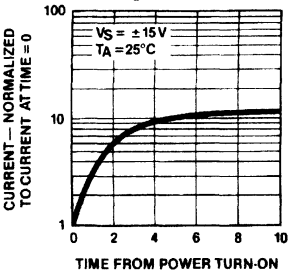
Frequency Response



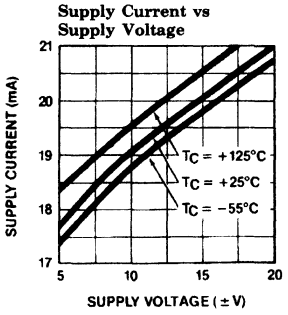
Offset Voltage vs Supply Voltage



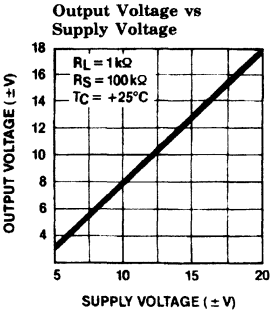
Normalized Input Bias Current During Warm-up



Supply Current vs Supply Voltage



Output Voltage vs Supply Voltage



2004-8

Applications Information

The EL2004 is one member of a family of high performance buffers manufactured by Elantec. The 2004 is optimized for speed while others offer choices of input DC parameters or output drive or cost. The following table illustrates those members available at the time of this printing. Consult the factory for the latest capabilities in this developing line.

Elantec's Buffer Family

Part #	Slew Rate V/μs	Bandwidth MHz	Input Current (Warm)	Peak I_{OUT} mA	Rise Time ns
ELH0002	200	50	6 μA	400	7
ELH0033	1500	100	2.5 nA	250	2.9
EL2004	2500	350	2.5 nA	250	1.0
EL2005	1500	140	0.1 nA	250	2.5

Recommended Layout Precautions

The very high-speed performance of the EL2004 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.1 μF or more should be connected with the shortest practical lead lengths between the device supply leads and a ground plane. In addition, it can be helpful to parallel these with 4.7 μF electrolytics (Tantalum preferred). Failure to follow these precautions can result in oscillation.

Circuit Operation

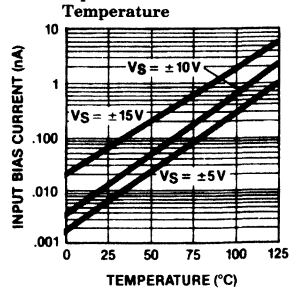
The EL2004 is effectively an ideal unity gain amplifier with almost infinite input impedance and about 6Ω output impedance.

Input Characteristics

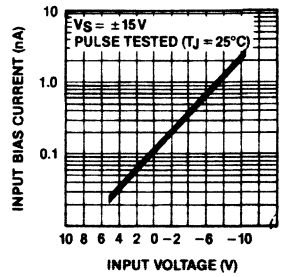
The input impedance of a junction FET is a strong function of temperature and input voltage. Nominal input resistance of EL2004 is 10^{12} at 25°C junction, but as I_B doubles every 11°C in the JFET, the input resistance falls. During warm-up, self-heating raises the junction temperature up to 60°C or more (without heatsink) so operating I_B will be much higher than the data sheet 25°C specification.

Another factor which can increase bias current is input voltage. If the input voltage is more than 20V below the positive supply, the input current rises exponentially. (See Curve.)

Input Bias Current vs Temperature



Input Bias Current vs Input Voltage



2004-9

In applications such as sample and hold circuits where it is important to maintain low input bias current over input voltage range, the EL2005 High Accuracy Fast Buffer is recommended.

The input capacitance of EL2004 comprises the FET device gate-to-source capacitance (which is a function of input voltage) and stray capacitance to the case. Effective input capacitance can be minimized by connecting the case to the output since it is electrically isolated. Or, for reduced radiation, the case may be grounded. The AC characteristics specified in this data sheet were obtained with the case floating.

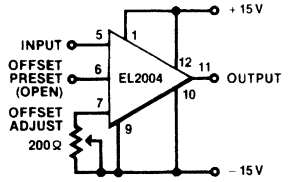
Offset Voltage Adjustment

The EL2004's offset voltages have been actively laser trimmed at ±15V supplies to meet specified limits when the offset adjust pin is shorted to the offset preset pin. If external offset null is required, the offset adjust pin should be connected to a 200Ω trim pot connected to the negative supply.

EL2004/EL2004C
350 MHz FET Buffer

Circuit Operation — Contd.

Offset Zero Adjust



2004-10

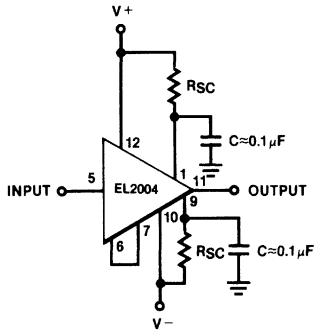
Capacitive Loading

The EL2004 is designed to drive capacitive loads up to several thousand picofarads without oscillation. However, peak current resulting from charging currents on fast edges should be limited below the absolute maximum peak current rating of 250 mA. In some cases it may be necessary to employ one of the current limit schemes shown below.

Short Circuit Protection

Dynamic response of the EL2004 was preserved by excluding current limit circuits which are not needed in most applications. However, in situations where operating conditions are not controlled, short circuit protection can be added by inserting resistors between the output device collectors and supplies as illustrated.

Using Resistor Current Limiting



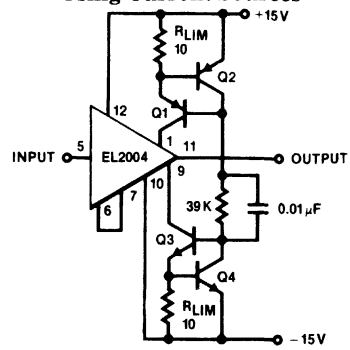
2004-11

Suitable resistor values can be calculated as follows:

$$R_{SC} = \frac{V+}{I_{SC}} = \frac{V-}{I_{SC}}$$

where $I_{SC} \leq 100$ mA for EL2004.

Current Limiting Using Current Sources



2004-12

The inclusion of limiting resistors in the collectors of the output devices will reduce the output voltage swing and speed. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses.

An alternate active current limit technique that retains full DC output swing is shown above. Here the current sources are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as the current source reaches its limit.

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{100\ mA} = 6\Omega$$

Power Supplies

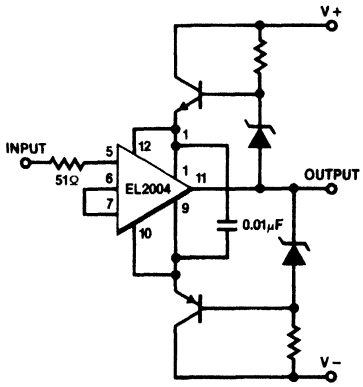
The EL2004 has been characterized for both ±15 and ±5V dual supply operation, but other combinations can also be useful. For example, in many video applications it is only necessary for the output to swing ±2V or less, but speed and distortion are important. In this situation, the input stage can be operated at the full ±15V supply while the output collectors are returned to ±5V. The speed and distortion will be almost as good as if the whole circuit was operating at ±15V, but the dissipation is substantially reduced and higher load currents can be safely accommodated.

Circuit Operation — Contd.

Increasing Operating Voltage and Reducing Thermal Tail

When driving heavy loads, the changing dissipation in the output transistors can sometimes cause temperature gradients in the circuit which cause a shift in offset voltage and the phenomenon known as "thermal tail". Bootstrapping the output as illustrated substantially reduces the power in the output transistors and mitigates the effect.

High Voltage Inputs can be Accommodated with Bootstrapped Supplies



2004-13

Hardware

In order to utilize the full drive capabilities of the EL2004, it should be mounted with a heatsink, particularly for extended temperature operation. Suitable heatsinks include Thermalloy 2240A (33°C/W), Wakefield 215CB (30°C/W) and IERC-UP-TO-848CB (15°C/W).

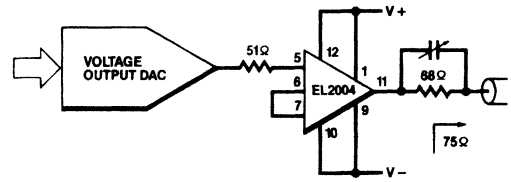
The case is isolated from the circuit and may be connected to system chassis. Sockets are not recommended as they add substantial inductance and capacitance which impair the performance of the device. However, for test purposes they are unavoidable and precautions such as shielding input from output are suggested.

General Application Suggestions

Video DAC Buffer

Many of the available video D to A converters are unable to directly drive 50Ω or 75Ω cables. The EL2004's excellent phase linearity at video frequencies make it an ideal solution. In critical applications or where line termination is not controlled, a matching pad should be used as shown. The capacitor should be adjusted for optimum pulse response. If properly layed out this circuit will not overshoot.

Video DAC Buffer

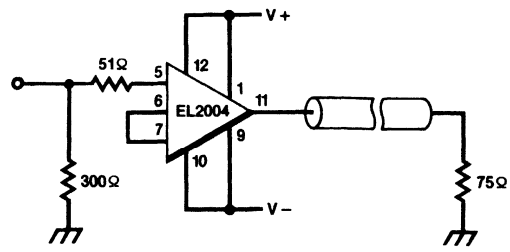


2004-14

Impedance Matching

The EL2004 provides power gain and isolation between source and load when used as an active tap or impedance matching device as illustrated here. In this example, there is no output matching pad between the 2004 and the 75Ω line. Such matching is not needed when the distant end of the cable is properly terminated as there is no reflected signal to worry about and the 2004 isolates the source. This technique allows the full output voltage of the EL2004 to be applied to the load.

Impedance Converter



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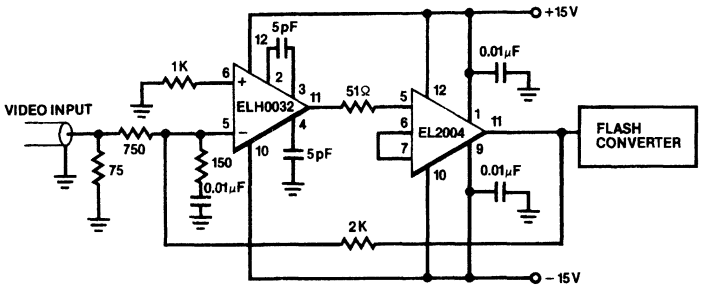
EL2004/EL2004C
350 MHz FET Buffer

General Application Suggestions — Contd.

Inverting Amplifier for 20 MHz Flash Converter

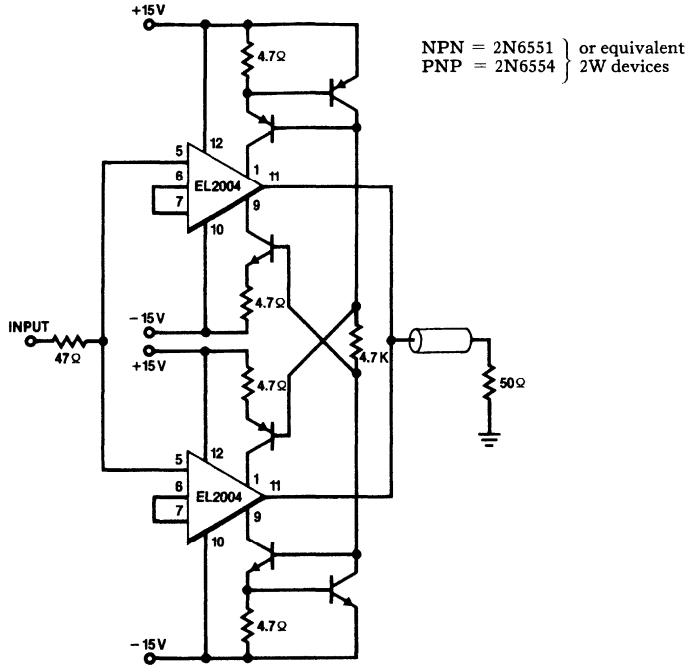


2004-16

Boosting the Output

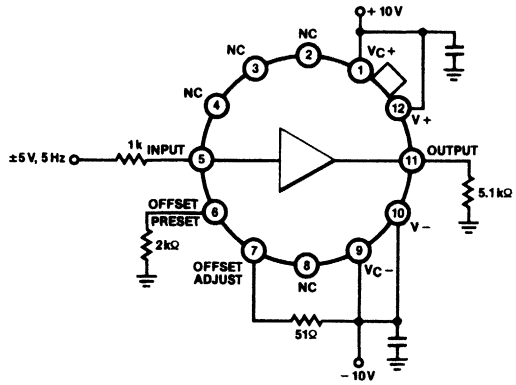
Unlike most integrated cicuits, two or more EL2004's can be paralleled for increased output drive. This capability results from the finite output resistance and low output mismatch of the EL2004. For example, a 50Ω cable driver with ±10V capability can be made by using two EL2004's. A short-circuit protected version is shown below.

50Ω Cable Driver with Short Circuit Protection



2004-17

Burn-In Circuit



Pin numbers are for TO-8 package.
LCC uses the same schematic.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2005/EL2005C
High Accuracy Fast Buffer

Features

- Low input current—50 pA
- Low offset and drift—2 mV/25 μV/°C
- High slew rate—1500 V/μs
- Fast rise and fall time—2.5 ns
- High input resistance—1000 GΩ
- Bandwidth—140 MHz
- Pin compatible with ELH0033
- MIL-STD-883 Revision C devices manufactured in U.S.A.

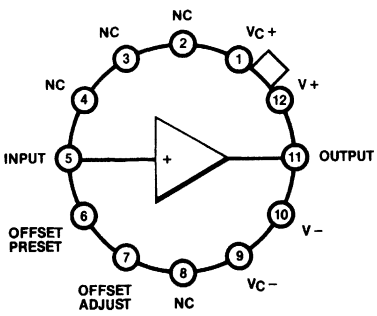
Advantages

- No input loading
- Input current independent of input voltage
- Eliminates offset adjustments
- Drives cables directly

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2005CG	−25°C to +85°C	TO-8	MDP0002
EL2005G	−55°C to +125°C	TO-8	MDP0002
EL2005G/883B	−55°C to +125°C	TO-8	MDP0002

Connection Diagram



Top View

Note: Case is electrically isolated.

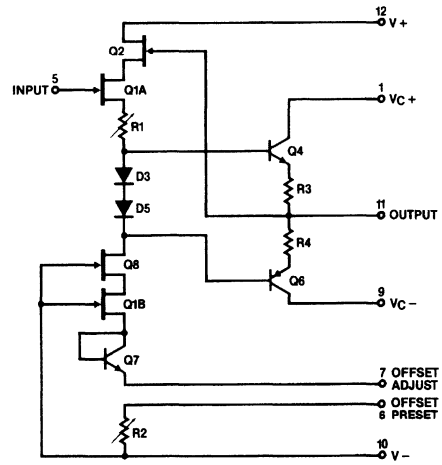
General Description

The EL2005 is a high-speed, FET input buffer similar to ELH0033 and EL2004 but with input specifications significantly improved over the previous types. The input stage employs a cascode configuration to maintain constant input characteristics over the full ±10V input range. The input looks like a 3 pF capacitor to ground in almost all cases since the DC bias current is constant with input voltage. In sample and hold circuits this results in an order of magnitude improvement in hold characteristics. Input offset voltage and offset voltage drift are also improved a factor of two over previous types.

These excellent DC characteristics are complemented by a wide 140 MHz bandwidth while the 1500 V/μs slew rate and excellent phase linearity of the ELH0033 family are preserved allowing direct plug-in replacement for upgraded performance. (For even faster operation see EL2004.)

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		EL2005	−55°C to +125°C
P_D	Power Dissipation (See curves)	1.5W		EL2005C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, V_{IN} = 0V, $T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le 100\ k\Omega$, T_J = 25°C (Note 1)		2	5	I		3	10	I	mV
		$R_S \le 100\ k\Omega$			10	I			15	III	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Offset Voltage	R_S = 100Ω		25		V		25		V	µV/°C
PSRR	Supply Rejection	±10V ≤ V_S ≤ ±20V	65	75		I	60	75		II	dB
I_B	Input Bias Current	T_J = 25°C (Notes 1 and 3)		2	50	I		5	100	I	pA
		T_A = 25°C (Notes 2 and 3)		50	500	IV		100	1000	IV	pA
		$T_J = T_A = T_{MAX}$		2	5	I		0.5	5	III	nA
A_V	Voltage Gain	R_S = 100Ω, R_L = 1 kΩ, V_{IN} = ±10V	0.97	0.98	1.0	I	0.96	0.98	1.0	II	V/V
		R_S = 100Ω, R_L = 100Ω, v_{IN} = ±10V	0.88	0.95	0.98	I	0.88	0.95	0.99	II	V/V
R_{IN}	Input Impedance	R_L = 1 kΩ, −10V ≤ V_{IN} ≤ ±10V	2×10^9	10^{12}		I	2×10^9	10^{12}		IV	Ω
		T_J = 25°C (Note 1), R_L = 1 kΩ	10^{10}	10^{12}		I	10^{10}	10^{12}		I	Ω
R_O	Output Impedance	R_L = 1 kΩ, V_{IN} = ±1V		4	8	I		4	9	II	Ω

EL2005/EL2005C
High Accuracy Fast Buffer

DC Electrical Characteristics $V_S = \pm 15V, V_{IN} = 0V, T_{MIN} \leq T_A \leq T_{MAX}$ — Contd.

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$, $R_L = 1\ k\Omega$		±12.5		V		±12.5		V	V
		$V_{IN} = \pm 10.5V, R_L = 100\Omega$, $T_A = 25°C$	±9	±9.8		I	±9	±9.8		I	V
I_S	Supply Current	$V_{IN} = 0$ (Note 1)		19	22	I		19	24	II	mA
PD	Power Consumption	$V_{IN} = 0$		570	660	I		570	720	II	mW

AC Electrical Characteristics $T_C = 25°C, V_S = \pm 15V, R_S = 50\Omega, R_L = 1\ k\Omega$

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	$V_{IN} = \pm 10V, V_{OUT} = \pm 5V$	1000	1500		III	1000	1500		III	V/μs
BW	Bandwidth	$V_{IN} = 1\ V_{rms}$		140		V		140		V	MHz
ϕ_{NL}	Phase Non-Linearity	BW = 1 MHz to 20 MHz		2		V		2		V	Degree
t_r	Rise Time	$\Delta V_{IN} = 0.5V$		2.5		V		2.5		V	ns
t_P	Propagation Delay	$\Delta V_{IN} = 0.5V$		1.0		V		1.0		V	ns
HD	Harmonic Distortion	f > 1 kHz		<0.1		V		<0.1		V	%
A_V	Voltage Gain	$R_S = 100\Omega, V_{IN} = 1\ V_{rms}$, f = 1 kHz	0.97	0.99	1.0	I	0.96	0.99	1.0	II	V/V
R_O	Output Impedance	$V_{IN} = 1\ V_{rms}$, f = 1 kHz		4	8	I		4	9	II	Ω

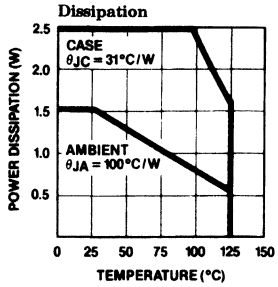
Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperatures may rise 40°C to 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs Temperature graph for expected values.

Note 2: Measured in still air seven minutes after application of power.

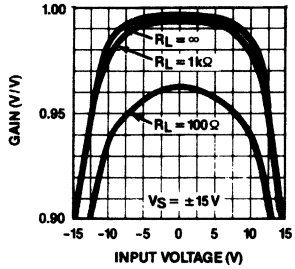
Note 3: Input bias current is guaranteed over the input range of $-10V \leq V_{IN} \leq +10V$.

Typical Performance Curves

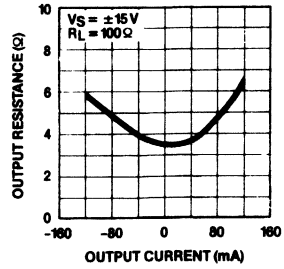
Maximum Power Dissipation



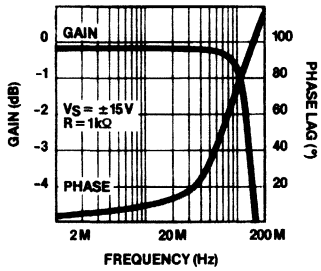
Gain vs Input Voltage



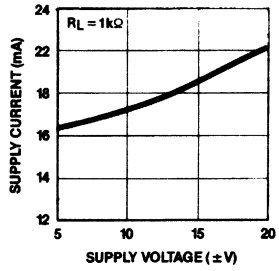
Output Resistance vs Output Current



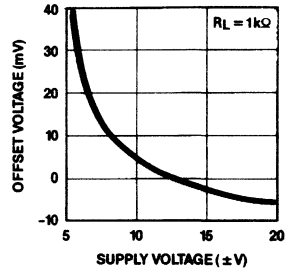
Frequency Response



Supply Current vs Supply Voltage

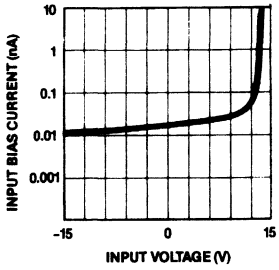


Offset Voltage vs Supply Voltage

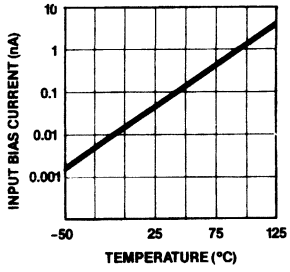


2005-3

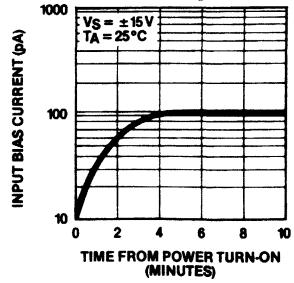
Input Bias Current vs Input Voltage



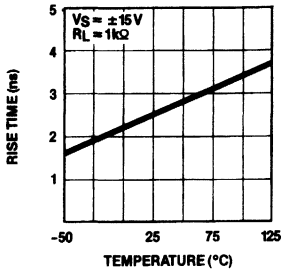
Input Bias Current vs Temperature



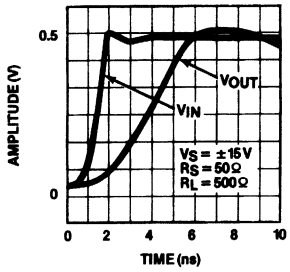
Input Bias Current During Warm-up



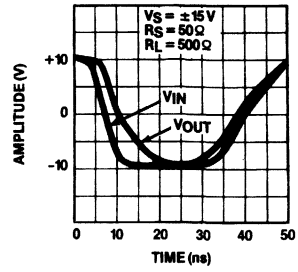
Rise Time vs Temperature



Small Signal Pulse Response



Large Signal Pulse Response

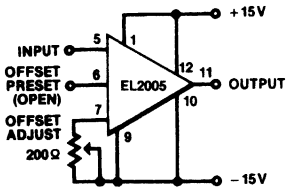


2005-4

EL2005/EL2005C
High Accuracy Fast Buffer

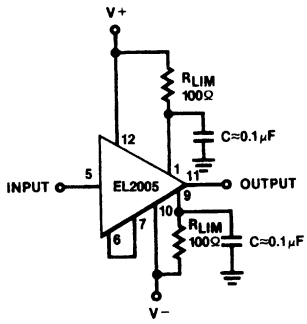
Typical Applications

Offset Zero Adjust



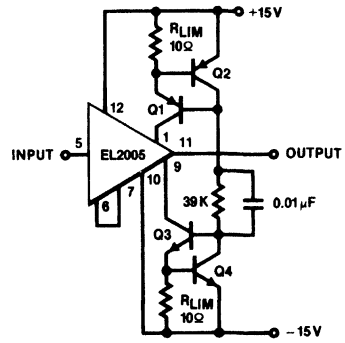
2005-5

Using Resistor Current Limiting



2005-6

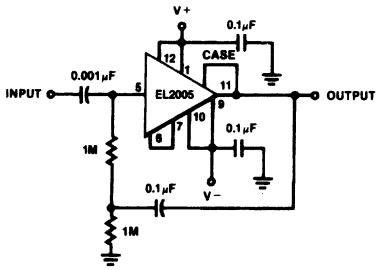
Current Limiting Using Current Sources



2005-7

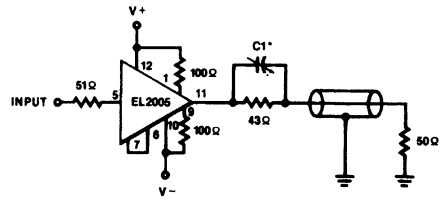
Q1 = Q2 = 2N2905
Q3 = Q4 = 2N2219

High Input Impedance AC Coupled Amplifier



2005-8

Coaxial Cable Driver

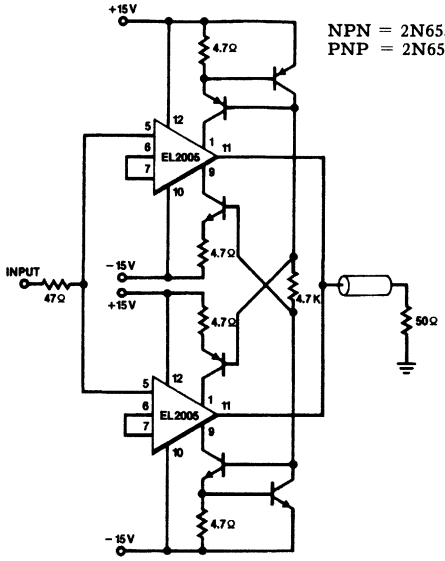


*Select C1 for optimum pulse response

2005-9

Typical Applications — Contd.

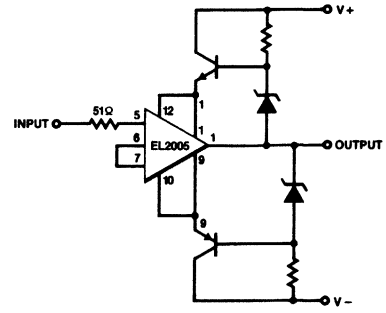
50Ω Cable Driver with Short Circuit Protection



NPN = 2N6551 } or equivalent
PNP = 2N6554 } 2W devices

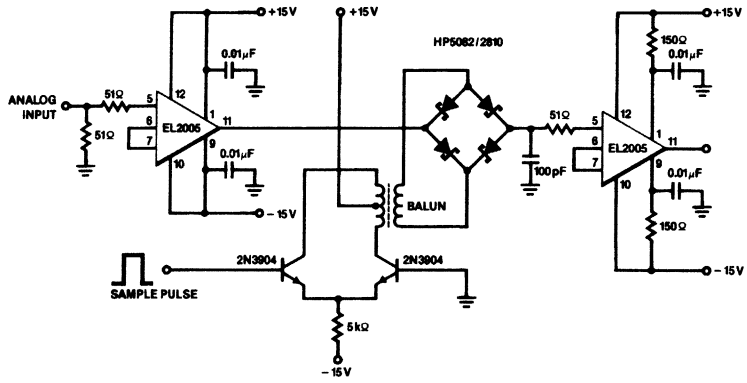
2005-10

Bootstrapped Supplies for High Voltage Applications



2005-11

High-Speed Sample and Hold



2005-12

EL2005/EL2005C
High Accuracy Fast Buffer

Applications Information

Recommended Layout Precautions

RF/video printed circuit board layout rules should be followed when using the EL2005 since it will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment

The EL2005's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. The pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 200Ω between the offset adjust pin and V− as illustrated on page 3-56.

Operation from Single or Asymmetrical Power Supplies

This device type may be readily used in applications where symmetrical supplies are unavailable or not desirable. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V+ - V-)}{2} = 0.005\,(V+ - V-)$$

where: A_V = No load voltage gain, typically 0.99
$V+$ = Positive supply voltage
$V-$ = Negative supply voltage

For example, with $V+ = +5V$ and $V- = -12V$, ΔV_O would be −35 mV. This may be adjusted to zero as described above.

Short Circuit Protection

In order to optimize transient response and output swing, output current limit has been omitted from the EL2005. Short circuit protection may be added by inserting appropriate value resistors between $V+$ and V_C+ pins and $V-$ and V_C- pins as shown on page 3-56.

Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V+}{I_{SC}} = \frac{V-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for EL2005

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing is also shown on page 3-56. In this circuit, the current sources are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

$$R_{LIM} \cong \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

Capacitive Loading

The EL2005 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (C × dV/dt) should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\frac{\Delta V_{IN}}{\Delta t} \times C_L \leq I_{OUT} \leq \pm 250\text{ mA}$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the total package power rating:

$$P_{DPkg} \geq P_{DC} + P_{AC}$$

$$P_{DPkg} \geq (V+ - V-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

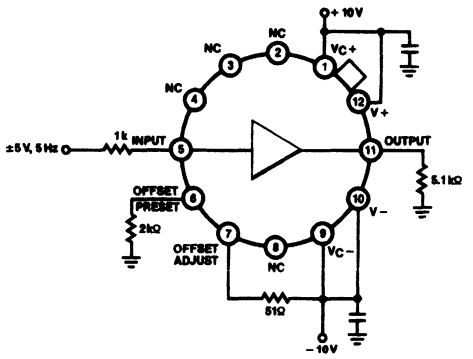
where: $V_{P\text{-}P}$ = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

Applications Information — Contd.

Operation within an Op Amp Loop

The EL2005 may be used as a current booster or isolation buffer within a closed loop with op amps such as the ELH0032 and HA2500 and HA2600 series. An isolation resistor of 47Ω should be used between the op amp output and the input of EL2005. The wide bandwidth and high slew rates of the EL2005 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Burn-In Circuit



Hardware

In order to utilize the full drive capabilities of the EL2005, it should be mounted with a heatsink, particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

IMPORTANT!

Power supply bypassing is necessary to prevent oscillation with the EL2005 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2008C
55 MHz 1 Amp Buffer Amplifier

Features

- High slew rate—2500 V/μs
- Wide bandwidth—
  100 MHz @ R_L = 50Ω
  55 MHz @ R_L = 10Ω
- Output current—1A continuous
- Output impedance—1Ω
- Quiescent current—13 mA
- Short circuit protected
- Over temperature protected
- Power package with isolated metal tab

Applications

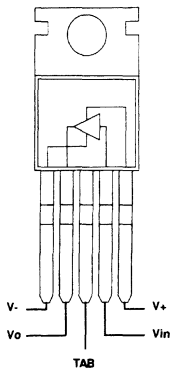
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2008CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



2008-1

Top View

General Description

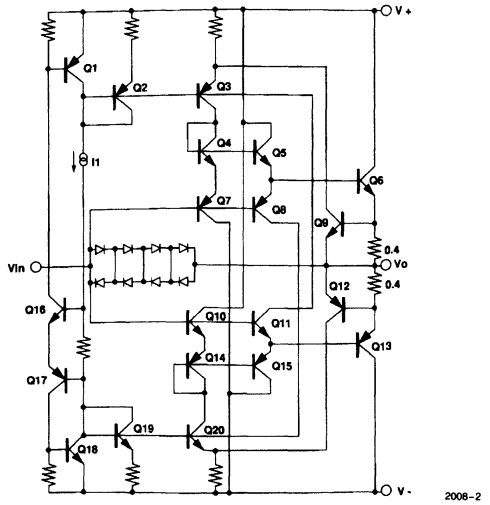
The EL2008 is a high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing only 13 mA of quiescent supply current. The EL2008's 1500 V/μs slew rate and 55 MHz bandwidth driving a 10Ω load is second only to the EL2009 and insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2008.

Used as an open loop buffer, the EL2008's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load. The EL2008 has output short circuit current limiting which will protect the device under both a DC fault condition and AC operation with reactive loads. In addition, the EL2008 has a temperature sensing circuit which disables the output stage in the event of a fault and limits the die temperature to a safe value.

The EL2008 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2008, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2008CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



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EL2008C
55 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15 or V_S	T_J	Operating Junction Temp	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{LD}	Lead Solder Temp <10 seconds	300°C
t_{SH}	Output Short Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	10	+40	I	mV
				T_{MIN}, T_{MAX}	−50		+50	IV	mV
I_{IN}	Input Current	0	∞	25°C	−35	−5	+35	I	µA
				T_{MIN}, T_{MAX}	−50		+50	IV	µA
R_{IN}	Input Impedance	±12V	100Ω	25°C	0.5	2		I	MΩ
A_{V1}	Voltage Gain	±10V	∞	25°C	0.985	0.9995		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	25°C	0.88	0.91		I	V/V
A_{V3}	Voltage Gain, V_S = ±15V	±3V	10Ω	25°C	0.87	0.89		I	V/V
V_{01}	Output Voltage Swing	±14V	100Ω	25°C	±13			I	V
V_{02}	Output Voltage Swing	±12V	10Ω	25°C	±10.5	±11		I	V
R_{01}	Output Impedance	±10V	±10 mA	25°C		1.8	2.5	I	Ω
R_{02}	Output Impedance	±10V	±1A	25°C		0.8	1.0	I	Ω
I_O	Output Current	±12V	(Note 4)	25°C	1.4	1.8		I	A
				T_{MIN}, T_{MAX}	1			IV	A
I_S	Supply Current	0	∞	25°C	9	13	22	I	mA
PSRR	Supply Rejection (Note 5)	0	∞	25°C	60			I	dB
V_S+, V_S-	Supply Sensitivity (Note 6)		∞	25°C			2	I	mV/V

EL2008C
55 MHz 1 Amp Buffer Amplifier

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
SR_1	Slew Rate	$\pm 10V$	50Ω	25°C		2500		V	V/μs
	(Note 7)	$\pm 10V$	10Ω	25°C		1500		V	V/μs
SR_2	Slew Rate (Note 8)	$\pm 5V$	10Ω	25°C		800		V	V/μs
t_r, t_f	Rise/Fall Time	100 mV	10Ω	25°C		7		V	ns
BW	−3 dB Bandwidth	100 mV	10Ω	25°C		55		V	MHz
C_{IN}	Input Capacitance			25°C		25		V	pF
THD				25°C			1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: During Output Short Circuit test the junction temperature rises and can activate the Thermal Shut down circuit. A heat sink will lower the junction temperature below the trip point.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V and −10V on the output.

Note 5: $V_S = \pm 4.5V$ then V_S is changed to ±18V.

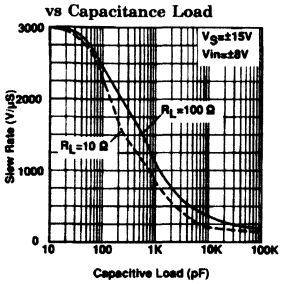
Note 6: $V_S+ = +15V$, $V_S- = -4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

Note 7: Slew Rate is measured between $V_{OUT} = +5V$ and $-5V$.

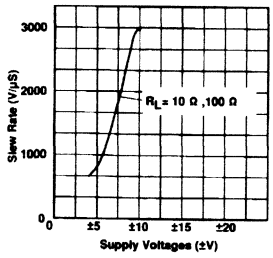
Note 8: Slew Rate is measured between $V_{OUT} = +2.5V$ and $-2.5V$.

Typical Performance Curves

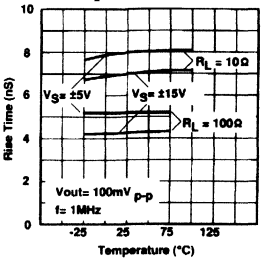
Slew Rate vs Capacitance Load



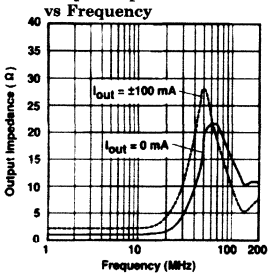
Slew Rate vs Supply Voltage



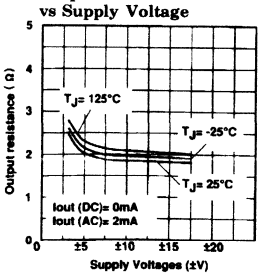
Rise Time vs Temperature



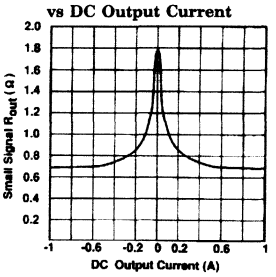
Output Impedance vs Frequency



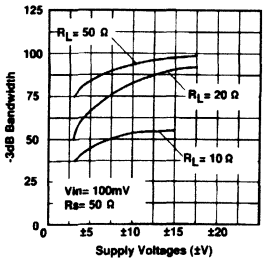
Output Resistance vs Supply Voltage



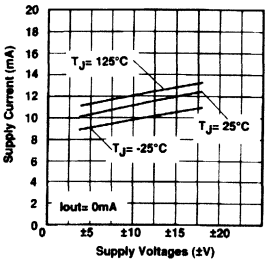
Small Signal Output Resistance vs DC Output Current



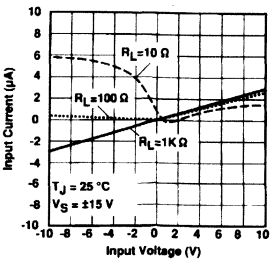
−3 dB Bandwidth vs Supply Voltage



Quiescent Supply Current vs Supply Voltage



Input Current vs Input Voltage



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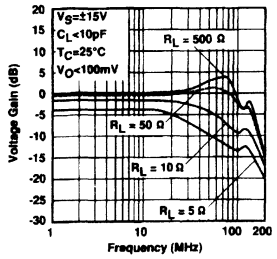
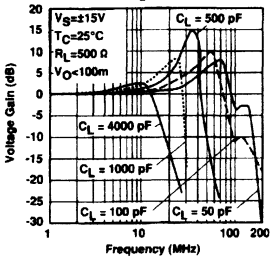
EL2008C
55 MHz 1 Amp Buffer Amplifier

Typical Performance Curves — Contd.

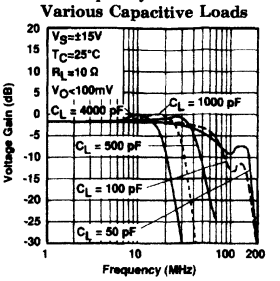
Voltage Gain vs Frequency at Various Resistive Loads



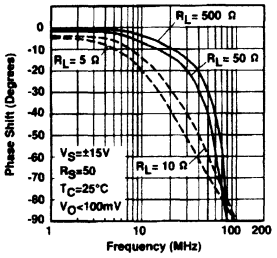
Voltage Gain vs Frequency at Various Capacitive Loads



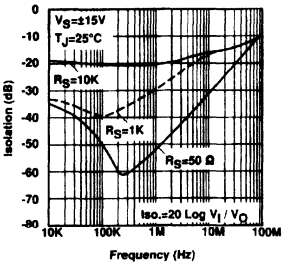
Voltage Gain vs Frequency at Various Capacitive Loads



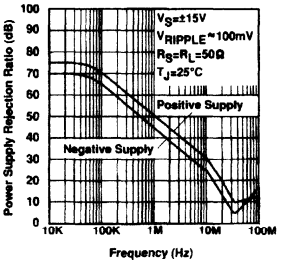
Phase Shift vs Frequency at Various Resistive Loads



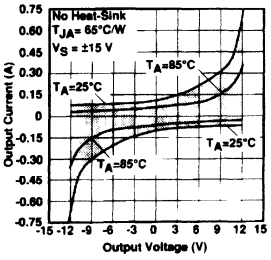
Reverse Isolation vs Frequency



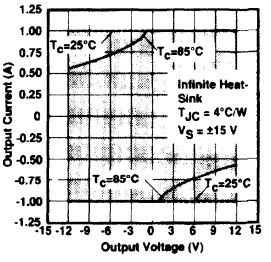
Power Supply Rejection Ratio vs Frequency



Active operating area. Operating outside area will invoke thermal shutdown or current limit.



Active operating area. Operating outside area will invoke thermal shutdown or current limit.



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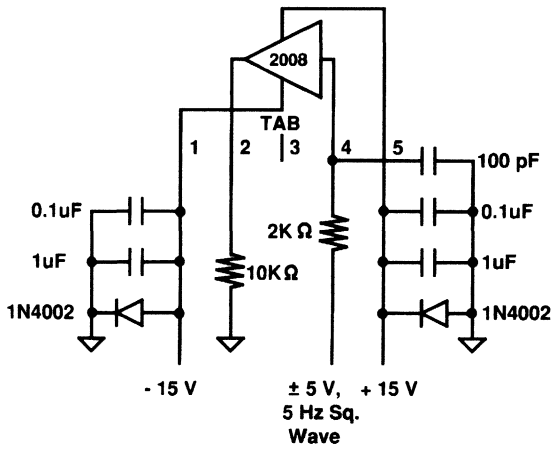
Burn-In Circuit



Applications Information

The EL2008 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2008 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2008's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 3000 V/μs slew rates with 10Ω load possible with modest supply current.

Power Supplies

The EL2008 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). However, bandwidth, slew rate and output impedance are affected by total supply voltages below 20V (±10V) as shown by the characteristic curves. It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum a 10 μF tantalum capacitor in parallel with a 0.1 μF capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2008 looks like a resistance in parallel with about 25 pF in addition to a DC bias current. The DC bias current is due to the mismatch in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range in some units. A few typical input current (I_{IN}) curves are shown in the characteristic curves.

Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. If the output of the EL2008 is accidentally shorted it is possible that some devices driving the EL2008's input could be damaged or destroyed driving the EL2008's load through the diodes while the EL2008 is unaffected. In such cases a resistor in series with the input of the EL2008 can limit the current.

EL2008C
55 MHz 1 Amp Buffer Amplifier

Applications Information — Contd.

Source Impedance
The EL2008 has good input to output isolation. Open loop, capacitive and resistive sources up to 100 kΩ present no oscillation problem driving resistive loads as long as care is used in board layout to minimize output to input coupling and the supplies are properly bypassed. When driving capacitive loads in the 100 pF to 1000 pF region source resistances above 25Ω can cause peaking and oscillation. Such problems can be eliminated by placing a capacitor from the EL2008's input to ground. The value should be about ¼ the load capacitance. In a feedback loop there is a speed penalty and a possibility of oscillation when the EL2008 is driven with a source impedance of 200Ω or more. Significant phase shift can occur due to the EL2008's 25 pF input capacitance. Inductive sources can cause oscillations. A series resistor of a few hundred ohms to 1 kΩ will usually solve the problem.

Current Limit
The EL2008 has internal current limiting to protect the output transistors. The current limit is about 1.5A at room temperature and decreases with junction temperature. At 150°C junction temperature it is above 1A.

Heat Sinking
A suitable heat sink will be required for most applications. When selecting a heat sink it should be remembered that the EL2008 will stop operating when the die temperature gets too high. The limit circuitry triggers between 150°C and 175°C. When the limit temperature is reached, the EL2008 is disabled and the supply current drops to about 2 mA regardless of load. The die must cool about 10°C before normal operation resumes. This hysteresis in the temperature limit circuit eliminates possible high frequency oscillation.

Depending on the heat sinking and ambient temperature the EL2008 will switch on and off at a few hertz when the device overheats. In thermal limiting the output is not tristated. The input protection diodes will still conduct when the input exceeds the output by ±2.5V. The thermal resistance junction to case for the TO-220 package is 4°C per watt. No voltage appears at the heat sink tab so no precautions need to be taken to avoid shorting the tab to a supply voltage or ground. As there is a small parasitic capacitance between the tab and the buffer circuitry, it is recommended that the tab be connected to AC ground (either supply voltage or DC ground). The center lead is internally connected to the tab so the connection can be made at the tab or the center lead.

Parallel Operation
If more than 1A is required or if heat management is a problem, several EL2008s may be paralleled together. The result is as through each device was driving only part of the load. For example, if two units are paralleled then a 5Ω load looks like 10Ω to each EL2008. Of course, parallel operation reduces both the input and output impedance and increases bias current. But there is no increase in offset voltage. Three units in parallel can drive a 3Ω load ±10V at 2500 V/μs. The output impedance will be about 0.33Ω.

Resistive Loads
The DC gain of the EL2008 is the product of the unloaded gain (0.999) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.999^* (R_L/R_L + R_{OUT})$$

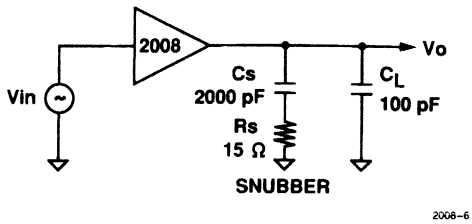
The high frequency response varies with the load resistance as shown by the characteristic curves. Both gain and phase are shown. If the 80 MHz peaking is undesireable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from output to ground. The capacitive load section discusses snubber usage in more detail.

Capacitive Loads
The EL2008 is not stable driving purely capacitive loads between 100 pF and 500 pF. Purely capacitive loads from 500 pF to 1000 pF will also have excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and ring for hundreds of nanoseconds.

When driving capacitive loads, stability can be achieved and peaking and ringing can be mini-

Applications Information — Contd.

mized either by adding a 50Ω (or less) load in parallel with the capacitive load or by an RC snubber circuit from output to ground. The snubber values can be found empirically by observing a squarewave or the frequency response. First just put a resistor alone from the output to ground until the desired response is achieved. The gain will be reduced due to the output resistance of the EL2008 and power consumption will be high. Then put a capacitor in series with the resistor to restore gain at low frequencies and eliminate the DC current. Start with a small capacitor and increase until the response is optimum. The figure below shows an example of an EL2008 driving a 100 pF load.



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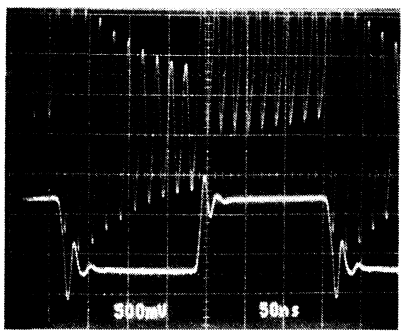

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Driving a pure capacitive load. Top trace is without a snubber. Bottom trace is with a snubber circuit.

Inductive Loads

The EL2008 with its 1A output current can drive small motors and other inductive loads. The EL2008's current limiting into inductive loads does NOT in and of itself cause spikes and kickbacks. However, if the EL2008 is in current limit and the input voltage is changing very quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltages. Motors are also able to generate kickback voltages when the EL2008 is in current limit.

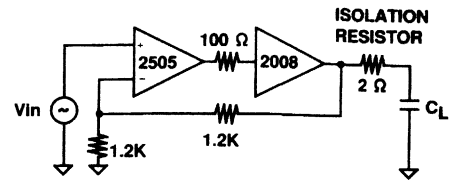
To prevent damage to the EL2008 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Op Amp Booster

The EL2008 can boost the output drive of almost any monolithic op amp. If the phase shift in the EL2008 is low at the op amp's unity gain frequency, no additional frequency compensation is required. An op amp followed with the EL2008 can drive loads as low as 10Ω to ±10V.

Driving capacitive loads with any closed loop system creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The EL2008 output impedance is less than 10Ω from DC to 30 MHz. But a capacitive load of 1000 pF will generate about 45 degrees of phase shift at 30 MHz. More capacitance will cause the problem at lower frequency.

With enough capacitance even slow op amps will become unstable. The simplest way to drive capacitive loads is to isolate them from the feedback with a series resistor. 1Ω to 5Ω is usually enough but the final value will depend on the op amp used and the range of load capacitance.



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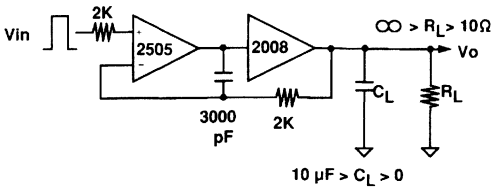
C_L		t_r		O.S.
13	pF	45	ns	20%
470	pF	50	ns	20%
1000	pF	55	ns	30%
3300	pF	60	ns	30%
0.1	μF	350	ns	0%
1	μF	4	μs	0%
5	μF	20	μs	0%

EL2008C
55 MHz 1 Amp Buffer Amplifier

Applications Information — Contd.

Unfortunately the isolation resistor is not inside the op amp feedback loop and cannot be neglected when computing the DC voltage gain into a resistive load. If load dependent DC gain is not tolerable then additional high frequency feedback from the op amp output (the EL2008 input) and an isolation resistor from the buffer output can be used to stabilize the loop. This configuration requires the op amp to be unity gain stable. This feedback method will allow the EL2008 to boost the output of the EHA2505 amplifier below and serve as a variable, bipolar 1A voltage supply with short circuit protection.



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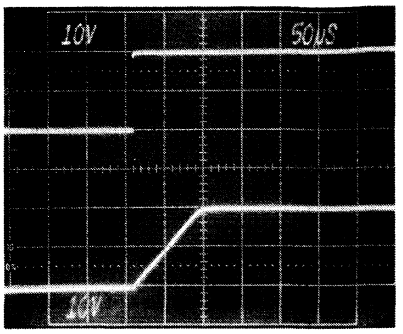
Slew Rate = $1A/C_L$

Video Distribution Amplifier

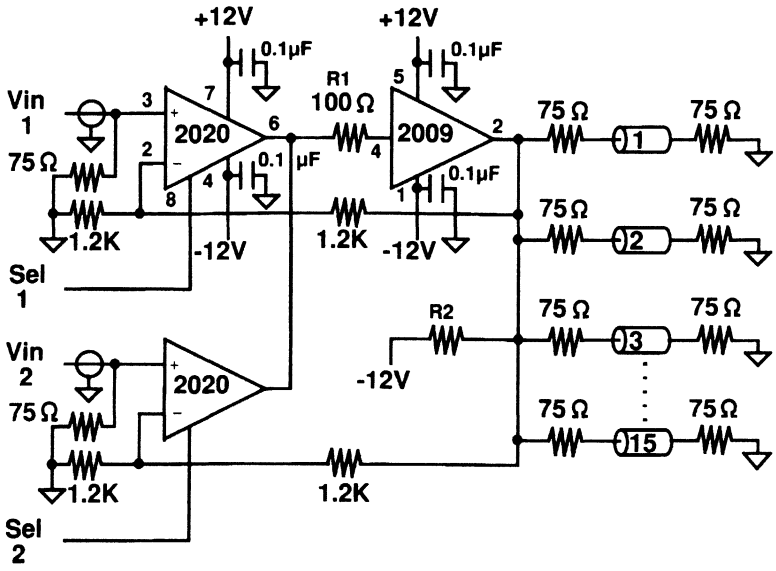
The EL2008 can drive 15 double matched 75Ω cables. If the EL2008 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase $<0.1°$ and differential gain $<0.1\%$. The 100Ω resistor at the EL2008 input (R1) is necessary to stabilize the loop. The 100Ω resistor at the EL2008 output (R2) to the $-12V$ supply, insures that the EL2008 sources current even when the output voltage is at 0V. This is necessary to achieve the excellent differential gain and phase values. More information about driving cables can be found in the EL2003 data sheet. See the EL2020 data sheet to learn more about using it as a multiplexer.



2008-10

Input (top trace) and output (bottom trace) of EHA2505 op amp boosted by EL2008.

Video Mux and Distribution Amplifier



2008-11

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2009C
90 MHz 1 Amp Buffer Amplifier

Features

- High slew rate—3000 V/μs
- Wide bandwidth—
  125 MHz @ R_L = 50Ω
  90 MHz @ R_L = 10Ω
- Output current—1A continuous
- Output impedance—1Ω
- Short circuit protected
- Over temperature protected
- Power package with isolated metal tab

Applications

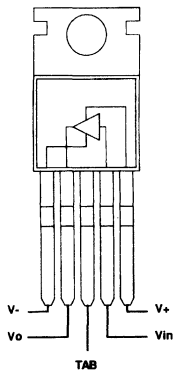
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2009CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



2009-1

Top View

General Description

The EL2009 is a high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing 40 mA of quiescent supply current. The EL2009's 3000 V/μs slew rate and 90 MHz bandwidth driving a 10Ω load insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2009.

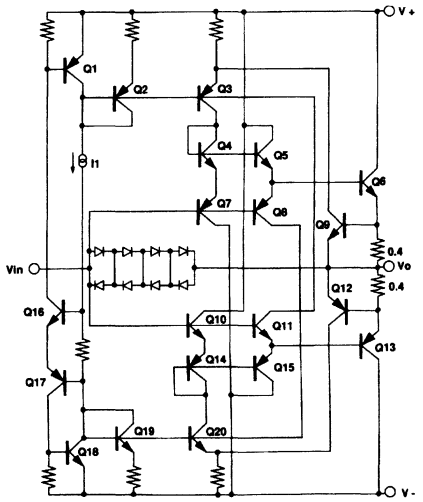
Used as an open loop buffer, the EL2009's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load.

The EL2009 has an output short circuit current limit which will protect the device under both a DC fault condition and AC operation with reactive loads. In addition, the EL2009 has a temperature sensing circuit which disables the output stage in the event of a fault and limits the die temperature to a safe value.

The EL2009 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2009, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore, the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2009CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



2009-2

EL2009C
90 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15V or V_S	T_J	Operating Junction Temp.	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp. Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{LD}	Lead Solder Temp. <10 seconds	300°C
t_{SH}	Output Short Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	25°C	−60		60	I	mV
				T_{MIN}, T_{MAX}	−80		80	IV	mV
I_{IN}	Input Current	0	∞	25°C	−125	−5	125	I	μA
				T_{MIN}, T_{MAX}	−200		200	IV	μA
R_{IN}	Input Impedance	±12V	100Ω	25°C	250	900		I	kΩ
A_{V1}	Voltage Gain	±10V	∞	25°C	0.985	0.999		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	25°C	0.88	0.90		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	10Ω	25°C	0.87	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	100Ω	25°C	±13			I	V
V_{O2}	Output Voltage Swing	±12V	10Ω	25°C	±10.5	±11		I	V
R_{O1}	Output Impedance	±10V	±10 mA	25°C			1.5	I	Ω
R_{O2}	Output Impedance	±10V	±1A	25°C		0.9	1.0	I	Ω
I_O	Output Current	±12V	(Note 4)	25°C	1.4	1.8		I	A
				T_{MIN}, T_{MAX}	1			IV	A
I_S	Supply Current	0	∞	25°C	30	45	65	I	mA
PSRR	Supply Rejection (Note 5)	0	∞	25°C	60			I	dB

EL2009C
90 MHz 1 Amp Buffer Amplifier

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_S+, V_S-	Supply Sensitivity (Note 6)		∞	25°C			2	I	mV/V
SR_1	Slew Rate (Note 7)	±10V	50Ω 10Ω	25°C		3000 2500		V	V/μs
SR_2	Slew Rate (Note 8)	±5V	10Ω	25°C		1250		V	V/μs
t_r, t_f	Rise/Fall Time	100 mV	10Ω	25°C		7		V	ns
BW	−3 dB Bandwidth	100 mV	10Ω	25°C		90		V	MHz
C_{IN}	Input Capacitance			25°C		25		V	pF
THD	Total Harmonic Distortion			25°C			1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: During Output Short Circuit test the junction temperature rises and can activate the Thermal Shut down circuit. A heat sink will lower the junction temperature below the trip point.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V input and −10V on the output.

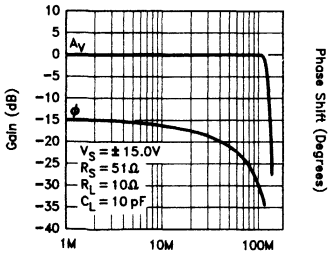
Note 5: $V_S = \pm 4.5V$ then V_S is changed to ±18V.

Note 6: $V_S+ = +15V$, $V_S- = 4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

Note 7: Slew Rate is measured between $V_{OUT} = +5V$ and −5V.

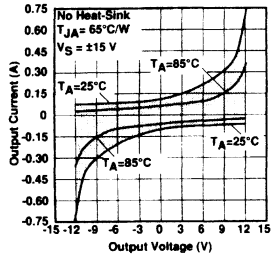
Note 8: Slew Rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

Voltage Gain and Phase vs Frequency



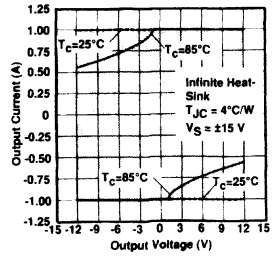
2009-4

Active operating area. Operating outside area will invoke thermal shutdown or current limit.



2009-5

Active operating area. Operating outside area will invoke thermal shutdown or current limit.



2009-6

Applications Information

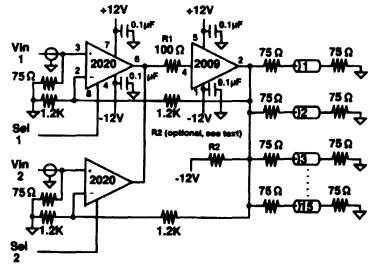
Video Distribution Amplifier

The EL2009 can drive 15 double matched 75Ω cables. If the EL2009 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase <0.1° and differential gain <0.1%. The 100Ω resistor at the EL2009 input (R1) is necessary to stabilize the loop. The EL2009 operates with a CLASS AB output which exhibits a slight rise in output impedance when-

Applications Information — Contd.

ever the current it sources into the load approaches zero. In those cases, where differential gain and phase are measurably affected, resistor R2 may be added to ensure that the EL2009 output current never reaches zero. This will result in a CLASS A output stage with active pulldown but with the penalty of power dissipation in R2. More information about driving cables can be found in the EL2003 data sheet.

Video Mux and Distribution Amp.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2031C
550 MHz Buffer Amplifier

Features
- Wide bandwidth—550 MHz
- High slew rate—7000 V/μs
- Low quiescent power
- FET input
- 100 mA peak output current

Applications
- Current booster
- Cable/line driver for high resolution graphics
- Flash A/D input buffer
- Isolation buffer
- A.T.E. pin driver

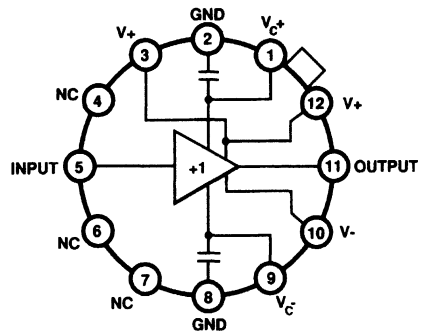
Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2031CG	0°C to +70°C	TO-8	MDP0026

General Description
The EL2031C is an extremely high speed hybrid buffer amplifier which can drive 100Ω loads at frequencies from DC to 550 MHz and with large signal slew rates greater than ±8000 V/μs. The FET input insures minimal loading of the input signal and optimum transient performance. It can output peak currents of ±100 mA. To minimize power supply coupling effects, 0.015 μF supply bypass capacitors are included inside the EL2031C.

These extremely high speed buffers may be used in a broad range of analog or digital applications requiring extremely fast, high current outputs. Examples include high resolution graphics terminal R-G-B line drivers, ATE pin drivers or pin receiver buffers, flash A/D converter input buffers, and oscilloscope input stages. The pinout is similar to earlier generation EL2004 and ELH0033 buffers.

Connection Diagram



2031-1

Top View

EL2031C
550 MHz Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

(V+) - (V−)	Supply Voltage	−0.3V to +25V	I_{OUT}	Output current (Continuous)	±70 mA
(V_C+) - (V_C−)	Output Device Collector Supplies	−0.3V to +25V		(Peak)	±100 mA
(V+) - (V_C+) or (V_C−) - (V−)			(V_C+) - Gnd or (V_C−) - Gnd		
	Supply Differential	−0.3V to +25V		Output device supply to gnd	±50V
(V+) - (V_{IN}) or (V_{IN}) - (V−)			T_J	Operating Junction Temperature	175°C
	Input Range	17.5V	T_A	Operating Temperature Range	0°C to +70°C
I_{IN}	Input (fault) Current	±20 mA	T_{ST}	Storage Temperature Range	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V+ = V_C+ = 10V, V− = V_C− = −10V, R_S = 50Ω

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	V_{IN} = 0, T_A = 25°C		3	10	I	mV
		T_{MIN}, T_{MAX}			20	III	mV
I_B	Input Bias Current	V_{IN} = 0, 5V, T_A = 25°C, T_{MIN}, T_{MAX}			10	II	nA
		V_{IN} = 5V, T_A = 25°C, T_{MIN}, T_{MAX}			1	II	µA
R_{IN}	Input Impedance	V_{IN} = ±1V, T_A = 25°C, T_{MIN}, T_{MAX}		4000		V	MΩ
V_O	Output Voltage Swing	V_{IN} = ±7.5V, T_A = 25°C, T_{MIN}, T_{MAX}					
		No Load,	±6.6	±7.2		II	V
		R_L = 100Ω	±6.0	±6.8		II	V
A_V	Voltage Gain	V_{IN} = ±5V, T_A = 25°C, T_{MIN}, T_{MAX}					
		No Load,	0.96	0.985	1.0	II	V/V
		R_L = 100Ω	0.86	0.93	0.96	II	V/V
R_O	Output Impedance	V_{IN} = ±5V, I_L = 0 mA to 50 mA	3	6	11	II	Ω
		T_A = 25°C, T_{MIN}, T_{MAX}					
I_S	Total Supply Current	V_{IN} = 0, T_A = 25°C, T_{MIN}, T_{MAX}		22	26	II	mA

EL2031C
550 MHz Buffer Amplifier

DC Electrical Characteristics $V+ = V_C+ = 10V, V- = V_C- = -10V, R_S = 50\Omega$ — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
PSRR	Power Supply Rejection	$V_{IN} = 0$, $T_A = 25°C$ (Note 1)		61		V	dB
V_S+	Sensitivity	$V_{IN} = 0$, $T_A = 25°C$, $V- = V_C- = -10V$ and $V+ = V_C+$ from $+5V$ to $+12V$		7	25	I	mV/V
V_S-	Sensitivity	$V_{IN} = 0$, $T_A = 25°C$, $V+ = V_C+ = 10V$ and $V- = V_C-$ from $-5V$ to $-12V$		9	25	I	mV/V

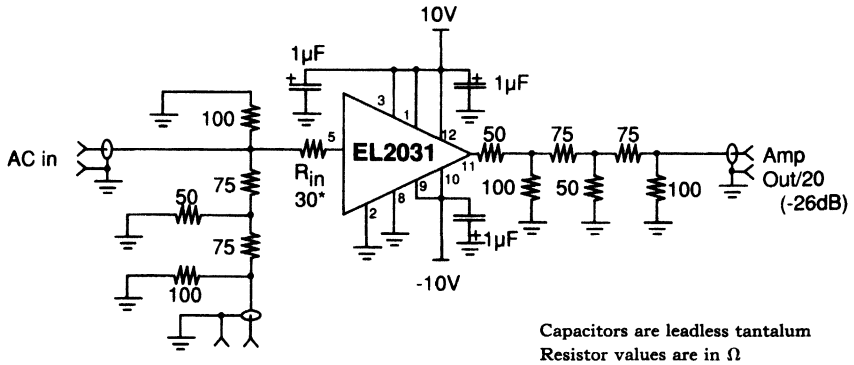
AC Electrical Characteristics (Note 2) $V+ = V_C+ = 10V, V- = V_C- = -10V, R_S = 50\Omega, T_A = 25°C$

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
t_r	Rise Time	$V_{IN} = -0.5V$ to $0.5V$, $R_L = 100\Omega$ 10% to 90%		650	1000	I	ps
t_f	Fall Time	$V_{IN} = 0.5V$ to $-0.5V$, $R_L = 100\Omega$, 10% to 90%		650	1000	I	ps
t_{pd}	Propagation Delay	$V_{IN} = -0.5$ to $0.5V$ or $0.5V$ to $-0.5V$, $R_L = 100\Omega$, 10% of V_{IN} to 10% of V_{OUT}		500		V	ps
t_{rl}	Large Signal Rise Time	$V_{IN} = -5V$ to $5V$, $R_L = 100\Omega$, 10% to 90%		650		V	ps
t_{fl}	Large Signal Fall Time	$V_{IN} = -5V$ to $5V$, $R_L = 100\Omega$, 10% to 90%		1200		V	ps
SR+	Positive Slew-rate	$V_{IN} = -5V$ to $5V$, $R_L = 100\Omega$, 25% to 75%	5000	10000		I	V/μs
SR−	Negative Slew-rate	$V_{IN} = 5V$ to $-5V$, $R_L = 100\Omega$, 25% to 75%	−5000	−7000		I	V/μs
BW	−3 dB Bandwidth	$V_{IN} = 1\ V_{p-p}$, $R_L = 100\Omega$		550		V	MHz
	Gain Peaking	$V_{IN} = 1\ V_{p-p}$, $R_L = 100\Omega$, 0.5 MHz to 500 MHz		0.5		V	dB
	Group Delay	$V_{IN} = 1\ V_{p-p}$, $R_L = 100\Omega$ 5 MHz to 125 MHz		0.5		V	ns
	Phase Linearity	$V_{IN} = 1\ V_{p-p}$, $R_L = 100\Omega$ 5 MHz to 125 MHz		1.0		V	°
A_V	Voltage Gain	$V_{IN} = 1\ V_{p-p}$, $R_L = 100\Omega$, 10 MHz		0.94		V	V/V
Z_{OUT}	Output Impedance	$V_{IN} = 1\ V_{p-p}$, 10 MHz		6		V	Ω
C_{IN}	Input Capacitance	10 MHz		3		V	pF

Note 1: PSRR tests are performed with $V+ = V_C+$ and $V- = V_C-$. The supplies are simultaneously changed from ±5V to ±12V.

Note 2: AC tests are done using an Avtech AVMP−3-C pulse generator and a Tektronics 11402 digitizing oscilloscope with an 11A71, 1 GHz plug-in. The device under test has 50Ω input termination, 100Ω output load, and a Tektronics P66501, 750 MHz probe buffers the output for cabling to the oscilloscope. The system rise time is removed from all device reading.

AC Test Fixture



Capacitors are leadless tantalum
Resistor values are in Ω

2031-2

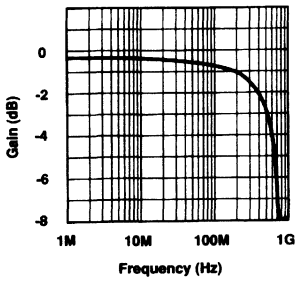
Reference out
= $(V_{inDUT})/10$
(−20 dB)

*R_{IN} = 30Ω for small signal AC
R_{IN} = 0 for transient signal tests

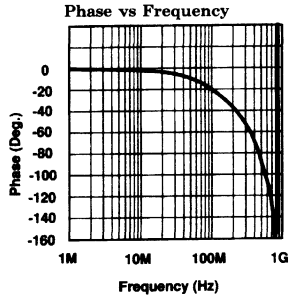
EL2031C
550 MHz Buffer Amplifier

Typical Performance Curves

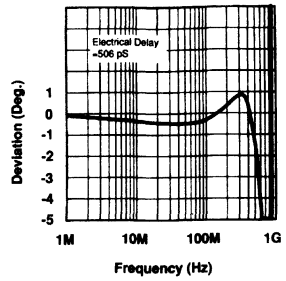
Gain vs Frequency



Phase vs Frequency

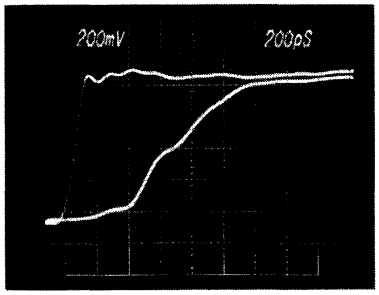


Deviation from Linear Phase



2031-3

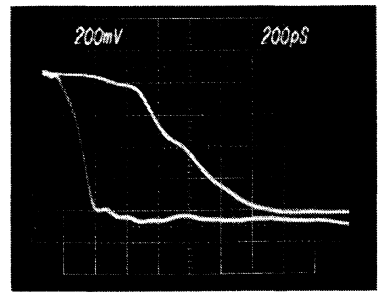
Small Signal Response



200 mV/cm vertical, 200 ps/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

2031-4

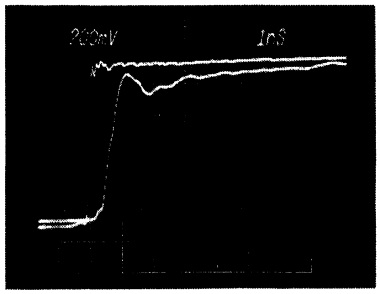
Small Signal Response



200 mV/cm vertical, 200 ps/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

2031-5

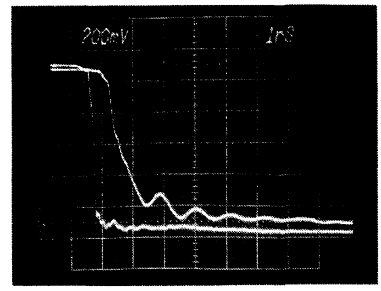
Large Signal Response



2 V/cm vertical, 1 ns/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

2031-6

Large Signal Response

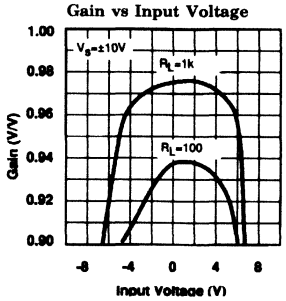


2 V/cm vertical, 1 ns/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

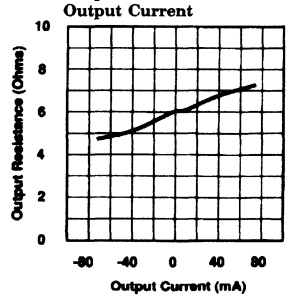
2031-7

Typical Performance Curves — Contd.

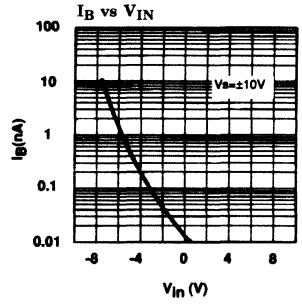
Gain vs Input Voltage



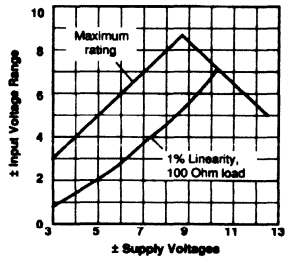
Output Resistance vs Output Current



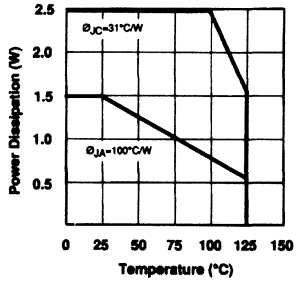
I_B vs V_{IN}



Input Range vs Supply Voltage



Maximum Power Dissipation



2031-8

EL2031C
550 MHz Buffer Amplifier

Application Information

The EL2031 is a very pure buffer amplifier—a wire with good reverse isolation, so to speak, and as such is very easy to use. Obtaining its ultimate performance, though, requires attention to operating limits and construction details.

Operating Voltages

The transistors used within the EL2031 have f_t's of several GHz, and are consequently limited in voltage range. As seen in the absolute rating table, the input voltage is restricted to within 17.5V of any supply rail. Thus, if the supplies are ±10V the input must not exceed ±7.5V. With the highest supplies allowed (±12.5V), the input is restricted to ±5V.

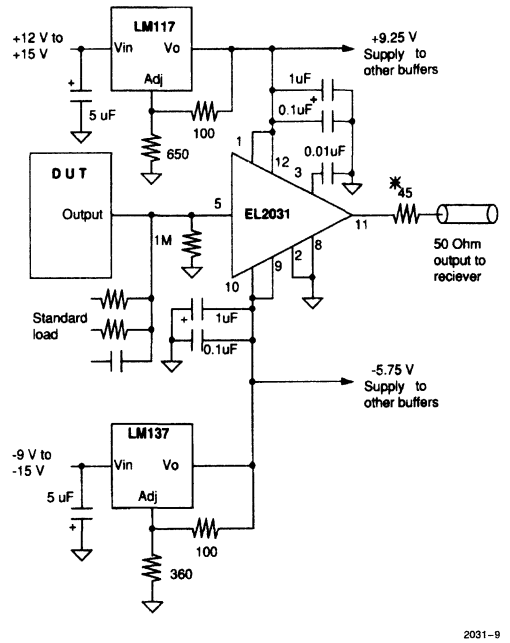
A practical approach might be to supply the power to the EL2031 via two inexpensive 3-terminal adjustable voltage regulators. The Input Voltage Range versus Supply Voltage curve shows the maximum supply and input voltage range along with the input range that does not exceed 1% linearity error wih a 100Ω load.

Design Example: Buffering Logic Outputs in an Automatic IC Test System

The output of logic circuits can range from a −2V low ECL level to a +5V high CMOS level. It would be desirable to buffer the output pin from the 50Ω transmission system so that the test-head electronics need not be packed with pin receivers and switches to route signal locally.

The 1% linear input range of the EL2031 should be set to at least −2.5V to +6V, or an 8.5V span. If this span was based symmetrically around ground, it would require supplies that support ±4.25V swings with 1% linearity. Referring to the Input Voltage Range versus Supply Voltage curve, we would need at least ±7.5V supplies. Offsetting the supplies to match the input range offset, we arrive at +9.25V and −5.75V supplies.

Figure 1 shows a practical ATE interface. Note the 1 MΩ resistor at the input of the EL2031, providing a known input level to the buffer in the absence of a device or standard load being connected. A second benefit from the buffer driving a 50Ω environment is that the full logic swing is halved before being monitored by the comparators in the measuring system, and their input range is not exceeded.



*45Ω + 5Ω output impedance of EL2031 matches 50Ω load.

Figure 1. EL2031 is Pin Buffer for an IC Test System

Circuit and Construction Techniques

In any circuit that operates above 100 MHz, parasitic capacitance and inductance will limit AC performance. Although the EL2031 is quite stable with source resistance as high as 500Ω, only 64 MHz of −3 dB bandwidth would be possible with a practical 5 pF circuit and parasitic input capacitance. Generally, all signals should be kept in a 50Ω environment to preserve bandwidth. Given such a 50Ω system (presenting a 25Ω source if doubly terminated), even 12 pF of stray capacitance can be tolerated while preserving the 550 MHz bandwidth of the EL2031.

Application Information — Contd.

Parasitic inductance is perhaps more of a problem than capacitance at these frequencies. An inch of straight #34 wire has an inductance of 50 nH. This apparently small inductance has a reactance of 173Ω at 550 MHz! Clearly, signals should be connected with traces shorter than ¼ inch (6 mm) wherever possible. Use low inductance leadless resistors and capacitors in the signal path.

To ease the power supply decoupling, two 0.015 μF capacitors are mounted inside the EL2031. External high frequency capacitors (0.1 μF in parallel with 1 μF), should be connected from the power supply pins of the buffer to the ground plain (See Figure 1), as close to the buffer as possible. A solid ground plane and stripline layout techniques will help realize the potential performance of the buffer. The ground plane below the strip intercepts and diminishes magnetic fields from the wire, greatly reducing its inductance. In general, a ground plane should always be used with the EL2031. It is better to have only one plane, the one on the opposite side of the signal interconnect, as the return of bypass and signal components. A second ground plane will not be at the same "ground" potential as the first ground plane, and the pulse quality and frequency flatness of the circuit will be compromised. Finally, gold plating reduces skin effect resistances of all circuit traces and improves AC performance.

A socket will add parasitic inductance and magnetic coupling, degrading AC characteristics. The EL2031 comes with short ¼" leads, but it is still better to mount the device as close to the circuit board as possible. Pin sockets are a good compromise.

The case is unconnected, but less ringing from pulses will result from grounding the case. Just where on the circuit board ground should be connected is found experimentally. A small degradation in speed results from grounding the case. For extended temperature operation, a Thermalloy 2240A (33°C/W), Wakefield 215CB (30°C/W) or IERC 848CB (15°C/W) heat sink can be used to reduce the nominal 100°C/W case to ambient thermal resistance.

Pinout Consideration

The pinout of the EL2031 is similar to that of the EL2004 and ELH0033 buffers, except that the Offset Adjust pins 6 and 7 are not brought out, to maintain the frequency response of the device. Pin 2 and 8 are being used in the EL2031 package as a ground return for the internal bypass capacitors and should be tied to the ground plane as close to the package as possible. V+ appears on both pin 3 and pin 12.

Short Circuit Protection

As stated before, the transistors within the EL2031 are fairly delicate and can only output 100 mA peak. Short-circuit protection circuitry inevitably would have slowed the performance of the device, and was not included.

The traditional use of resistors in series with the power supply lines limits the short-circuit (see the application section of the EL2004 buffer) but does not allow a full loaded output swing. Restricting the input voltage range allows the resistors to be a higher value while allowing adequate loaded swing. Back-termination (a 50Ω source working into an unterminated load) maximizes the swing with higher valued resistors.

Finally, a series 50Ω output resistor will help reduce the short-circuit current. Note that if the output of the buffer is shorted and a positive input applied to the input, input current will rise if the output transistor saturates against the supply line resistor. Maximum input as well as output currents must be observed.

Example: A worst case short-circuit and some remedies

Figure 2 shows a simplified schematic of the EL2031. For the worst short circuit situation, let V+ and V− be ±10V, R_{SC} = 0, R_S = 0, R_O = 0 and V_{IN} = +7.5V.

When the output is shorted, large and uncontrolled currents flow through Q2's collector and emitter. Uncontrolled currents also flow through Q1's gate and source and Q2's base, since Q1's gate is now forward biased. The input current maximum rating is also violated. Actually, even normal operation can violate the maximum

EL2031C
550 MHz Buffer Amplifier

Application Information — Contd.

current ratings of the part. If the input is a realistic 5V level, the output current will be almost 100 mA, not sustainable continuously.

Setting R_O to 50Ω will halve the output current to safe levels and provide better impedance match to the 50Ω cable and load, although the voltage gain is reduced to ½.

We can set R_{SC} to 140Ω in an attempt to limit Q2's collector current. With $R_O = 0$ and an output short to ground, Q2 will saturate with a collector current of about 70 mA. This will again cause large input currents to flow from V_{IN} if R_S is small. With the output shorted, the input voltage (at the maximum 20 mA of input current) will be about 1.8V. To tolerate an input of +5V, set R_S to 160Ω. To preserve frequency response, R_S should be paralleled with a 100 pF to 1000 pF capacitor. This approach will save the buffer from shorts, but it can only output 2.5V before Q2 or Q3 saturates.

At this point the values need to be refined. The Idss of Q1 is added to the 20 mA of input current and sent to the output. Thus, there is a total output current of 110 mA into a short. We can revise the value of R_S to 300Ω and R_{SC} to 250Ω to reduce currents. The maximum output swing is now diminished to 1.5V.

Another approach is to set R_O to 50Ω. Now an output short leaves 50Ω at the EL2031 output to ground rather than 0Ω. The 70 mA maximum output current sets 3.5V at the buffer output and V_{IN} may rise to about 5.3V before an input R_S is needed to limit input current. At $V_{IN} = 5V$, no input current flows, so only Idss adds to the output. R_{SC} is set to 130Ω (10V supply minus the 3.5V output, since Q2 is saturated, all divided by 70 mA minus the 20 mA Idss). Thus a 3.5V maximum output can be generated, or 1.7V at the load.

Clearly, not shorting the device output will obviate the need for R_S and R_{SC} and allow maximum output swing. When buffers are mounted on a board and are physically protected from shorts, no electrical protection should be needed.

Obtaining Optimum Frequency Responses

The EL2031, like all other amplifiers, has an input impedance that changes with frequency. At 750 MHz, the input impedance falls to about 15Ω, and has a negative real component. This means that a very fast input edge will cause a transient response at the input of the device, although this is not observed at the EL2031 output. A one to two dB peak can be seen in the frequency response curve at about 480 MHz as well, and it is affected by input wire inductance and source resistance and capacitance. A 30Ω resistor in series with the input will "de-Q" the EL2031 and provide the extremely well-behaved responses shown in the Bode and phase linearity plots.

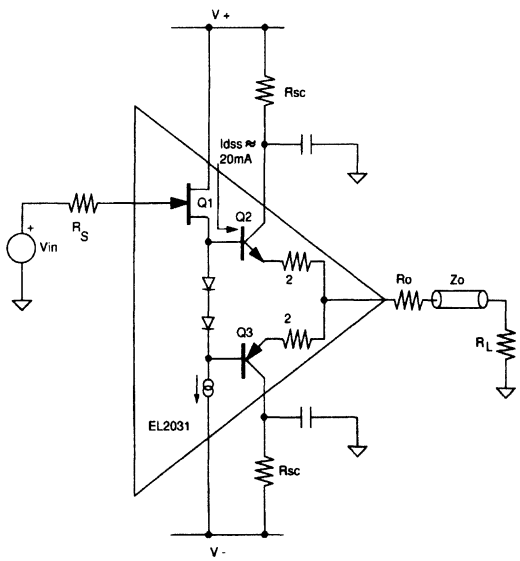
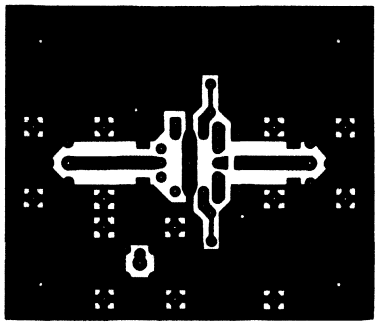


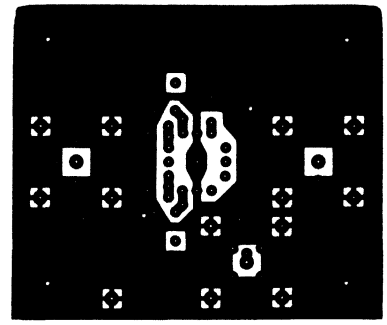
Figure 2. Simplified EL2031 Buffer Schematic

Component Side



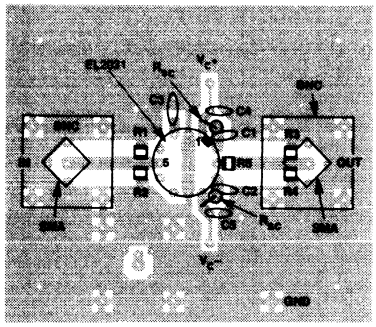
2031-11

Connector Side



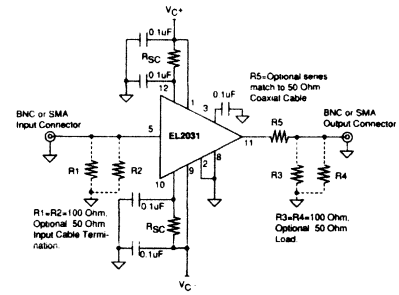
2031-13

Assembly Drawing



2031-12

PCB Schematic



2031-14

Suggested PC Board Layout

The EL2031 is a very fast buffer amplifier. Obtaining its ultimate performance requires attention to construction details. The PC board shown above was used to test and characterize the EL2031. It contains an extensive ground plane, parasitic capacitance and inductance are kept to a minimum by keeping the traces short and SMD low inductance leadless resistors were being used in the signal path and placed close to the EL2031.

Two 0.015 μF decoupling capacitors are mounted inside the EL2031. The PC board has provisions for five external high frequency 0.1 μF capacitors connected from the power supply pins of the buffer to the ground plane as close to the buffer as possible. Note that the capacitors can be mounted on the connector side.

The PC board has room for optional resistors:

R1 & R2: 100Ω resistors forming 50Ω termination of the input coaxial cable.

R3 & R4: 100Ω resistors forming a 50Ω load for the buffer.

R5: Series match for the output 50Ω coaxial cable.

R_{SC}: Short-circuit current limiting resistors.

Remember to insert a jumper if the R_{SC} resistors or R5 are not being used. Note that one of the ground pins in the SMA Coaxial connectors needs to be clipped to fit in the PCB. Mount the SMA or BNC connectors on the connector side so as not to interfere with R3 and R4.

Application Specific

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2021C
Monolithic Pin Driver

Features
- Wide range of programmable analog output levels
- 0.5 Ampere output drive with external transistors
- Programmable Slew Rate
- Low overshoot with large capacitive loads-stable with 500 pF
- 3-state output
- Power-down capability
- Wide supply range
- Overcurrent sense

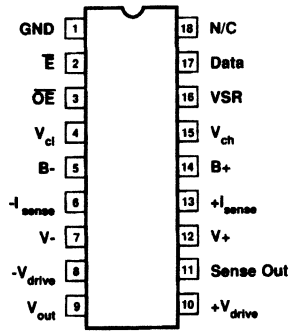
Applications
- Loaded circuit board testers
- Digital testers
- Programmable 4-quadrant power supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2021CJ	0°C to +75°C	CerDIP	MDP0025

Connection Diagram

18-Pin DIP Package



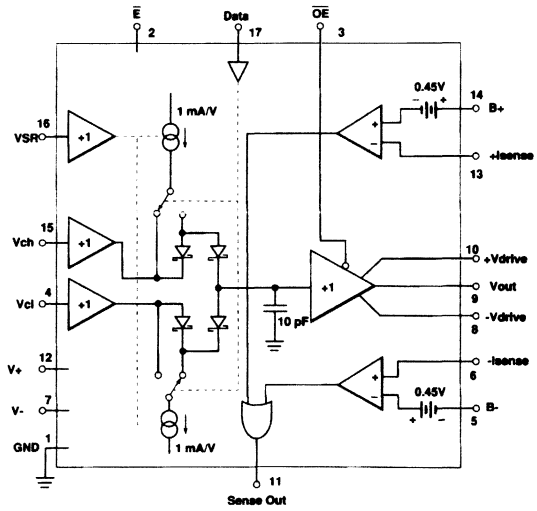
2021-1

Top View

General Description

The EL2021 is designed to drive programmed voltages into difficult loads. It has the required circuitry to be used as the pin driver electronics in board test systems. Capable of overpowering logic outputs, the part can accurately drive independently set high and low levels with programmed Slew Rates into reactive loads. It can also be placed into high impedance to monitor the load without having to disconnect. Previous board testers had multiplexing schemes to reduce the number of pin drivers required. With the small size and power consumption of the monolithic EL2021, a driver per node with little or no multiplexing becomes practical. Since only a few pins of "bed-of-nails" board testers need be active at any given time, the power-down feature saves substantial power in large systems.

Block Diagram



2021-2

Truth Table

$\overline{E}$	$\overline{OE}$	Data	V_{OUT}	Comments
0	0	0	V_{CL}	Active
0	0	1	V_{CH}	Active
0	1	X	High-Z	Third State
1	X	X	Undefined	Power-down

EL2021C
Monolithic Pin Driver

Absolute Maximum Ratings (T_A = 25°C)

V+	Supply Voltage	−0.3V to +16V	Sense Out	Output Current	−10 mA to +10 mA
V−	Supply Voltage	0.03V to −16V	V_{OUT}, Drive+, Drive−	Output Currents	−45 mA to +45 mA
B+, B−	Supply Voltages	V− to V+	T_J	Junction Temperature	150°C
Sense+	Input Voltages	(−2V + B+) to (0.3V + B+)	T_A	Operating Ambient Temperature Range	0°C to +75°C
Sense−	Input Voltages	(−0.3V + B−) to (2V + B−)			
$\overline{E}$, VSR, $\overline{OE}$, Data	Input Voltages	−0.3 to +6V	T_{ST}	Storage Temperature	−65°C to +150°C
V_{CH}, V_{CL}	Input Voltages	B− to B+ and V− to V+	P_D	Power Dissipation (T_A = 25°C) (See Curves)	1.8W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta>40 @ I_C = 400 mA and Beta>27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
I_S	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = H or L	15	25	30	I	mA
		V_{CH} = 11V, V_{CL} = −6V, VSR = 5V, Data = H or L	21	33	45	IV	mA
		V_{CH} = −6V, V_{CL} = 11V, VSR+2.5V, Data = H or L	15	25	30	IV	mA
I_S, disabled	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data = H or L, $\overline{E}$ = H	0	0.5	2.5	I	mA
I_{VCH}	V_{CH} Input Current	V_{CH} = −1V to +7.5V, V_{CL} = 0V, VSR = 5V, Data = H or L	−20	5	20	I	μA
I_{VCL}	V_{CL} Input Current	V_{CL} = −3.5V to +3.5V, V_{CH} = 0V, VSR = 5V, Data = H or L	−20	−5	20	I	μA
I_{Data}	Data Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0 or 5V	−50	5	50	I	μA
I_{OE}	$\overline{OE}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{OE}$ = 0V or 5V	−20	5	20	I	μA
I_E	$\overline{E}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{E}$ = 0V or 5V	−20	2	20	I	μA
I_{VSR}	VSR Input Current	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 0V or 5V	−20	2	20	I	μA
$\pm I_{sense}$	Sense Input Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0V or 5V	−20	5	20	IV	μA
I_B+, I_B-	B+, B− Input Currents	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 5V	−20	5	20	IV	μA

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta>40 @ I_C = 400 mA and Beta>27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low. — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage	V+ = 14.5V, V− = −9.5V					
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = L,					
		Output Current = −100 mA, 0 mA, or +100 mA	−50		50	I	mV
		Output Current = −400 mA or +400 mA	−300		300	I	mV
		Output Current = −500 mA or +500 mA	−600		600	I	mV
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = H					
		Output Current = −100 mA, 0 mA, or +100 mA	4.95		5.05	I	V
		Output Current = −400 mA or +400 mA	4.7		5.3	I	V
		Output Current = −500 mA or +500 mA	4.4		5.6	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = L	−6.1		−5.9	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = H	10.9		11.1	I	V
I_{sense+}	+I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = H	400	450	500	I	mA
I_{sense-}	−I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = L	−400	−450	−500	I	mA
$V_{O, sense}$	Sense Out Levels	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data L or H,					
		Output Current = −350 mA or +350 mA	0		0.6	I	V
		Output Current = −550 mA or +550 mA	3.5		5.0	I	V
$I_{OUT,TRI}$	High-Impedance Output Leakage	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = L, $\overline{OE}$ = H, Output Voltage = −2.5V or +7.5V	−100	5	100	I	μA

AC Electrical Characteristics

DC test conditions apply except where noted. For AC tests, R_L = 1k, C_L = 200 pF. Delay times are measured from $\overline{OE}$ or Data crossing 2.5V, V_{CH} = 5V, V_{CL} = 0.

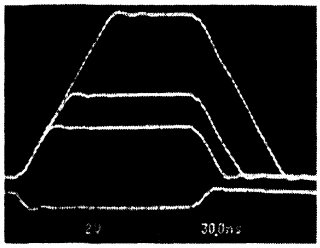
Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
SR+	+Slew Rate	Data L to H, Output from 0.5V to 4.5V, VSR = 1V	80	100	120	I	V/μs
		VSR = 3V	150	240	360	I	V/μs
SR−	−Slew Rate	Data H to L, Output from 4.5V to 0.5V, VSR = 1V	−80	−100	−120	I	V/μs
		VSR = 3V	−150	−240	−360	I	V/μs
SRSYM	Slew Rate Symmetry	$\left[\frac{(SR+)-(SR-)}{(SR+)+(SR-)}\right]$ VSR = 1V	−10		10	I	%
		VSR = 2V	−20		20	IV	%
T_{pd}	Propagation Delay	Data L to H, Output to 0.2V, VSR = 2.5V	6.5	9	11.5	I	ns
		Data H to L, Output to 4.8V, VSR = 2.5V	6.5	9	11.5	I	ns
T_s	Settling Time	VSR = 5V, Data L to H, Output 4.5V to 5V±0.2V			30	IV	ns
		VSR = 5V, Data H to L, Output 0.5V to ±0.2V			30	IV	ns
OS	Overshoot	VSR = 1V, Data L to H or H to L	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = L, R_L to 5V	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = H, R_L to 0V	−300		300	I	mV
T_{pda}	Propagation Delay, High-Z to Active	VSR = 2.5V, $\overline{OE}$ H to L, C_L = 50 pF					
		R_L to 5V, Data = L, Output to 3.5V			50	I	ns
		R_L to 0V, Data = H, Output to 1.5V			50	I	ns
T_{pdh}	Propagation Delay, Active to High-Z	VSR = 2.5V, $\overline{OE}$ L to H, C_L = 50 pF,					
		Data = L, R_L to 5V, Output to 0.5V			50	I	ns
		Data = H, R_L to 0V, Output to 4.5V			50	I	ns

EL2021C
Monolithic Pin Driver

Pin Description Table

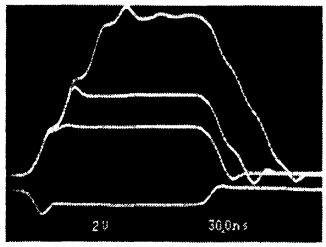
Pin #	Name	Description
1	GND	System ground.
2	$\overline{E}$	$\overline{\text{Enable}}$ control input. A logic low allows normal operation; a logic high puts the device into power down mode. No output levels are defined in powerdown nor does the output behave as a high impedance.
3	$\overline{OE}$	$\overline{\text{Output Enable}}$ input. A logic low sets the output to low-impedance driver mode; a logic high places the output into a high-impedance state.
4	V_{CL}	Lower analog control input. When Data = $\overline{OE}$ = $\overline{E}$ = L, the V_{CL} level is output as V_{OUT} (assuming $V_{CL} < V_{CH}$).
5	B−	System power supply. The EL2021 uses this pin as a negative output current monitor connection. Little current is drawn from this pin, transient or static.
6	$I_{sense}-$	Negative output current monitor input.
7	V−	Negative power supply. Because all negative output drive currents come from this pin (as much as 60 mA transiently), good bypassing is essential.
8	Drive−	Output to external pnp transistor base.
9	V_{OUT}	High-current input and output, depending on $\overline{OE}$.
10	Drive+	Output to external npn transistor base.
11	Sense Out	Logic output which signals that a high + or − output current is flowing.
12	V+	Positive power supply. Like V−, it should be well bypassed.
13	$I_{sense}+$	Positive output current monitor input.
14	B+	System power supply, similar to B−.
15	V_{CH}	Higher analog control input. When Data = H and $\overline{OE}$ = $\overline{E}$ = L, the V_{CH} level is output as V_{OUT} (assuming $V_{CH} > V_{CL}$).
16	VSR	Slew rate control input. A 1V level on this pin causes the output to slew at 100 V/μs, 0.5V causes a slew rate of 50 V/μs, etc.
17	Data	Output level control input. This pin digitally selects V_{CL} or V_{CH} as the output voltage when $\overline{OE}$ = $\overline{E}$ = L.
18	N/C	Not Connected.

Typical Performance Curves



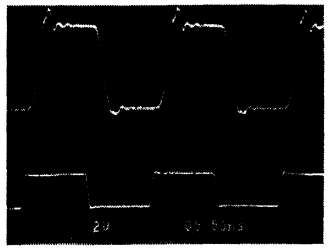
2021-3

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 50 pF, VSR = 1V.



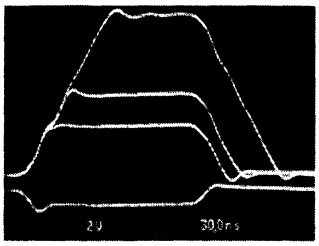
2021-4

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V.



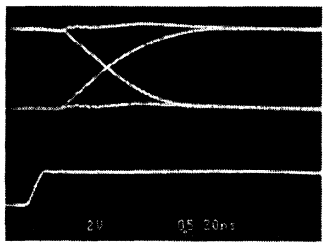
2021-5

Output waveshapes with 5 MHz data rate. C1 = 50 pF, VSR = 4V.



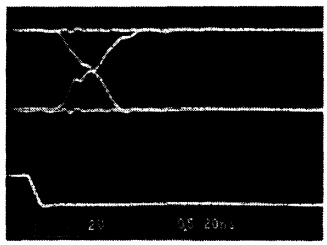
2021-6

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V, and overcompensated with 22 pF from each drive pin to ground.



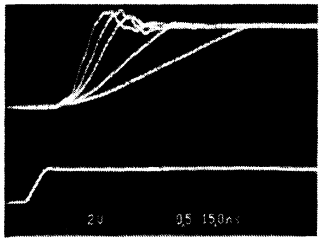
2021-7

Family of output waveshapes from active H, L to high-impedance H, L.



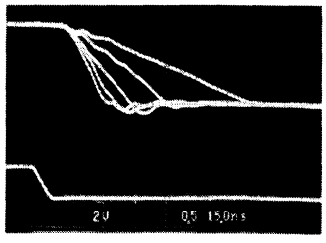
2021-8

Family of output waveshapes from high-impedance H, L to active H, L.



2021-9

Family of + output edges, 0V to 5V for VSR = 0.5V, 1V, 2V, 3V, 5V.



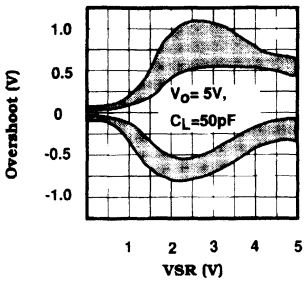
2021-10

Family of—output edges, 5V to 0V or VSR = 0.5V, 1V, 2V, 3V, 5V.

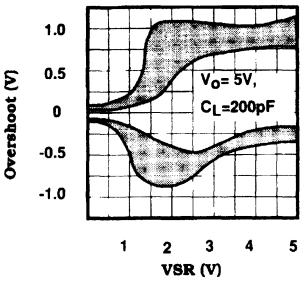
EL2021C
Monolithic Pin Driver

Typical Performance Curves — Contd.

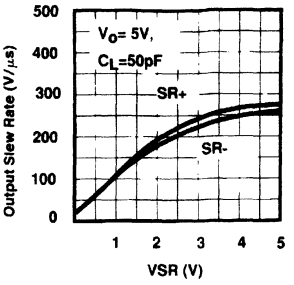
Overshoot vs VSR



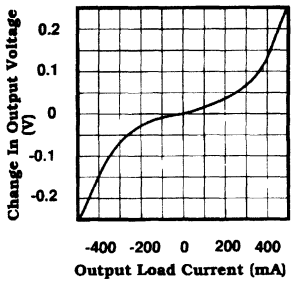
Overshoot vs VSR



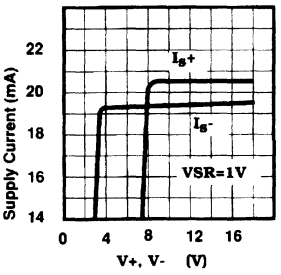
Slew Rate vs VSR



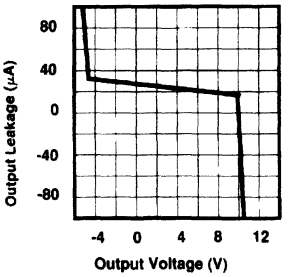
V_{OUT} vs Load Current



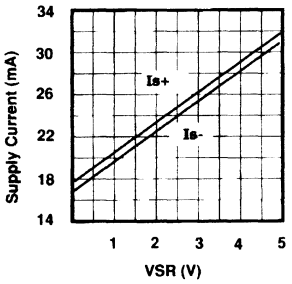
Supply Current vs Supply Voltage



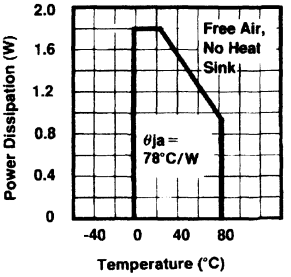
Tri-State Leakage vs Output Voltage



Supply Current vs VSR



Power Dissipation vs Temperature



2021-11

Applications Information

Output Stage

To meet the requirements of low output impedance, wide bandwidth, and large capacitive load driving capability, the EL2021 has a fairly exotic output stage. Figure 1 shows a simplified schematic of the circuit, only applicable in normal, low impedance mode. External transistors are used to handle the large load currents and peak power dissipations. Since there is no need for good AC crossover distortion performance in a pin driver, the output transistors are operated class C. That is, for small output currents, neither output transistor will conduct bias current, and when load currents do flow, one of the devices is off. This is accomplished by biasing the output transistors from Schottky diodes D1 and D2. In operation, the diode forward voltage is about 0.4V, whereas the "on" output transistor will have a V_{BE} of 0.6V. This leaves only 0.2V across the "off" transistor's base-emitter junction, not nearly enough to cause bias currents to flow in it. Schottky diodes have a temperature drift similar to silicon transistors, so the class C bias maintains over temperature. One caution is that the diodes are in the IC package and are thermally separate from the transistors, so there can exist temperature differences between packages that can cause thermal runaway. Runaway is avoided as long as the external transistors are not hotter than the EL2021 package by more than 80°C. The only way runaway has been induced as of this writing is to use "freeze spray" on the IC package while the output transistors are very hot.

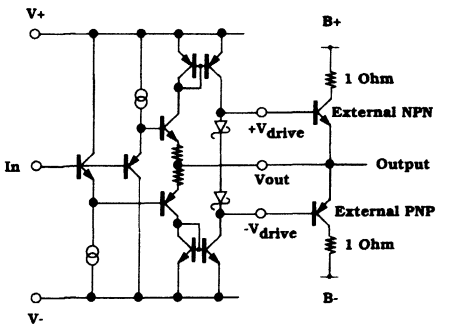


Figure 1. Simplified Output Stage (Normal Mode)

This circuit allows the external transistors to run from B+ and B− supplies that are of less voltage than V+ and V− to conserve power. Reducing B± supplies also reduces dissipations in the output devices themselves. B+ is typically made K volts more than V_{CH} and B− made K volts more negative than V_{CL}. Ideally K is made as small as possible to minimize output transistor dissipation, but two factors limit how small K can be. These factors are both related to the fact that transistors have two collector resistance numbers: "hard" and "soft" saturation resistance. As a transistor begins to saturate at high collector currents and small collector-emitter voltages, minority carriers begin to be generated from the base-collector junction. These carriers act as more collector dopant and actually reduce effective series collector resistance. At conditions of heavy saturation, the collector is flooded with minority carriers and exhibits minimum collector resistance. In this way, small geometry transistors like the 2N2222 and 2N2907 devices have excellent collector-emitter voltage drops at high currents, but are actually still in heavy saturation for 1V-2V drops. This "soft" saturation shows up as reduced beta at high currents and moderate V_{CE}'s as well as very poor AC performance. A transistor may exhibit an f_t of only 2 MHz in soft saturation when, like the 2N2222, it gives 300 MHz in non-saturated mode. The EL2021 requires the output transistors to have an f_t of at least 200 MHz to prevent degradation in overshoot, slew rate into heavy loads, and tolerance of heavy output capacitance. With a K of 3.2V and 1Ω collector resistors, almost all 2N2222 and 2N2907 devices perform well, but we have obtained devices from some vendors where the beta does indeed fall permaturely at reduced V_{CE} and high currents. It is important to characterize the external devices for the service that the EL2021 will be expected to provide.

The output stage of the EL2021 does not ring appreciably into a capacitive load in quiescent conditions, but it does ring while it slews. This is an unusual characteristic, but the output slews monotonically and the slew "ripple" does not cause problems in use. The slew ripple does cause a similar "ripple" in the overshoot-vs-VSR characteristic: the overshoot may decrease for slightly increasing VSR, then increase again for larger VSR's again. The overshoot-vs-VSR graphs

EL2021C
Monolithic Pin Driver

Applications Information — Contd.

presented in this data sheet thus reflect the range of overshoot rather than one particular device's wavy curve.

The typical 2N2222 and 2N2907 will deliver 750 mA into a short-circuit. This puts four watts of dissipation into the 2N2222 for V_{CH} = 5V. The npn can dissipate this power for a few tenths of a second as long as a metal-base TO-39 package is used. The small or non-metal-based packages have short thermal time constants and high thermal resistances, so they should withstand shorts for only a few milliseconds. The Sense Out signal should be used to control $\overline{OE}$, or $\overline{E}$, or reduce V_{CH} and V_{CL} to relieve the output devices from overcurrent conditions.

Transistors such as the MJE200 and MJE210 have very much improved collector resistances and high-current beta compared to the 2N2222 and 2N2907. Their f_t's are almost as good and sustain at higher currents, and high-current output accuracy will improve. They allow a K of 2V to reduce dissipations further, but short-circuit currents will be as much as two amperes! The geometries of these transistors are larger, and the added transistor capacitances will slow the maximum Slew Rates that the EL2021 can provide.

If transistors with f_t's less than 200 MHz are used, the EL2021 will need to be overcompensated. This is accomplished by connecting equal capacitors from the Drive pins to ground. These capacitors will range from 10 pF to 50 pF. The overcompensation will slow the maximum slew rate, but it will improve the overshoot and reactive load driving capability, and can be considered a useful technique.

Figure 2 shows the equivalent output stage schematic when the circuit is in high-impedance mode ($\overline{OE}$ = H). The external transistors have their base-emitter junctions each reverse-biased by a Schottky diode drop. A buffer amplifier copies the output voltage to give a bootstrapped bias for the Schottky stack. This scheme guarantees that the external transistors will be off for any output level, and the output leakage current is simply the bias current of the buffer.

The circuit works properly for AC signals up to 500 V/μs. Above this slew rate, the buffer cannot keep up and the external transistors may turn on transiently. Because of the bootstrap action, the output capacitance is less than 10 pF up to 10 MHz of small-signal bandwidth and 300 V/μs slew rate, increasing beyond these values. Adding overcompensation capacitors will degrade the slew rate that the output can withstand before current is drawn.

It is sometime necessary to provide a "snubber" network-a series R and C— to provide a local R.F. impedance for the buffer to look into. 330Ω and 56 pF should serve. Also, it is well to provide some DC path to ground (47k for instance) to bias the output stage when no actual circuit is connected to the EL2021 in high-impedance mode.

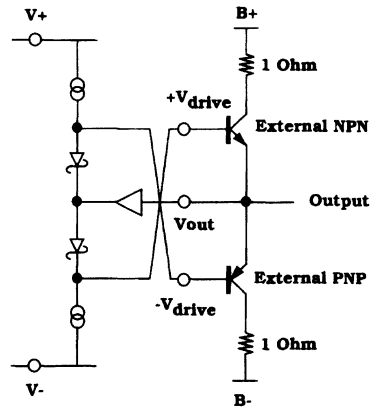


Figure 2. Simplified Output Stage (High-Impedance Mode)

Power Supplies

In typical operation, V+ and V− can be as much as ±15V and as little as V_{CH} +3V and V_{CL} −3V, respectively. When driving heavy output currents, however, it is wise to have 5V of headroom above V_{CH} and below V_{CL} to ensure no saturation of devices within the EL2021 and attendent waveshape distortions. Thus, for V_{CH} = 5V and V_{CL} = −2V, minimum operating voltages are +10, −7V. It is very important to bypass the supply terminals with low-inductance

Applications Information — Contd.

capacitors to ground, since the full base drive currents of the output transistors are derived from these supplies. Because the pulse currents can reach 60 mA, the capacitors should be at least a microfarad; 4.7 μF tantalum are ideal and require no small bypasses in parallel.

B+ and B− can be any voltage within V+ and V− and some amount previously discussed above V_{CH} and below V_{CL}. If V_{CH} or V_{CL} exceeds B+ or B−, very large internal fault currents can flow when the EL2021 attempts to bring an output transistor's base beyond the collector voltage. The bypassing care of the V± lines apply to the B± lines, as well as the fact that ampere currents can occur. Large (100 μF–500 μF) capacitors should be used to bypass perhaps every tenth EL2021.

The V_{CH}, V_{CL}, Data and $\overline{OE}$ lines should be driven locally so as to not pick up magnetic interference from the output. The inductance of interconnects to these lines can allow coupling to cause waveshape anomalies or even oscillations. If long lines are unavoidable, local 1k resistors or 50 pF–100 pF capacitors to ground can also serve the purpuse.

Data Pin

The slew rate of the input to the Data pin should be kept less than 1000 V/μs. Some feedthrough can occur for large Slew Rates which will distort the output waveshape. A 1k–2k resistor in series with the data pin will reduce feedthrough.

Current Sense

The output current is sensed by comparing the voltage dropped across the external shunt resistors to an internal 0.45V reference. The center of the trip level is adjusted for the particular output transistor betas listed in the data specifications. Transistors with less beta at high currents will cause the sense comparators to trip at slightly higher output currents. The 1Ω shunt resistors should be non-inductive. The family of wirewound resistors called "non-inductive" are too inductive for these shunts.

The response of the Sense Out can be thought of as slow attack and fast decay. A continuous overcurrent condition must last for at least 2 μs before Sense Out will go high, but will clear to low only about 200 ns after the overcurrent is withdrawn. This allows transient currents due to slewing capacitive load to not generate a flag. On the other hand, the output transistors will not be damaged with only a 2 μs system reaction time to a short-circuit.

Construction Practices

The major cautions in connecting to the EL2021 involve magnetic rather than capacitive parasitic concerns. The circuits can output as much as 100 A/μs. Even with normal Slew Rates and moderately large capacitive loads, the dI/dT can cause magnetic fields in harmless looking wires to fill adjacent lines with noise, and sometimes ringing or even sustained feedback. Thus, rules for wiring the EL2021 are:

(a) Keep leads short and large. Short wires are less inductive, as are wires with large surface area. The large surface area also reduces skin resistance at high frequencies, important at high currents (at 100 MHz, current penetrates only a few microns in meals).

(b) Use a ground plane. Due to inductance and skin effect, "ground" voltages will be different only inches apart on a copper ground plane. Individual wires do not create ground at high frequencies. The common "star" ground is a very bad idea for high-current and high-frequency circuits.

(c) Dress all wires against the ground plane. The magnetic fields that the wires would have generated will be intercepted by the ground plane and absorbed, thus reducing the wire's effective inductance. The capacitance added by this method is not important to EL2021 operation.

(d) The external transistors should have short interconnects to the EL2021, the collector shunt resistors, and the bypass capacitors. As previously stated, the shunt resistors must not be wire wound because of their inductance.

EL2021C
Monolithic Pin Driver

Applications Information — Contd.

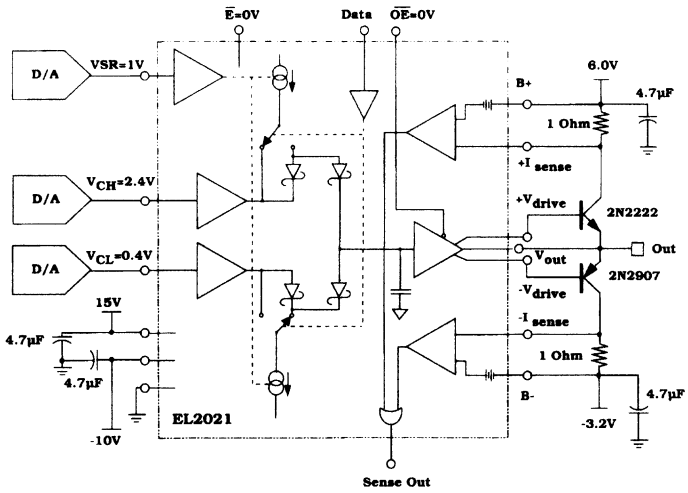
(e) The bypass capacitors should have low series resistance and inductance, but should not have a high Q. This may seem contradictory, but a 4.7 μF tantalum capacitor seems to work the best. An electrolytic capacitor should be added to help bolster the supply levels in the 0.1 μs–1 μs after a transition. No small capacitors are needed in parallel with the tantalums. The bypasses' ground returns are best connected to the area of ground inside the package outline to reduce the circulating current path length, if possible.

Using the EL2021 without External Transistors

By connecting both drive pins to the output pin, the EL2021 can be used as a stand-alone driver, not requiring the external transistors. The EL2021 is good for more than 50 mA in this mode. The output impedance rises to 12Ω, however, and the current sense and high-impedance mode are not available. The ripple seen in slew edges using the external transistors is largely absent from the standalone waveshapes; and overshoot is markedly improved at VSR > 1V, especially with large capacitive loads.

Typical Applications

100 V/μs High-Current Pin Driver Outputting TTL Levels



2021-14

Comparators

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

COMPARATOR SELECTION GUIDE

ELANTEC Part Number	Description	Typ Prop Delay (5 mV over-drive)	Typ Open Loop Gain (V/V)	Input Common Mode Range		Typ Input Bias Current	Max Supply Current		Temp Range	Packages
				(V_{CC} = ±15V)	(V_{CC} = ±5V)		Output Active	Output 3-State		
EL2018	Fast, High Voltage Comparator with Latch 3-State Output Monolithic	20 ns From Input to Output	40,000 (92 dB)	±12V Min	±3V Typ	±100 nA	+11/−18 mA	+7/−6.5 mA	−55°C to +125°C 0°C to +75°C	8-Pin CerDIP 8-Pin P-DIP 8-Pin TO-99
EL2019	Fast, High Voltage Comparator with Master Slave Flip-Flop, 3-State Output, Monolithic	6 ns Setup, 20 ns From Clock to Output	150,000 (103 dB)	±12V Min	±3V Typ	±100 nA	+12/−18 mA	+7/−8 mA	−55°C to +125°C 0°C to +75°C	8-Pin CerDIP 8-Pin P-DIP 8-Pin TO-99
EL2252	50 MHz Dual Comparator/Pin Receiver	7 ns (100 mV Overdrive)	8000	+10, −9 Min	N.A.	6 μA	+19/−20 mA (both Comparators)	N.A.	−55°C to +125°C 0°C to +75°C	14-Pin CerDIP 14-Pin P-DIP 20-Pin SOL

EL2018/EL2018C

Fast, High Voltage Comparator with Transparent Latch

Features

- Fast response time—20 ns
- Wide input differential voltage range—24V to ±15V supplies
- Precision input stage—V_{OS} = 1 mV
- Low input bias current—I_B = 100 nA
- Low input offset current—I_{OS} = 30 nA
- ±4.5V to ±18V supplies
- 3-State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain—40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2018CH	0°C to +75°C	TO-99	MDP0004
EL2018CJ	0°C to +75°C	CerDIP	MDP0010
EL2018CN	0°C to +75°C	P-DIP	MDP0031
EL2018H	−55°C to +125°C	TO-99	MDP0004
EL2018H/883B	−55°C to +125°C	TO-99	MDP0004
EL2018J	−55°C to +125°C	CerDIP	MDP0010
EL2018J/883B	−55°C to +125°C	CerDIP	MDP0010

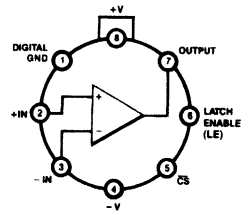
General Description

The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

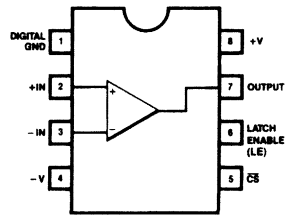
Connection Diagrams

TO-99 Metal Can



2018-1

8-Pin CerDIP
8-Pin Plastic DIP



2018-2

Top View

EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies		EL2018	−55°C to +125°C
				EL2018C	0°C to +75°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_J	Operating Junction Temperature	
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		Ceramic DIP Package,	
P_D	Maximum Power Dissipation			Metal Can Package	175°C
	(Note 4—See Curves)			Plastic DIP Package	150°C
	CerDIP	1.5W	T_{ST}	Storage Temperature	−65°C to +150°C
	Metal Can	1.0W		Lead Temperature	
	Plastic DIP	1.25W		(Soldering, 10 seconds)	300°C
I_{OP}	Peak Output Current	50 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2018	EL2018C	
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_O = 1.4V	25°C		1.0	3	I	I	mV
		T_{MIN}, T_{MAX}			5	I	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		100	300	I	I	nA
		T_{MIN}, T_{MAX}			500	I	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	I	nA
		T_{MIN}, T_{MAX}			250	I	III	nA
CMRR	Common Mode Rejection Ratio (Note 2)	25°C	85	105		I	I	dB
		T_{MIN}, T_{MAX}	80			I	III	dB
PSRR	Power Supply Rejection Ratio (Note 3)	25°C	85	100		I	I	dB
		T_{MIN}, T_{MAX}	80			I	III	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	I	V
		T_{MIN}, T_{MAX}	±12			I	III	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	25°C	15	40		I	I	V/mV
		T_{MIN}, T_{MAX}	10			I	III	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	25°C	−0.05	0.15	0.4	I	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	I	III	V

DC Electrical Characteristics V_S = ±15V unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2018	EL2018C	
V_{oh}	Output Voltage Logic High V_S = ±15V	25°C	3.5	4.0	4.65	I	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	I	III	V
	V_S = ±5V	25°C	2.4			I	I	V
	V_S = ±5V	T_{MIN}	2.4			I	III	V
	V_S = ±5V	T_{MAX}	2.4			I	III	V
V_{odis1}	V_{OUT} Range, Disabled, I_{OL} = −1 mA V_S = ±15V	25°C	4.65			I	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	4.65			I	II	V
	V_S = ±5V	25°C		3.5		V	V	V
V_{odis2}	V_{OUT} Range, Disabled, I_{OL} = 1 mA V_S = ±5V to ±15V	ALL	−0.3	−1		I	II	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	25°C	2.0			I	I	V
		T_{MIN}, T_{MAX}	2.0			I	III	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	I	V
		T_{MIN}, T_{MAX}			0.8	I	III	V
I_{in}	LE or $\overline{CS}$ Inputs Logic Input Current V_{IN} = 0V to 5V	25°C			±200	I	I	µA
		T_{MIN}, T_{MAX}			±300	I	III	µA
I_{s+en}	Positive Supply Current Enabled	25°C		8.4	10	I	I	mA
		T_{MIN}, T_{MAX}			11	I	III	mA
I_{s+dis}	Positive Supply Current Disabled	25°C		4.7	6	I	I	mA
		T_{MIN}, T_{MAX}			7	I	III	mA
I_{s-en}	Negative Supply Current Enabled	25°C		13.0	17	I	I	mA
		T_{MIN}, T_{MAX}			18	I	III	mA
I_{s-dis}	Negative Supply Current Disabled	25°C		5.0	6.5	I	I	mA
		T_{MIN}, T_{MAX}			6.5	I	III	mA

EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

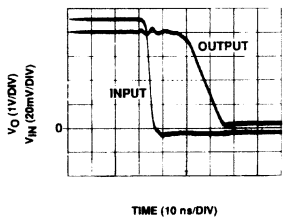
AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level		Units
					EL2018	EL2018C	
T_{pd}	Propagation Delay, 5 mV Overdrive		20	30	I	III	ns
T_s	Setup Time		6	12	I	III	ns
T_h	Hold Time		−2	0	I	III	ns
T_{un}	Unlatch Time		23	30	I	III	ns
T_{mpw}	Minimum Clock Pulse Width		12		V	V	ns
T_{en}	Output 3-State Enable Delay		40	70	I	III	ns
T_{dis}	Output 3-State Disable Delay		150	300	I	III	ns

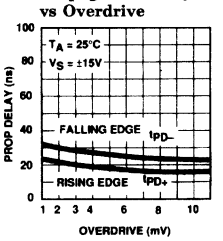
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = 12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to $\pm 15V$.
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

Typical AC Performance Curves

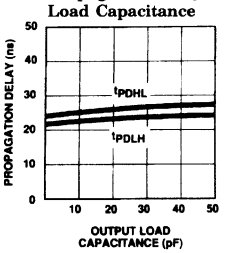
Propagation Delay (−) 5 mV Overdrive



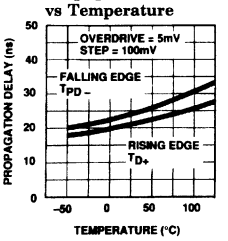
Propagation Delay vs Overdrive



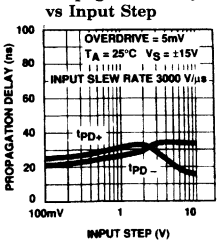
Propagation Delay vs Load Capacitance



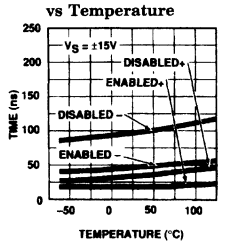
Propagation Delay vs Temperature



Propagation Delay vs Input Step



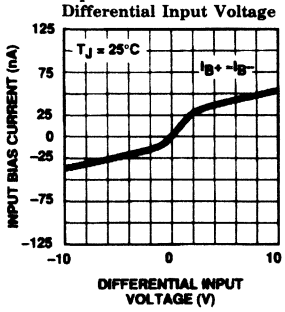
Enabled/Disabled Time vs Temperature



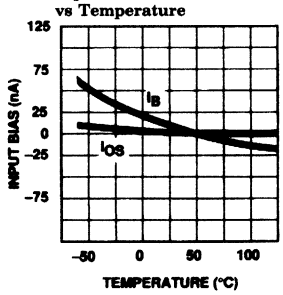
2018-3

Typical AC Performance Curves — Contd.

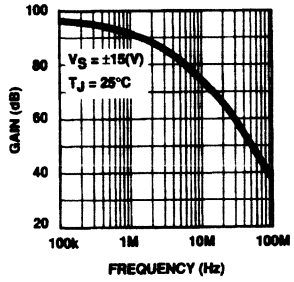
Input Bias Current vs Differential Input Voltage



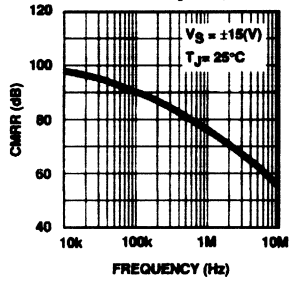
Input Bias Current vs Temperature



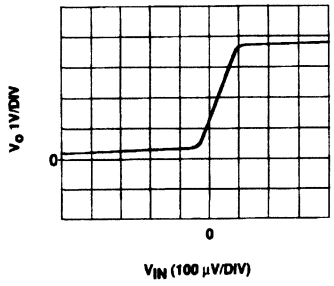
Open-Loop Gain vs Frequency



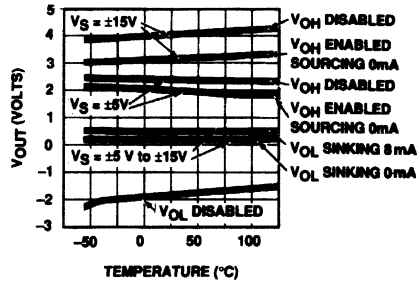
CMRR vs Frequency



V_O/V_I Transfer Characteristic



V_{OUT} vs Temperature



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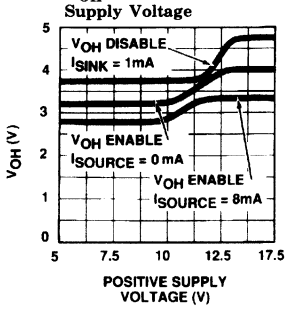
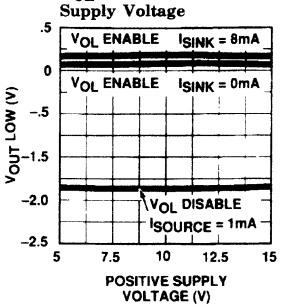
EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Typical Performance Curves — Contd.

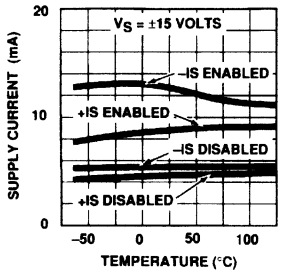
V_{OH} vs Positive Supply Voltage



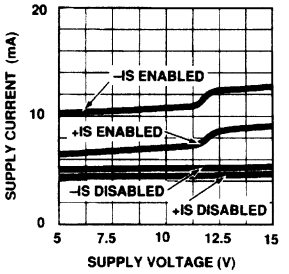
V_{OL} vs Positive Supply Voltage



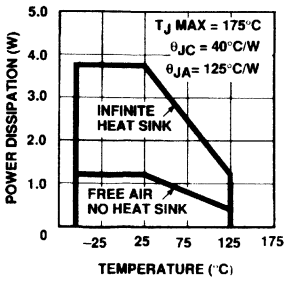
Supply Current vs Temperature



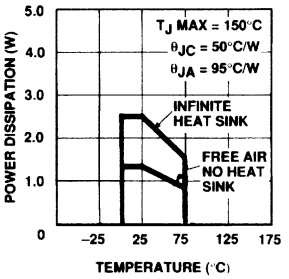
Supply Current vs Supply Voltage



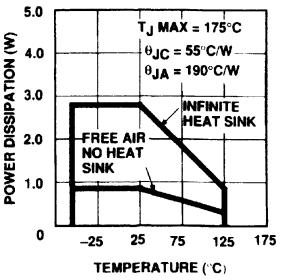
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



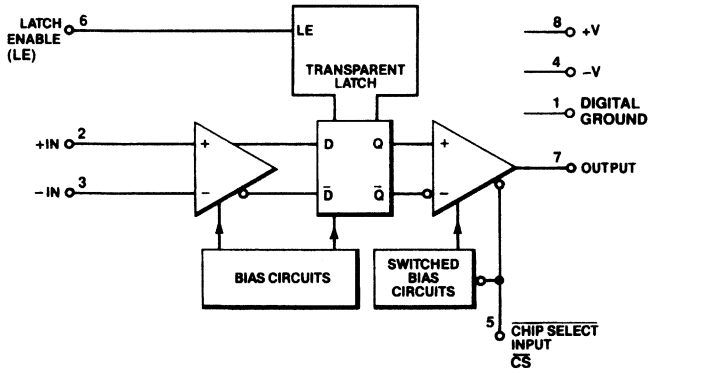
8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



2018-5

EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Block Diagram



Function Table

Inputs (time n−1)				Internal Q	Notes	Output
+IN	−IN	$\overline{CS}$	LE			
+	−	L	L	H	Normal Comparator Operation	H
−	+	L	L	L		L
+	−	H	L	H	Internal Normal Comparator Operation	High Z
−	+	H	L	L	Output Power Down Mode	High Z
X	X	L	H	Qn−1	Data Retained in Latch	Qn−1
X	X	H	H	Qn−1	Data Retained in Latch Power Down Mode	High Z

Application Hints

Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2018 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.1 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

Front End

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12V minimum) and differental voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Application Hints — Contd.

Recovery from Large Overdrives
Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

Input Slew Rate
All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

Latch
The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The $\overline{CS}$ input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

Output Stage
The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature
The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

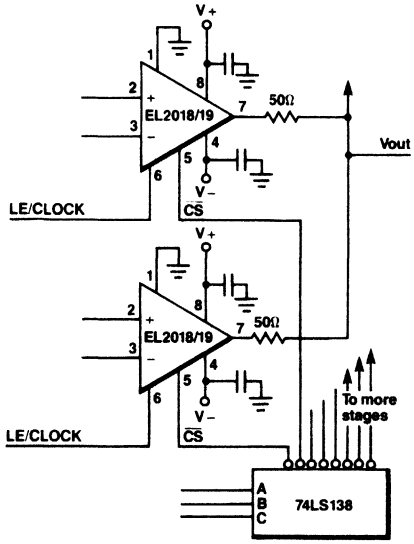
Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

System Design Considerations
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master/slave flip flop.

Device Functions
The various operating states of the EL2018 are described in the function table on page 5-9.

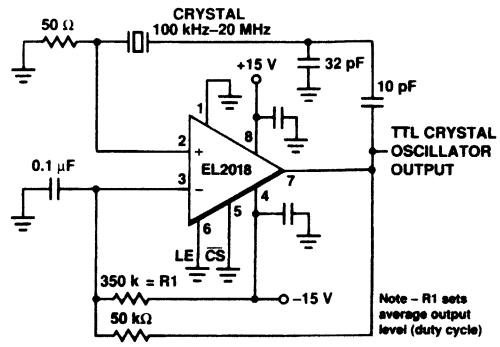
Typical Applications

Using the Power Down/ 3-State Feature



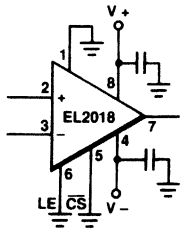
2018-7

Series Resonant Crystal Oscillator



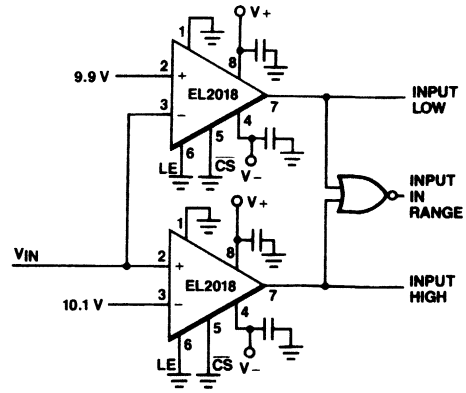
2018-8

Using the EL2018 in the Transparent Mode (Latch Not Used)



2018-9

A Wide Input Range Window Comparator

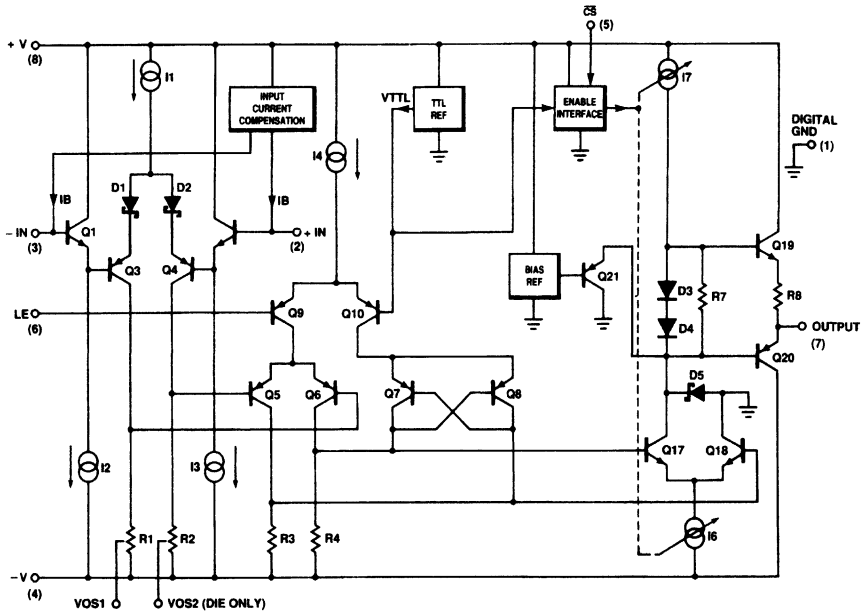


2018-10

V_{IN} Range +12V to −12V
with V_S = ±15V

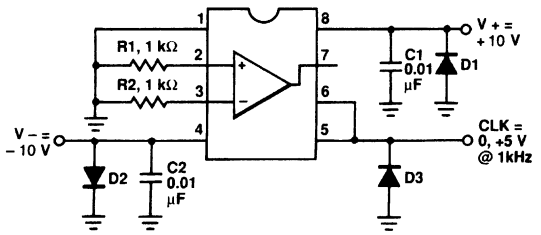
EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Equivalent Schematic



2018-11

Burn-In Circuit



2018-12

Pin numbers are for DIP packages.
All packages use the same schematic.

EL2019/EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Features

- Comparator cannot oscillate
- Fast response—5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range—24V on ±15V supplies
- Wide input common mode voltage range—±12V
- Precision input stage—V_{OS} = 1.5 mV
- Low input bias current—100 nA
- Low input offset current—30 nA
- ±4.5V to ±18V supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty ≈ 30 μV)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

Applications

- Analog to digital converters
- ATE pin receiver
- Zero crossing detector
- Window detector
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2019CH	0°C to +75°C	TO-99	MDP0004
EL2019CJ	0°C to +75°C	CerDIP	MDP0010
EL2019CN	0°C to +75°C	P-DIP	MDP0006
EL2019H	−55°C to +125°C	TO-99	MDP0004
EL2019H/883B	−55°C to +125°C	TO-99	MDP0004
EL2019J	−55°C to +125°C	CerDIP	MDP0010
EL2019J/883B	−55°C to +125°C	CerDIP	MDP0010

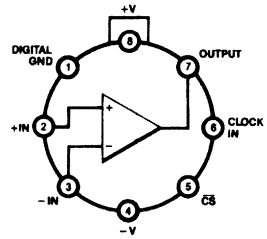
General Description

The EL2019 offers a new feature previously unavailable in a comparator before—a master/slave edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see *Elantec's Military Processing-Monolithic Products.*

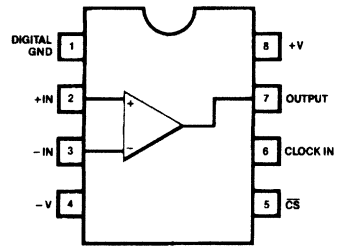
Connection Diagrams

TO-99 Metal Can



2019-1

8-Pin CerDIP
8-Pin Plastic DIP



2019-2

Top View

EL2019/EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies		EL2019	−55°C to +125°C
				EL2019C	0°C to +75°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_J	Operating Junction Temperature	
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		Ceramic DIP Package,	
P_D	Maximum Power Dissipation (Note 3 - See Curves)			Metal Can Package	175°C
	CerDIP	1.5W		Plastic DIP Package	150°C
	Metal Can	1.0W	T_{ST}	Storage Temperature	−65°C to +150°C
	Plastic DIP	1.25W		Lead Temperature	
I_{OP}	Peak Output Current	50 mA		(Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, unless otherwise specified

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2019	EL2019C	
V_{OS}	Input Offset Voltage	25°C		1.5	5	I	I	mV
	V_{CM} = 0V, V_O Transition Point	T_{MIN}, T_{MAX}			7	I	III	mV
I_B	Input Bias Current	25°C		±100	±300	I	I	nA
	V_{CM} = 0V, Pin 2 or 3	T_{MIN}, T_{MAX}			±500	I	III	nA
I_{OS}	Input Offset Current	25°C		30	150	I	I	nA
	V_{CM} = 0V	T_{MIN}, T_{MAX}			250	I	III	nA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	75	90		I	I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	75	95		I	I	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	I	V
		T_{MIN}, T_{MAX}	±12			I	III	V
V_{uncer}	Input Uncertainty Range			30		V	V	μV/RMS
V_{OL}	Output Voltage Logic Low	25°C	−0.05	0.15	0.4	I	I	V
	I_{OL} = 8 mA and I_{OL} = 0 mA)	T_{MIN}, T_{MAX}	−0.1		0.4	I	III	V
V_{OH}	Output Voltage Logic High							
	V_S = ±15V	25°C	3.5	4.0	4.65	I	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	I	III	V
	V_S = ±5V	25°C	2.4			I	I	V
	V_S = ±5V	T_{MIN}	2.4			I	III	V
	V_S = ±5V	T_{MAX}	2.4			I	III	V

DC Electrical Characteristics $V_S = \pm 15V$, unless otherwise specified — Contd.

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2019	EL2019C	
V_{ODIS1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA							
	$V_S = \pm 15V$	25°C	4.65			I	I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			I	III	V
	$V_S = \pm 5V$	25°C		3.65		V	V	V
V_{ODIS2}	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $+15V$	All	−0.3	−1		I	II	V
V_{INH}	Clock or $\overline{CS}$ Inputs	25°C	2			I	I	V
	Logic High Input Voltage	T_{MIN}, T_{MAX}	2			I	III	V
I_{IN}	Clock or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ and $V_{IN} = 5V$	25°C			±200	I	I	μA
		T_{MIN}, T_{MAX}			±300	I	III	μA
V_{INL}	Clock or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	I	V
		T_{MIN}, T_{MAX}			0.8	I	III	V
I_{S+EN}	Positive Supply Current Enabled	25°C		8.8	11	I	I	mA
		T_{MIN}, T_{MAX}			12	I	II	mA
I_{S+DIS}	Positive Supply Current Disabled	25°C		4.9	6	I	I	mA
		T_{MIN}, T_{MAX}			7	I	II	mA
I_{S-EN}	Negative Supply Current Enabled	25°C		14.5	17	I	I	mA
		T_{MIN}, T_{MAX}			18	I	II	mA
I_{S-DIS}	Negative Supply Current Disabled	25°C		6.4	8.0	I	I	mA
		T_{MIN}, T_{MAX}			8.0	I	II	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Limits			Test Level		Units
		Min	Typ	Max	EL2019	EL2019C	
T_S	Setup Time 5 mV Overdrive		12	20	I	II	ns
T_H	Hold Time		−3	0	I	II	ns
T_{OPOUT}	Clock to Output Delay		20	25	I	II	ns
T_{OPMIN}	Minimum Clock Width		7		V	V	ns
T_{EN}	Output 3-State Enable Delay		40	70	I	II	ns
T_{DIS}	Output 3-State Disable Delay		150	300	I	II	ns

Note 1: $V_{CM} = +12V$ to $-12V$.

Note 2: $V_S = \pm 5V$ to $\pm 15V$.

Note 3: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2232/EL2232C

60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Features

- 60 MHz −3 dB bandwidth, $A_V = 1$
- 50 MHz −3 dB bandwidth, $A_V = 2$
- 3 mV offset voltage
- 10 μV/°C Offset Drift
- 600 V/μs Slew Rate
- 30 mA output current
- Drives ±12.5 into 500Ω load
- Characterized at ±5V and ±15V
- 9.5 mA supply current
- 125 ns settling time to 0.02% for 10V step
- Output short circuit protected
- Low cost
- Dual version of the EL2020

Applications

- Video amplifiers
- Video distribution amplifiers
- Fast, precise D/A converter output amplifier
- High speed A/D input amplifier
- CCD imager amplifier
- Ultrasound and sonar systems

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2232CN	0°C to +75°C	8-Pin P-DIP	*MDP0031
EL2232CM	0°C to +75°C	16-Lead SOL	*MDP0027
EL2232J	−55°C to +125°C	8-Pin CerDIP	*MDP0001
EL2232J/883B	−55°C to +125°C	8-Pin CerDIP	*MDP0001

*See 1990 Databook for package outlines.

General Description

The EL2232 is a dual monolithic operational amplifier with a 60 MHz unity gain bandwidth. Built using Elantec's in-house high speed bipolar process, the dual amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier. The EL2232 design was optimized to achieve fast rise and fall times and short settling times.

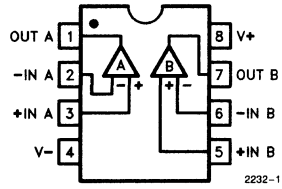
The EL2232 is a dual version of the popular EL2020, demonstrating similar AC performance, yet the 2 amplifiers of the EL2232 consume no more power than a single EL2020.

The EL2232 operates on standard ±15V supplies, swings ±12.5V at its output into a 500Ω load. The EL2232 was designed and is characterized to operate with supply voltages between ±5V and ±15V. Its low power consumption and short circuit protection make the EL2232 a safe and reliable amplifier to be used in commercial, industrial and military applications where the part is available screened to MIL-STD-883.

Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

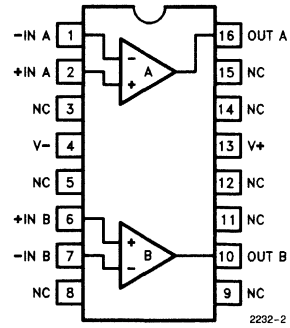
Connection Diagrams

CerDIP Package



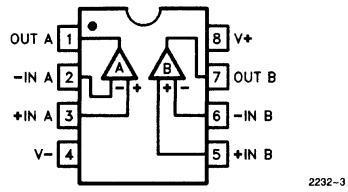
Top View

SOL Package



Top View

Plastic DIP



Top View

EL2232/EL2232C

60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage	±15V or V_S		Ceramic Packages	175°C
ΔV_{IN}	Differential Input Voltage	±6V		Plastic Packages	150°C
P_D	Maximum Power Dissipation	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
I_{IN}	Input Current	±10 mA		Lead Temperature	
I_{OP}	Peak Output Current	Short Circuit Protected		DIP Package	
	Output Short Circuit Duration (Note 1)	Continuous		(Soldering, <10 seconds)	300°C
				SOL Package	
T_A	Operating Temperature Range			Vapor Phase (60 seconds)	215°C
	EL2232	−55°C to +125°C		Infrared (15 seconds)	220°C
	EL2232C	0°C to +75°C			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±15V, R_L = 500Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level		Units
							EL2232	EL2232C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	7	I	I	mV
			T_{MIN}, T_{MAX}			10	I	III	mV
dV_{OS}/dT	Offset Voltage Drift		Full		10		V	V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		1.2	3	I	I	µA
			T_{MIN}, T_{MAX}			5	I	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	20	I	I	µA
			T_{MIN}, T_{MAX}			25	I	III	µA
$+R_{IN}$	+Input Resistance		Full	2	20		I	II	MΩ
C_{IN}	Input Capacitance		25°C		3		V	V	pF
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	56	63		I	II	dB
−ICMR	Input Current Common-Mode Rejection (Note 2)		25°C		0.25	0.75	I	I	µA/V
			T_{MIN}, T_{MAX}			1	I	II	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	66	80		I	II	dB
+IPSR	+Input Current Power Supply Rejection (Note 3)		25°C		0.03	0.06	I	II	µA/V
			T_{MIN}, T_{MAX}			0.1	I	III	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.06	0.2	I	II	µA/V
			T_{MIN}, T_{MAX}			0.3	I	III	µA/V
R_{OL}	Transimpedance ($dV_{OUT}/d\text{-}I_{IN}$) (Note 4)	V_S = ±5V, ±15V	25°C	1.2	4		I	II	MΩ
			T_{MIN}, T_{MAX}	0.9			I	III	MΩ

EL2232/EL2232C
60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Open Loop DC Electrical Characteristics
V_S = ±15V, R_L = 500Ω, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level		Units
							EL2232	EL2232C	
V_O	Output Voltage Swing	V_S = ±15V, R_L = 500Ω	Full	11.5	12.5		I	II	V
		V_S = ±5V, R_L = 500Ω	Full	2	2.5		I	II	V
I_{OUT}	Output Current	V_S = ±15V	Full	23	30		I	II	mA
		V_S = ±5V	Full		25		V	V	mA
I_S	Quiescent Supply Current		25°C		9.5	13	I	II	mA
			T_{MIN}, T_{MAX}			14	I	III	mA
I_{SC}	Short-Circuit Current	V_S = ±15V	25°C		50		V	V	mA
		V_S = ±5V	25°C		45		V	V	mA

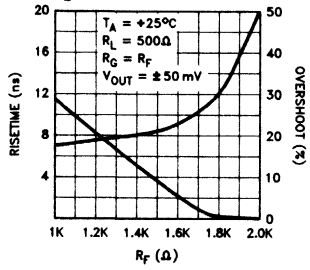
Closed Loop AC Electrical Characteristics
V_S = ±15V, A_V = +1, R_F = 1.5kΩ, R_L = 500Ω, T_A = 25°C

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level		Units
							EL2232	EL2232C	
SR	Slew Rate (Note 5)	A_V = +1	25°C	400	600		I	I	V/μs
		A_V = +10	25°C	500	650		I	I	Vμs
BW	−3 dB Bandwidth	A_V = −1	25°C		50		V	V	MHz
		A_V = +1	25°C		60		V	V	MHz
		A_V = +10	25°C		35		V	V	MHz
t_r, t_f	Rise Time, Fall Time	100 mV Step	25°C		8		V	V	ns
	A_V = +1, 10% to 90%	10V Step	25°C		21		V	V	ns
t_s	Settling Time (Note 6)	A_V = −1, 0.1%	25°C		85		V	V	ns
		0.02%	25°C		120		V	V	ns
		A_V = +1, 0.1%	25°C		85		V	V	ns
		0.02%	25°C		110		V	V	ns
		A_V = +10, 0.1%	25°C		85		V	V	ns
		0.02%	25°C		125		V	V	ns
CS	Channel Separation	100 kHz, R_L = 1MΩ	25°C		100		V	V	dB
dG	Differential Gain (Note 7)	R_L = 150Ω	25°C		0.1		V	V	% p-p
dPhase	Differential Phase (Note 7)	R_L = 150Ω	25°C		0.1		V	V	° p-p

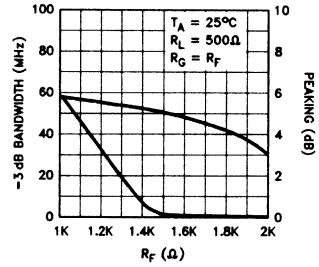
Note 1: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: V_{CM} = ±10V for V_S = ±15V. For V_S = ±5V, V_{CM} = ±2V.
Note 3: V_{OS} is measured at V_S = ±4.5V and at V_S = ±18V. Both supplies are changed simultaneously.
Note 4: R_L = 500Ω, V_O = ±10V for V_S = ±15V, V_O = ±2V for V_S = ±5V.
Note 5: V_O = ±10V, SR is tested at V_O = ±5V.
Note 6: Setting time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.
Note 7: NTSC (3.58 MHz) and PAL (4.43 MHz). See Differential Gain and Phase Test Circuit.

Typical Performance Curves

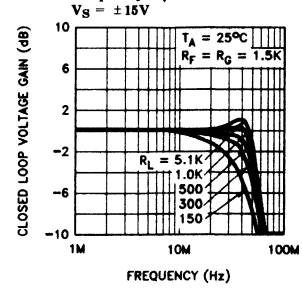
Rise Time and Overshoot vs R_F for $A_V = -1$, $V_S = \pm 15V$



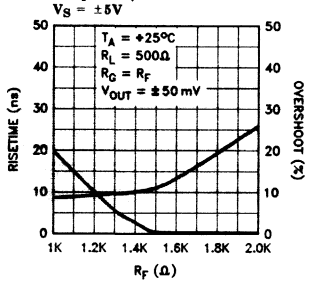
Bandwidth and Peaking vs R_F for $A_V = -1$, $V_S = \pm 15V$



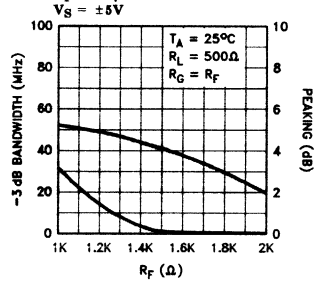
Voltage Gain vs Frequency $A_V = -1$, $V_S = \pm 15V$



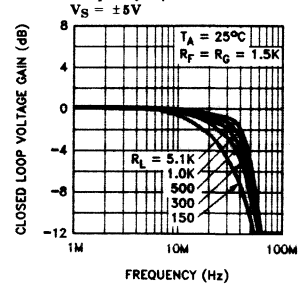
Rise Time and Overshoot vs R_F for $A_V = -1$, $V_S = \pm 5V$



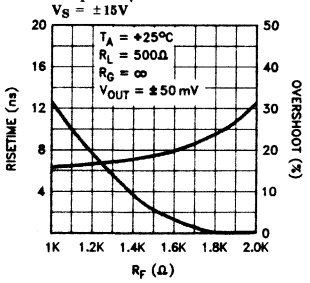
Bandwidth and Peaking vs R_F for $A_V = -1$, $V_S = \pm 5V$



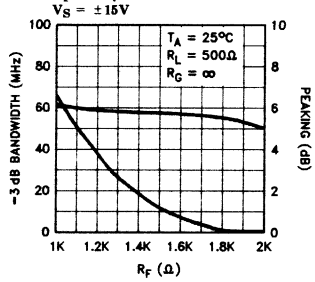
Voltage Gain vs Frequency $A_V = -1$, $V_S = \pm 5V$



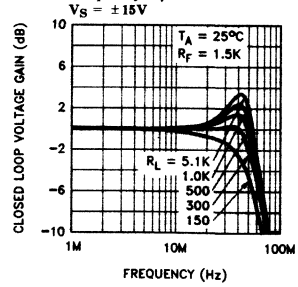
Rise Time and Overshoot vs R_F for $A_V = +1$, $V_S = \pm 15V$



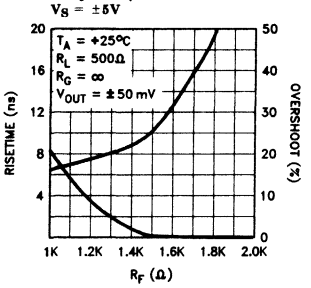
Bandwidth and Peaking vs R_F for $A_V = +1$, $V_S = \pm 15V$



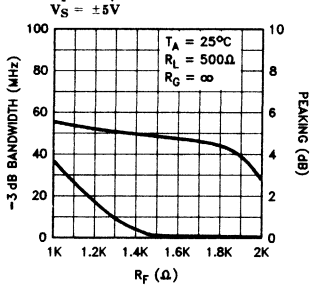
Voltage Gain vs Frequency $A_V = +1$, $V_S = \pm 15V$



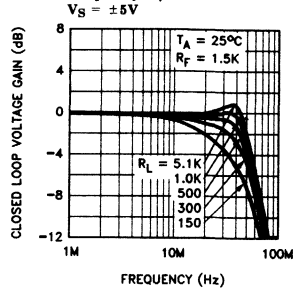
Rise Time and Overshoot vs R_F for $A_V = +1$, $V_S = \pm 5V$



Bandwidth and Peaking vs R_F for $A_V = +1$, $V_S = \pm 5V$



Voltage Gain vs Frequency $A_V = +1$, $V_S = \pm 5V$



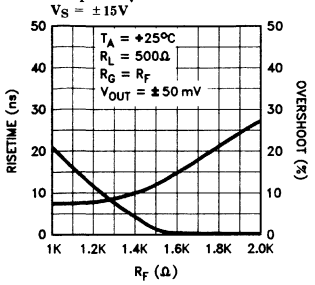
2232-4

EL2232/EL2232C

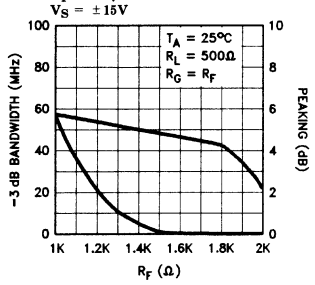
60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Typical Performance Curves — Contd.

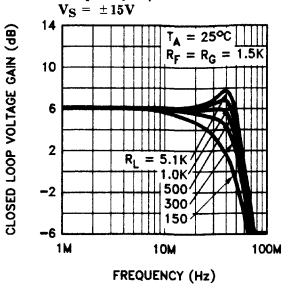
Rise Time and Overshoot vs R_F for A_V = +2, V_S = ±15V



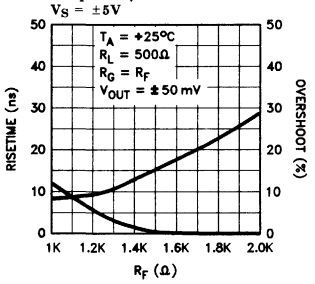
Bandwidth and Peaking vs R_F for A_V = +2, V_S = ±15V



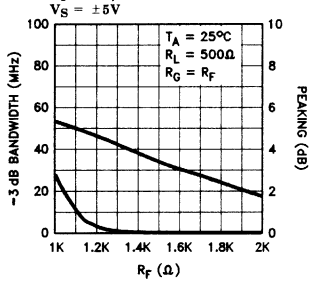
Voltage Gain vs Frequency A_V = +2, V_S = ±15V



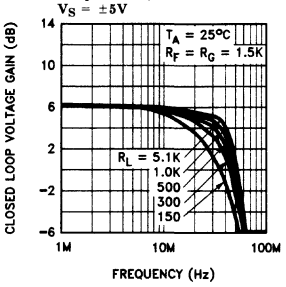
Rise Time and Overshoot vs R_F for A_V = +2, V_S = ±5V



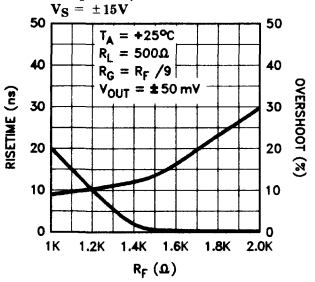
Bandwidth and Peaking vs R_F for A_V = +2, V_S = ±5V



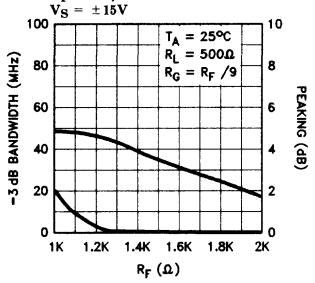
Voltage Gain vs Frequency A_V = +2, V_S = ±5V



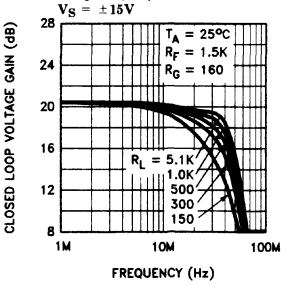
Rise Time and Overshoot vs R_F for A_V = +10, V_S = ±15V



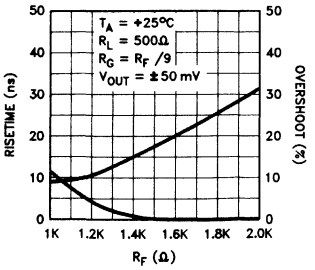
Bandwidth and Peaking vs R_F for A_V = +10, V_S = ±15V



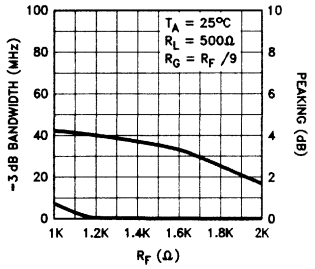
Voltage Gain vs Frequency A_V = +10, V_S = ±15V



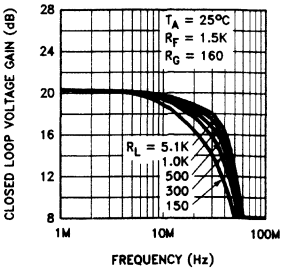
Rise Time and Overshoot vs R_F for A_V = +10, V_S = ±5V



Bandwidth and Peaking vs R_F for A_V = +10, V_S = ±5V



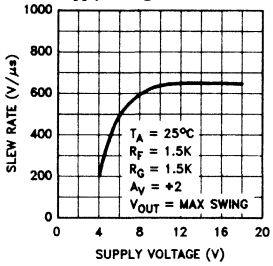
Voltage Gain vs Frequency A_V = +10, V_S = ±5V



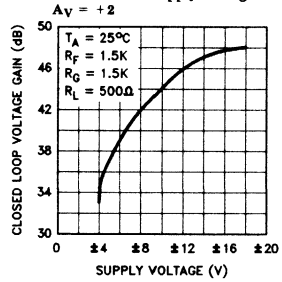
2232-5

Typical Performance Curves — Contd.

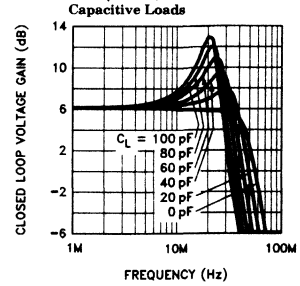
Slew Rate vs Supply Voltage



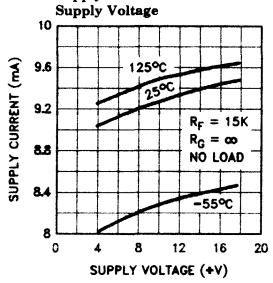
Small-Signal −3 dB Bandwidth vs Supply Voltage A_V = +2



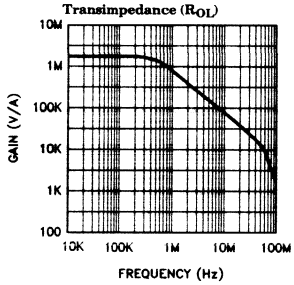
Voltage Gain vs Frequency for A_V = +2, Various Capacitive Loads



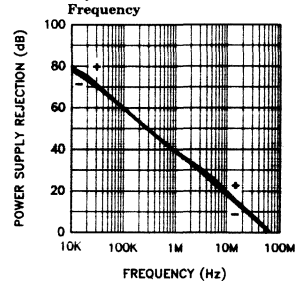
Supply Current vs Supply Voltage



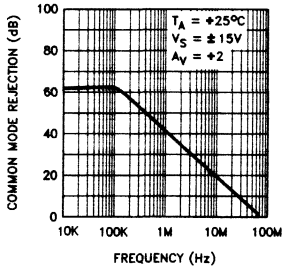
Transimpedance (R_{OL})



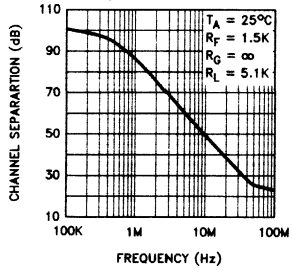
Power Supply Rejection vs Frequency



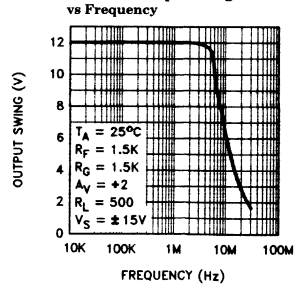
Common Mode Rejection vs Frequency



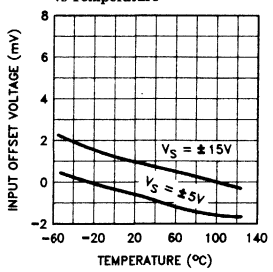
Channel Separation vs Frequency



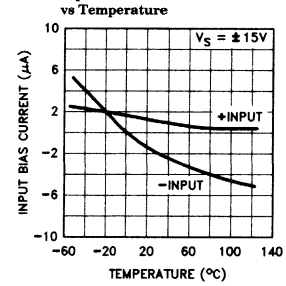
Maximum Output Swing vs Frequency



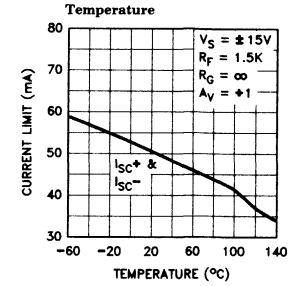
Input Offset Voltage vs Temperature



Input Bias Current vs Temperature



Current Limit vs Temperature



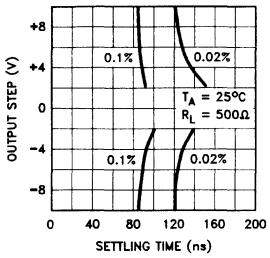
2232-6

EL2232/EL2232C

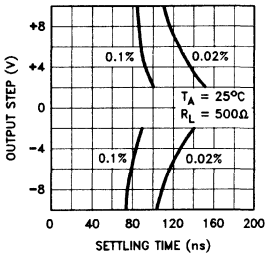
60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Typical Performance Curves — Contd.

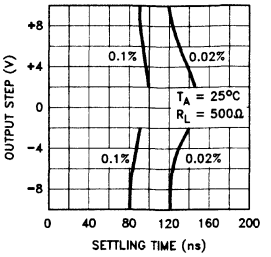
Settling Time vs Output Swing
$A_V = -1$, $V_S = \pm 15V$



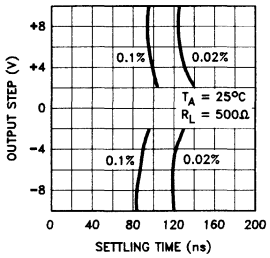
Settling Time vs Output Swing
$A_V = +1$, $V_S = \pm 15V$



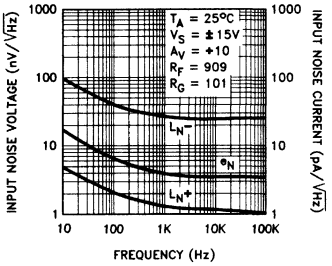
Settling Time vs Output Swing
$A_V = +2$, $V_S = \pm 15V$



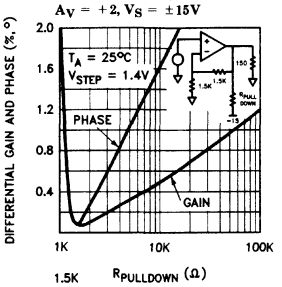
Settling Time vs Output Swing
$A_V = +10$, $V_S = \pm 15V$



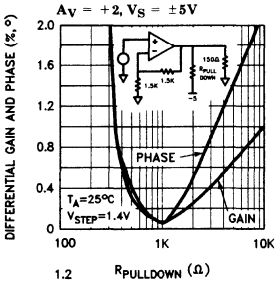
Equivalent Input Noise



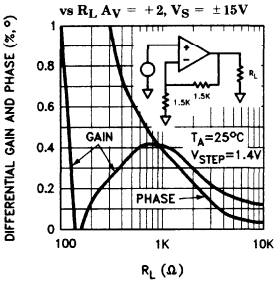
Differential Gain and Phase vs R Pulldown
$A_V = +2$, $V_S = \pm 15V$



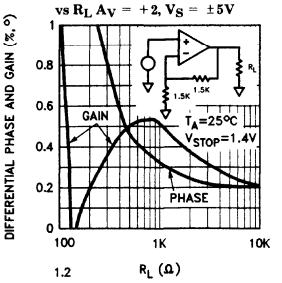
Differential Gain and Phase vs R Pulldown
$A_V = +2$, $V_S = \pm 5V$



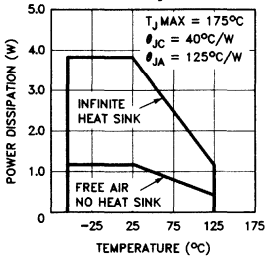
Differential Gain and Phase vs R_L $A_V = +2$, $V_S = \pm 15V$



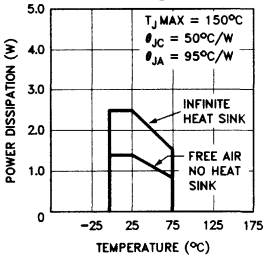
Differential Gain and Phase vs R_L $A_V = +2$, $V_S = \pm 5V$



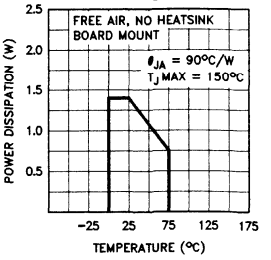
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



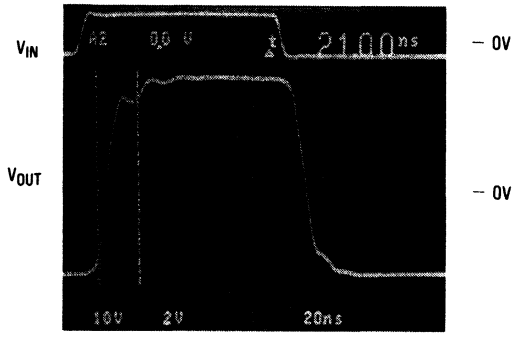
16-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2232-7

Typical Performance Curves — Contd.

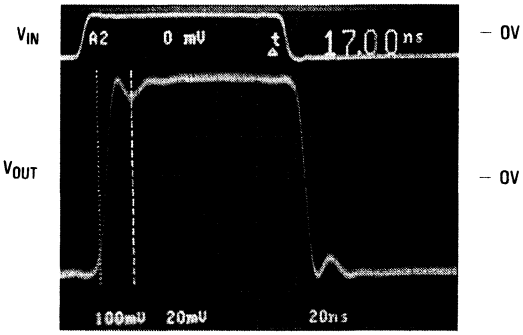
Large Signal Response



A_V = +1, R_F = 1.5k,
R_L = 500Ω, V_S = ±15V

2232-8

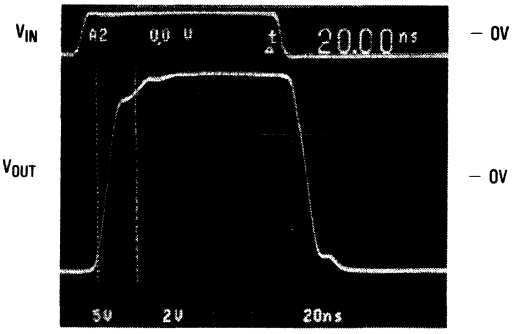
Small Signal Response



A_V = +1, R_F = 1.5k,
R_L = 500Ω, V_S = ±15V

2232-9

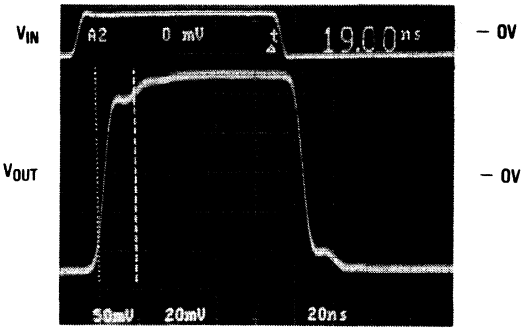
Large Signal Response



A_V = +2, R_F = R_G = 1.5k,
R_L = 500Ω, V_S = ±15V

2232-10

Small Signal Response



A_V = +2, R_F = R_G = 1.5k,
R_L = 500Ω, V_S = ±15V

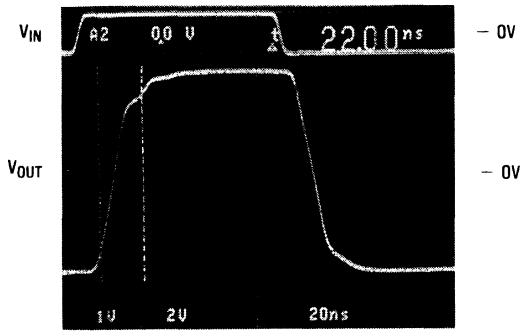
2232-11

5

EL2232/EL2232C
60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Typical Performance Curves — Contd.

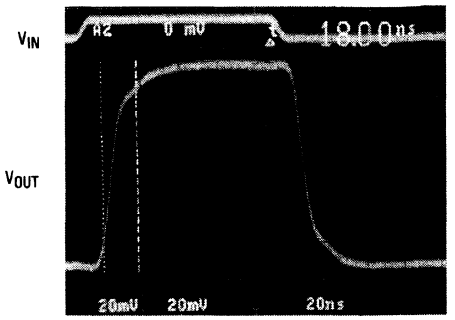
Large Signal Response



A_V = +10, R_F = 1.5k, R_G = 167,
R_L = 500Ω, V_S = ±15V

2232-12

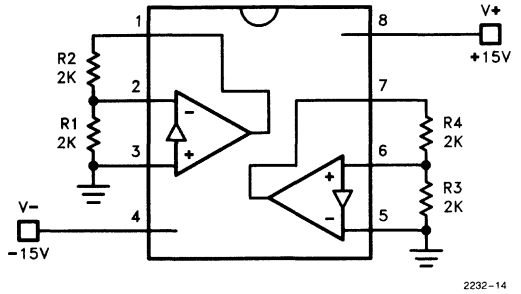
Small Signal Response



A_V = +10, R_F = 1.5k, R_G = 167,
R_L = 500Ω, V_S = ±15V,

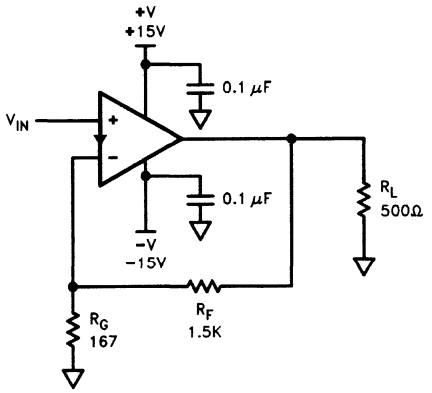
2232-13

Burn-In Circuit



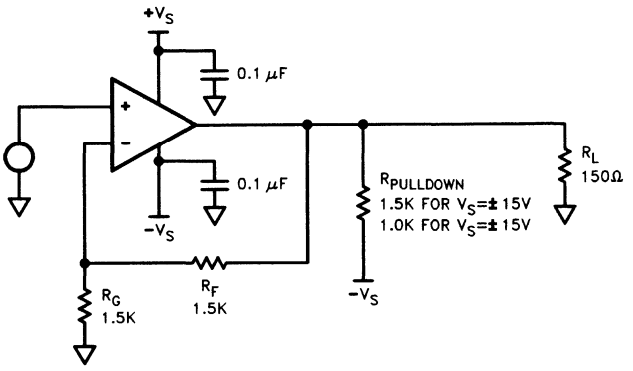
2232-14

Test Circuit



2232-15

Differential Gain and Phase Test Circuit



2232-16

Applications Information

Product Description

The EL2232 is a dual current-mode feedback amplifier similar to the industry-standard EL2020. Each of the EL2232's amplifiers has greater −3 dB bandwidth (60 MHz) and slew-rate (600 V/μs) than the EL2020, yet the total supply current for the EL2232 (9.5 mA) is only slightly more than the EL2020. Furthermore, the EL2232 has been characterized at both V_S = ±5V and V_S = ±15V.

With two amplifiers in a single package, the EL2232 allows 2-channel amplification with matched performance, as well as reduction of PC board area when compared to 2 single amplifiers. Designing with the EL2232 is simple, since in most applications it performs similarly to a conventional voltage-feedback operational amplifier.

Power Supply Bypassing/Lead Dressing

It is important to bypass the power supplies of the EL2232 with 0.1 μF or 0.01 μF ceramic disc capacitors. A 4.7 μF tantalum capacitor is also recommended for each supply. These capacitors should be placed as close to the package as possible, and long lead lengths should be avoided. Failure to bypass the supplies in this manner will result in oscillation or signal distortion.

The −input of the EL2232 is fairly sensitive to stray capacitance, therefore it is important for the feedback and gain-setting resistors to be as close as possible to the −input. It is also a good idea to remove the PC board ground-plane near the −input.

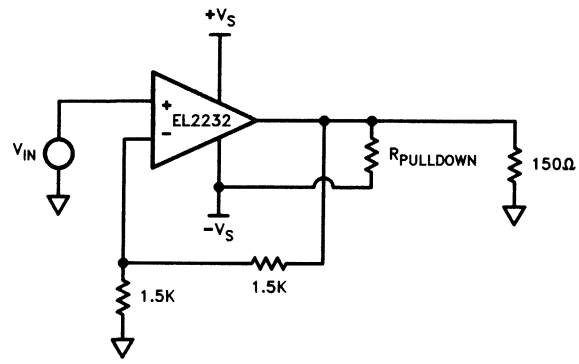
Current Limit

The EL2232 has an internal current limit of approximately 50 mA per amplifier, so if one of the outputs is shorted to ground (with V_S ±15V) the power dissipation could be as much as 1.1W. A heatsink is therefore required to survive an indefinite short at one of the outputs. If both of the outputs are shorted, power dissipation can approach 2W, resulting in the eventual destruction of the device, even with a heatsink.

Video Performance

To keep total supply current for the EL2232 at 9.5 mA, the output stage idle current had to be reduced substantially from the values used in the EL2020. As a consequence, a pulldown resistor is needed at the output of the EL2232 to achieve good video performance when driving the standard 150Ω double-terminated load. As seen in the Differential Gain and Phase Test Schematic, with ±15V rails a 1.5k pulldown resistor from the output to the −15V rail gives good video performance (0.1% dG 0.1° dP). With 5V rails, a 1k resistor gives similar results. These resistor values will vary with different load impedances, but in general the video performance improves as load impedance increases.

Adding a Pulldown Resistor to Improve Video Performance



2232-17

EL2232/EL2232C
60 MHz, Fast Settling, Dual Current Mode Feedback Amplifier

Applications Information — Contd.

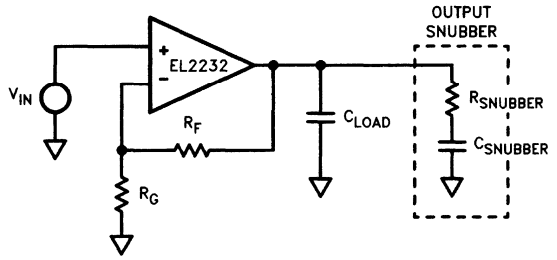
Capacitive Loading/Snubbing

The EL2232 has been designed to be stable in most situations with purely capacitive loads of up to about 50 pF. With 500Ω in parallel with the load capacitance, the EL2232 is usually stable with load capacitances of up to 100 pF, and often more (see the Cload vs Peaking curve). As expected with any high speed amplifier, the capacitive loading will increase the peaking of the closed loop frequency response (and therefore overshoot and ringing in the time domain) due to the decreased phase margin of the amplifier.

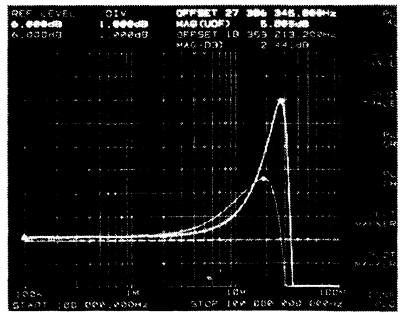
The use of an output snubber can be a valuable technique for improving stability when driving large capacitive loads. The output snubber is simply a series RC network placed from the output to ground, so that at high frequencies the amplifier is driving the load capacitance in parallel with a low value resistance (the snubber R). At low frequencies, the capacitance of the snubber is a high enough impedance so that the load looks the same as if the snubber were not tied to the output.

Selection of the R and C for the snubber is fairly simple. First, an R is selected to reduce peaking. As seen in the Frequency Response vs RL curves, the EL2232 has dramatically reduced peaking with a 150Ω load, so this is a good starting value. The resistor is then placed from the output to ground, and its value is varied until the desired response has been achieved. The capacitor is then chosen so that the corner frequency of the RC snubber is below the frequency of the peaking. Looking at the Cload vs Peaking Curve, the peaking is generally in the 20 MHz range for a gain of 2. Setting the corner frequency at 10 MHz, we get Csnubber = $1/(2\pi * Rsnubber * 10\ MHz)$ = 100 pF. This capacitance is then put in series with the snubber resistor and adjusted to achieve the desired response. As seen in the photograph, a 150Ω/100 pF snubber in conjunction with a 68 pF load reduces peaking from 5.8 dB down to a respectable 2.4 dB.

Adding An Output Snubber to Tame Capacitive Loads



2232-18

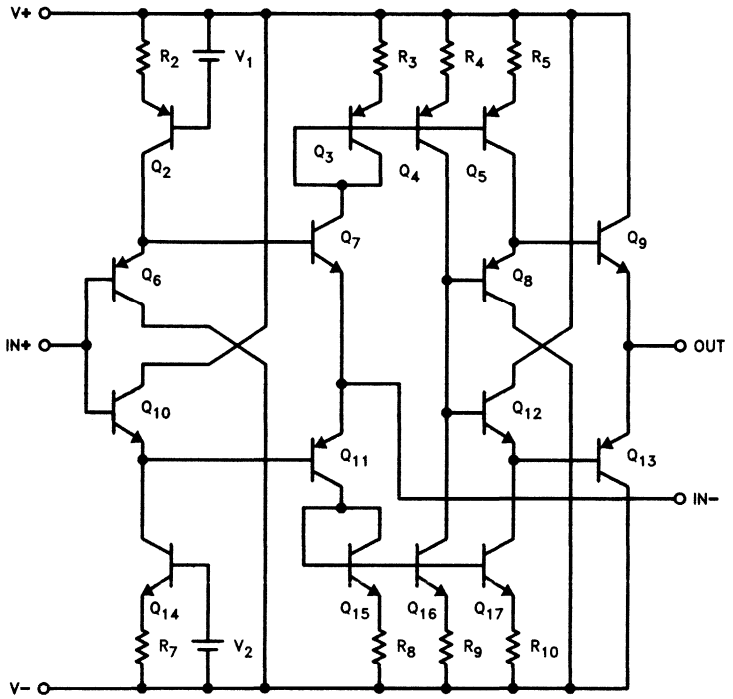


2232-19

EL2232 Frequency response with and without 150Ω/100 pF output snubber C_L = 68 pF

Applications Information — Contd.

Equivalent Circuit (One of Two Amplifiers)



2232-20

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2252/EL2252C
Dual 50 MHz Comparator/Pin Receiver

Features

- Fast response—7 ns
- Inputs tolerate large overdrives with no speed nor bias current penalties
- Propagation delay is relatively constant with variations of input Slew Rate, overdrive, temperature, and supply voltage
- Output provides proper CMOS or TTL logic levels
- Hysteresis is available on-chip
- Large voltage gain—8000 V/V
- Not oscillation-prone
- Can detect 4 ns glitches
- MIL-STD-883 Rev. C compliant

Applications

- Pin receiver for automatic test equipment
- Data communications line receiver
- Frequency counter input
- Pulse squarer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2252CJ	0°C to +75°C	14-Pin CerDIP	MDP0014
EL2252CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2252CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2252J	−55°C to +125°C	14-Pin CerDIP	MDP0014
EL2252J/883B	−55°C to +125°C	14-Pin CerDIP	MDP0014

General Description

The EL2252 dual comparator replaces the traditional input buffer + attenuator + ECL comparator + ECL to TTL translator circuit blocks used in digital equipment. The EL2252 provides a quick 7 ns propagation delay while complying with ±10V inputs. Input accuracy and propagation delay is maintained even with input signal Slew Rates as great as 4000 V/μs. The EL2252 can run on supplies as low as −5.2V and +9V and comply with ECL and CMOS inputs, or use supplies as great as ±18V for much greater input range.

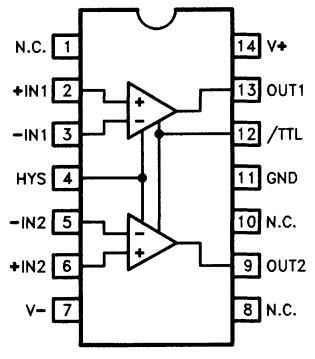
The EL2252 has a /TTL pin which, when grounded, restricts the output V_{OH} to a TTL swing to minimize propagation delay. When left open, the output V_{OH} increases to a valid CMOS level.

The comparators are well behaved and have little tendency to oscillate over a variety of input and output source and load impedances. They do not oscillate even when the inputs are held in the linear range of the device. To improve output stability in the presence of input noise, an internal 60 mV of hysteresis is available by connecting the HYS pin to V−.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2; *"Elantec's Military Processing, Monolithic Integrated Circuits"*.

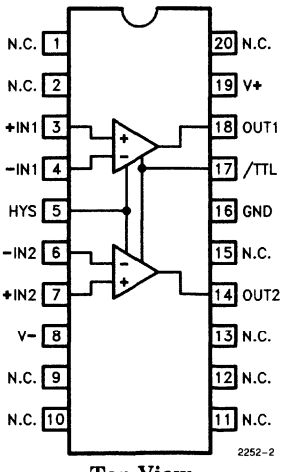
Connection Diagrams

14-Pin DIP



Top View

20-Pin SOL



Top View

EL2252/EL2252C
Dual 50 MHz Comparator/Pin Receiver

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	
Voltage at V+	18V	CerDIP	175°C
Voltage between −IN and +IN pins	36V	Plastic DIP, SOL	150°C
Output Current	12 mA	Storage Temperature Range	−65° to +150C
Current into +IN, −IN, HYS		Lead Temperature	
or /TTL	5 mA	DIP Package	
Internal Power Dissipation	See Curves	(Soldering, <10 seconds)	300°C
Operating Ambient Temperature Range		SOL Package	
EL2252	−55°C to +125°C	Vapor Phase (<60 seconds)	215°C
EL2252C	−25°C to +85°C	Infrared (<15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; HYS and /TTL grounded; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2252	EL2252C	
V_{OS}	Input Offset Voltage	25°C		1	6	I	I	mV
		Full			10	I	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		7		V	V	µV/C
I_B	Input Bias Current at Null	25°C		6	12	I	I	µA
		Full			17	I	III	µA
I_{OS}	Input Offset Current	25°C		0.2	1	I	I	µA
		Full			2	I	III	µA
R_{IN}, diff	Input Differential Resistance	25°C		30		V	V	kΩ
R_{IN}, comm	Input Common-Mode Resistance	25°C		10		V	V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	V	pF
V_{CM}+	Positive Common-Mode Input Range	Full	10	13		I	II	V
V_{CM}−	Negative Common-Mode Input Range	Full	−9	−12		I	II	V
A_{VOL}	Large Signal Voltage Gain V_O = 0.8V to 2.0V	25°C	4000	8000		I	I	V/V
		Full	3000			I	III	V/V

EL2252/EL2252C
Dual 50 MHz Comparator/Pin Receiver

DC Electrical Characteristics

$V_S = \pm 15V$; HYS and /TTL grounded; $T_A = 25°C$ unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2252	EL2252C	
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	70	95		I	II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	70	90		I	II	dB
V_{HYS}	Peak-to-Peak Input Hysteresis with HYS connected to V−	25°C		60		V	V	mV
V_{OH}	High Level Output, CMOS Mode	Full	4.0	4.6	5.1	I	II	V
	TTL Mode	Full	2.4	2.7	3.2	I	II	V
V_{OL}	Low Level Output, I1 = 0	Full	−0.2	0.2	0.4	I	II	V
	I1 = 5 mA	Full	−0.2	0.4	0.8	I	II	V
I_S+	Positive Supply Current	Full		16	19	I	II	mA
I_S-	Negative Supply Current	Full		17	20	I	II	mA

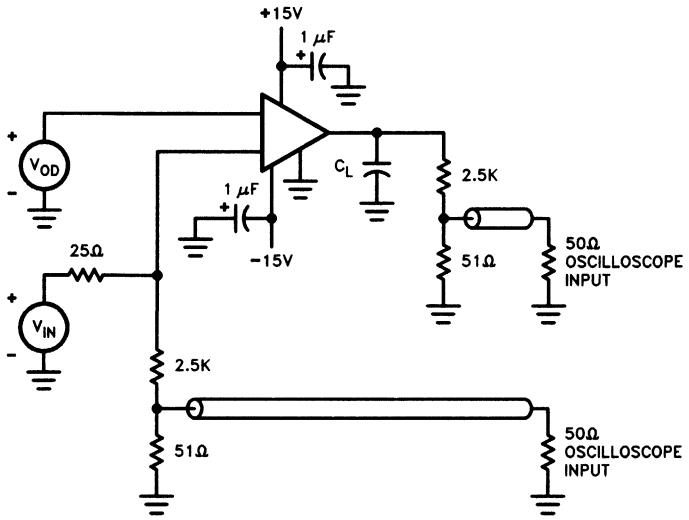
AC Electrical Characteristics

$V_S = \pm 15V$; $C_L = 10$ pF; $T_A = 25°C$; TTL output threshold is 1.4V, CMOS output threshold is 2.5V; unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level		Units
					EL2252	EL2252C	
$T_{PD}+$, $T_{PD}-$	Input to Output Propagation Delay, $0 < V_{IN} < 5V$, 500 mV Overdrive, 2000 V/μs Input Slew Rate						
	TTL Output Swing		6		V	V	ns
	CMOS Output Swing		8		V	V	ns
$T_{PD}+$, $T_{PD}-$	Input to Output Propagation Delay, $-2V < V_{IN} < -1V$, 200 mV Overdrive, 2 ns Input Rise Time						
	TTL Output Swing		7		V	V	ns
	CMOS Output Swing		9		V	V	ns
T_{PDSYM}	Propagation Delay Change between Positive and Negative Input Slopes		1.5		V	V	ns

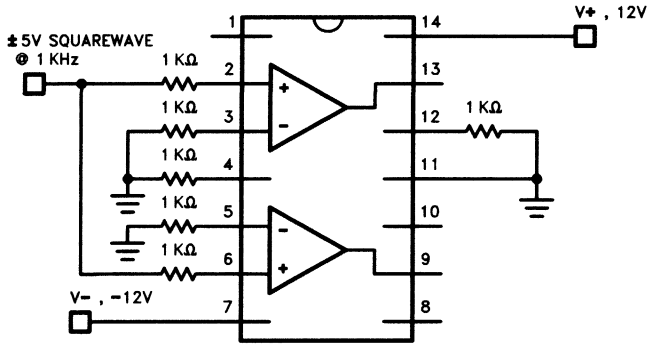
Note 1: Two tests are performed with $V_{CM} = 0V$ to $-9V$ and $V_{CM} = 0V$ to 10V.
Note 2: Two tests are performed with V+ = 15V, V− changed from −10V to −15V; V− = −15V, V+ changed from 10V to 15V.

AC Test Circuit



2252-3

Burn-In Circuit

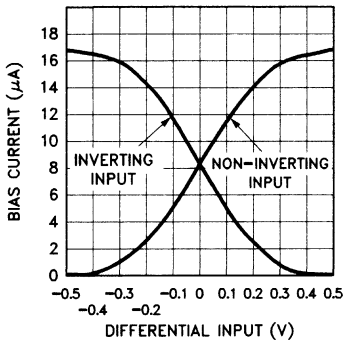


2252-4

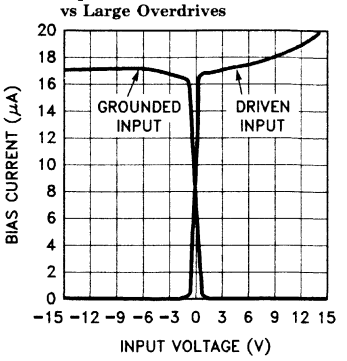
EL2252/EL2252C
Dual 50 MHz Comparator/Pin Receiver

Typical Performance Curves

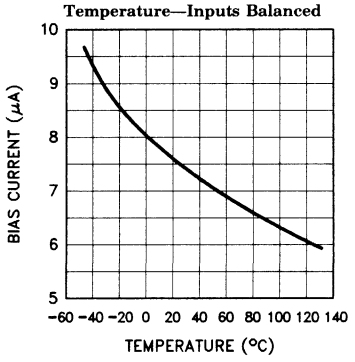
Input Bias Current vs Small Overdrives



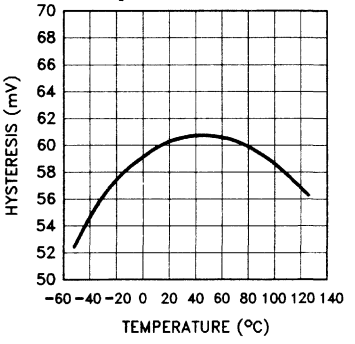
Input Bias Current vs Large Overdrives



Bias Current vs Temperature—Inputs Balanced

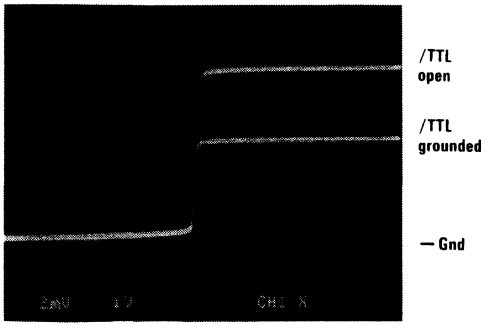


Input Hysteresis Voltage vs Temperature



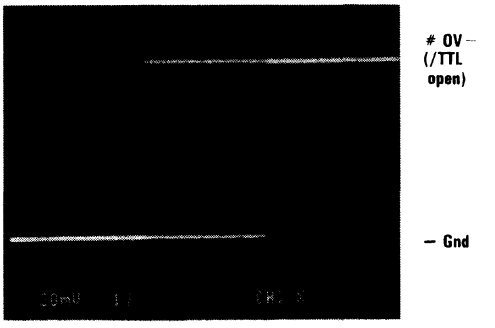
2252-5

Input/Output Transfer Function—HYS Open



2252-6

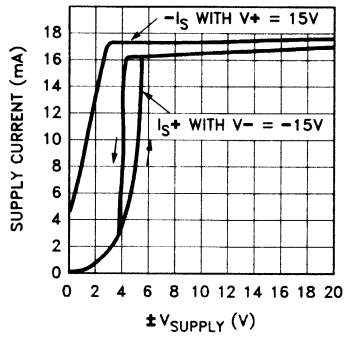
Input/Output Transfer Function—HYS Connected to V



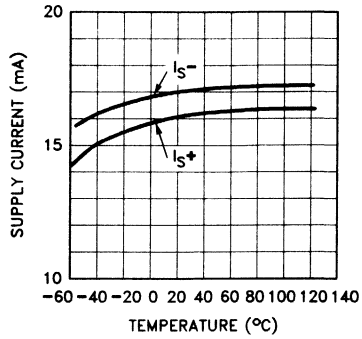
2252-7

Typical Performance Curves — Contd.

Supply Current vs Supply Voltage

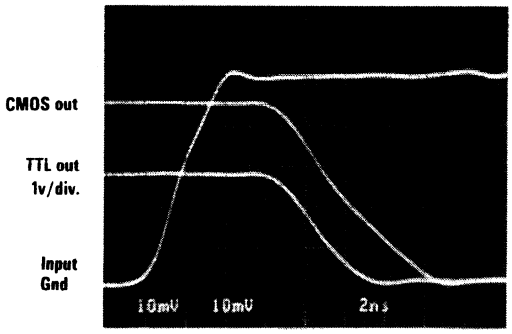


Supply Current vs Temperature (V_S = ±15V)



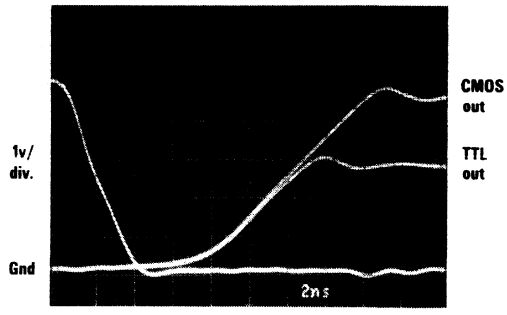
2252-8

Output Delay—0.5V Overdrive



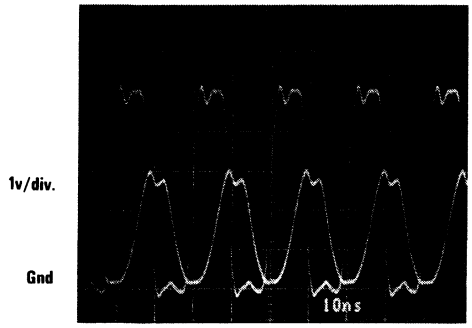
2252-9

Output Delay—0.5V Overdrive



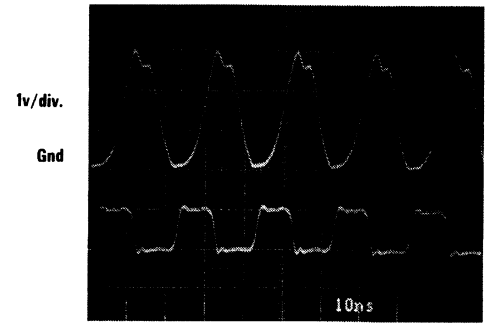
2252-10

Output with 50 MHz CMOS Input



2252-11

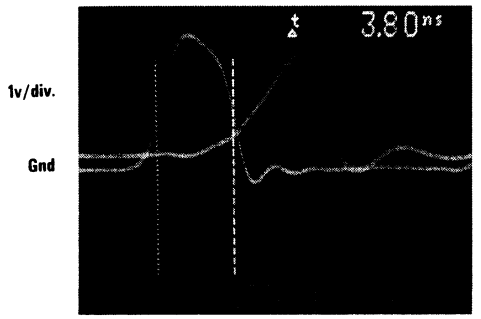
Output with 50 MHz ECL Input



2252-12

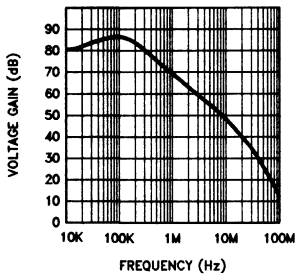
Typical Performance Curves — Contd.

4 ns TTL Glitch Detection

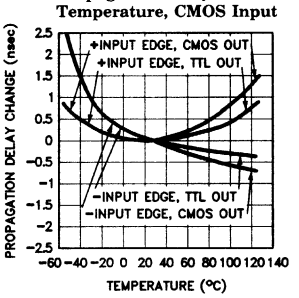


2252-13

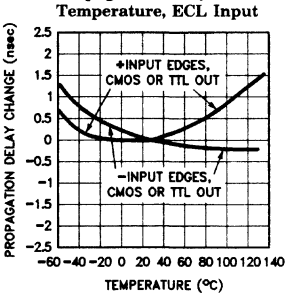
Gain vs Frequency



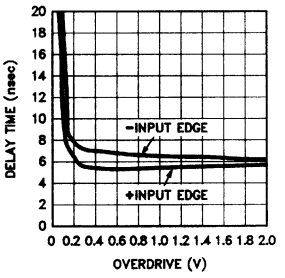
Propagation Delay vs Temperature, CMOS Input



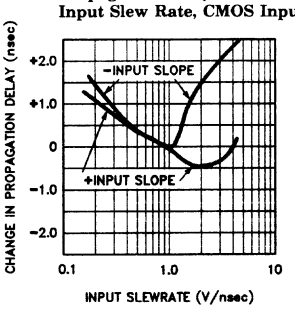
Propagation Delay vs Temperature, ECL Input



Propagation Delay vs Overdrive, CMOS Input



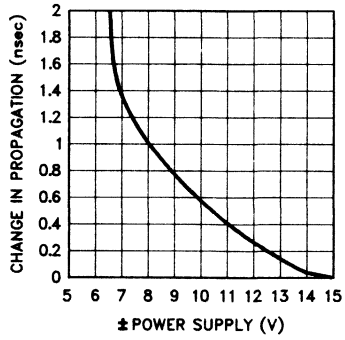
Propagation Delay vs Input Slew Rate, CMOS Input



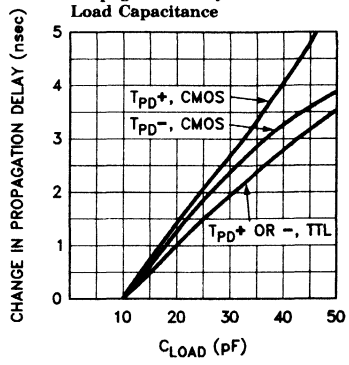
2252-14

Typical Performance Curves — Contd.

Propagation Delay vs Power Supply Voltage

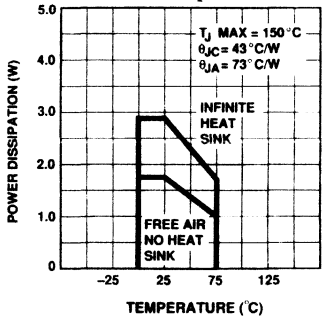


Propagation Delay vs Load Capacitance



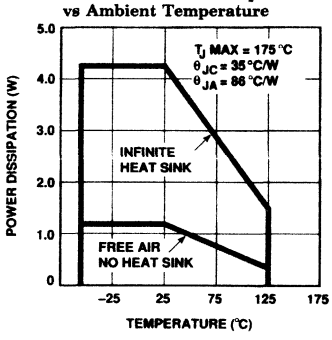
2252-15

14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



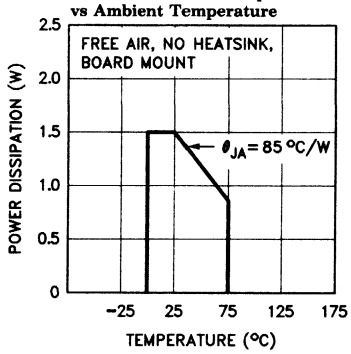
2252-16

14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



2252-17

20-Lead SOL Maximum Power Dissipation vs Ambient Temperature

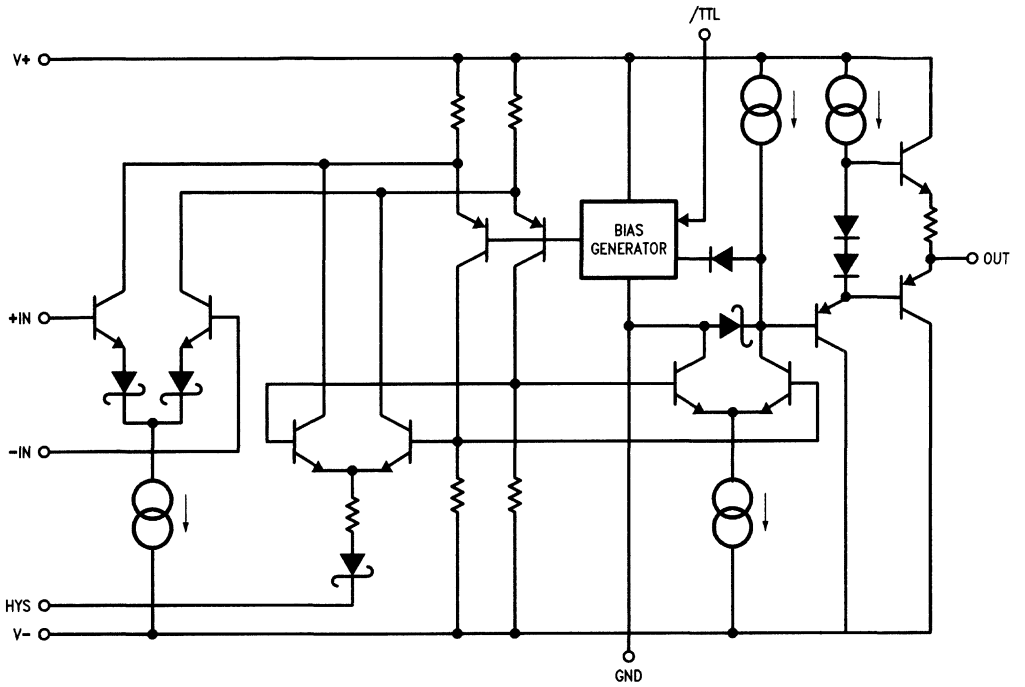


2252-18

EL2252/EL2252C
Dual 50 MHz Comparator/Pin Receiver

Simplified Schematic

One Comparator



2252-19

Applications Information

The EL2252 is very easy to use and is relatively oscillation-free, but a few items must be attended. The first is that both supplies should be bypassed closely. 1 μF tantalums are very good and no additional smaller capacitors are necessary. The EL2252 requires V− to be at least 5V to preserve AC performance. V+ must be at least 6V for a TTL output swing, 8V for CMOS outputs.

The input voltage range will be referred to the more positive of the two inputs. That is, bringing an input as negative as V− will not cause problems; it's the other input's level that must be considered. The typical input range is +13/−12V when the supplies are ±15V. This range diminishes over temperature and varies with processing; it is wise to set power supplies such that V+ is 5V more positive than the most positive input signal and V− more negative than 6V below the most negative input. ±12V supplies will easily encompass all CMOS and ECL logic inputs. If the input exceeds the device's common-mode input capability, the EL2252 propagation delay and input bias current will increase. Fault currents will occur with inputs a diode below V− or above V+. No damage nor V_{OS} shift will occur even when fault currents within the absolute maximum ratings.

Applications Information — Contd.

One of the few ways in which oscillations can be induced is by connecting a high-Q reactive source impedance to the EL2252 inputs. Such sources are long wires and unterminated coaxial lines. The source impedance should be de-Q'ed. One method is to connect a series resistor to the EL2252 input of around 100Ω value. More resistance will calm the system more effectively, but at the expense of comparator response time. Another method is to install a "snubber" network from comparator input to ground. A snubber is a resistor in series with a small capacitor, around 100Ω and 33 pF. Each physical and electrical environment will require different treatments, although many need none.

The EL2252 is specifically designed to be tolerent of large inputs. It will exhibit very much increased delay times for input overdrives below 100 mV. If very small overdrives must be sensed, the EL2018 or EL2019 comparators would be good choices, although they lose accuracies with signal input Slew Rates above 400 V/μs. The EL2252 keeps its timing accuracy with input Slew Rates between 100 V/μs and 4000 V/μs of input Slew Rate.

The output stage drives tens of pF load capacitances without increased overshoot, but propagation delay increases about 1 ns per 10 pF. The output circuit is not a traditional TTL stage, and using an external pullup resistor will not change the V_{OH}. In general setting the output swing to TTL (by grounding the /TTL pin) will optimize overall propagation delay and ±swing symmetry.

Arrays

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec Transistor Arrays

ELANTEC Part Number	Description	Test Temp	V_{be} Match		H_{fe} Match		Min H_{fe}		BV_{ceo} BV_{cbo} Over Temp (Min)	Packages
			25°	Over Temp	25°C	Over Temp	25°C	Over Temp		
EP2015	Monolithic, D.I. Matched Quad PNP Transistor Array	−55°C to +125°C	5 mV	10 mV	10%	20%	75	30	40V	14-Pin CerDIP
EP2015C		0°C to +75°C	5 mV	N/A	10%	N/A	75	N/A	40V	14-Pin Plastic DIP 14-Pin CerDIP
EP2015A	Monolithic, D.I. Precision Matched Quad PNP Transistor Array	−55°C to +125°C	1 mV	2 mV	5%	10%	150	60	40V	14-Pin CerDIP
EP2015AC		0°C to +75°C	1 mV	2 mV	10%	20%	150	60	40V	14-Pin Plastic DIP 14-Pin CerDIP
EN2016	Monolithic, D.I. Matched Quad NPN Transistor Array	−55°C to +125°C	5 mV	10 mV	10%	20%	75	50	40V	14-Pin CerDIP
EN2016C		0°C to +75°C	5 mV	N/A	10%	N/A	75	N/A	40V	14-Pin Plastic DIP 14-Pin CerDIP
EN2016A	Monolithic, D.I. Precision Matched Quad NPN Transistor Array	−55°C to +125°C	1 mV	2 mV	5%	10%	150	100	40V	14-Pin CerDIP
EN2016AC		0°C to +75°C	1 mV	2 mV	10%	20%	150	100	40V	14-Pin Plastic DIP 14-Pin CerDIP

élantec HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EP2015/EP2015A
Fast Quad PNP Array

Features

- Four independent fast PNP's
- 350 MHz f_t
- Tight V_{BE} matching—1 mV
- Tight H_{fe} matching—5%
- One chip construction with dielectric isolation
- Excellent thermal tracking
- High H_{fe}—150 minimum
- 40V minimum BV_{ceo}
- Each transistor similar to 2N3906
- Pin compatible with TPQ3906 and MPQ3906

Applications

- Current sources
- Current mirrors
- Log amplifiers
- Multipliers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EP2015CN	0°C to +75°C	P-DIP	MDP0031
EP2015ACN	0°C to +75°C	P-DIP	MDP0031
EP2015CJ	0°C to +75°C	CerDIP	MDP0014
EP2015ACJ	0°C to +75°C	CerDIP	MDP0014
EP2015J	−55°C to +125°C	CerDIP	MDP0014
EP2015AJ	−55°C to +125°C	CerDIP	MDP0014
EP2015J/883B	−55°C to +125°C	CerDIP	MDP0014
EP2015AJ/883B	−55°C to +125°C	CerDIP	MDP0014
EP2015AL	−55°C to +125°C	LCC	MDP0007
EP2015L	−55°C to +125°C	LCC	MDP0007
EP2015L/883B	−55°C to +125°C	LCC	MDP0007
EP2015AL/883B	−55°C to +125°C	LCC	MDP0007
EP2015CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EP2015 family are quad monolithic vertical PNP transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz f_t provides A.C. performance similar to 2N3906 class devices. Manufactured on Elantec's Complementary Bipolar process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete D.C. isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

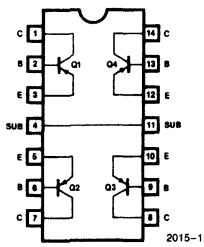
The low cost EP2015C is specified at 25°C. The EP2015AC is more tightly specified and guaranteed over the commercial temperature range of 0°C to +75°C. The EP2015 and the more stringently specified EP2015A are tested over the full military temperature range of −55°C to +125°C. The EP2015C and EP2015AC are available in either 14-pin plastic dual-in-line or ceramic dual-in-line packages. The EP2015 is also available in chip form for hybrid applications. Its large bonding pads provide for easy automated manufacturing.

For information on a complementary NPN transistor array, see Elantec's EN2016 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

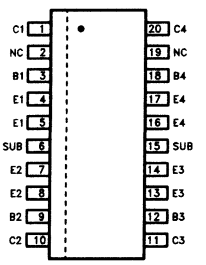
DIP Package



2015-1

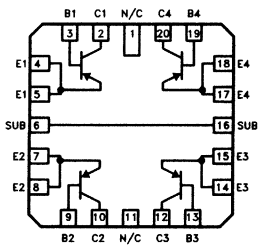
Top View

20-Lead SOL



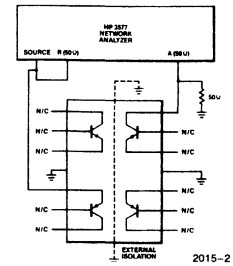
2015-13

LCC



2015-3

Isolation Characteristics Test Circuit



2015-2

EP2015/EP2015A
Fast Quad PNP Array

Absolute Maximum Ratings

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
	Total Package	1.25W (T_A = 25°C)
T_A	Operating Temperature Range	
	EP2015A/EP2015	−55°C to +125°C
	EP2015C/EP2015AC	−0°C to +75°C
T_J	Maximum Junction Temperature	
	CerDIP, Ceramic LCC	175°C
	Plastic DIP and SOL	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature	
	SOL Package	
	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
	(Soldering, <10 seconds)	300°C
V_{CB}	Max	40V
V_{EB}	Max	5V
V_{CE}	Max	40V
I_C	Max	50 mA
I_B	Max	10 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

Parameter	Description	Test Conditions	EP2015				EP2015C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA, T_A = 25°C			5	I			5	I	mV
		$T_{MIN} < T_A < T_{MAX}$			10	I					mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C			10	I			10	I	%
		$T_{MIN} < T_A < T_{MAX}$			20	I					%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA, T_A = 25°C			10	I			10	I	%
		$T_{MIN} < T_A < T_{MAX}$			20	I					%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA, T_A = 25°C			10	I			10	I	%
		$T_{MIN} < T_A < T_{MAX}$			20	I					%
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C	75			I	75			I	
		$T_{MIN} < T_A < T_{MAX}$	30			I					
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C	75			I	75			I	
		$T_{MIN} < T_A < T_{MAX}$	30			I					

Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EP2015				EP2015C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	75			I	75			I	
		$T_{MIN} < T_A < T_{MAX}$	30			I					
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$			1.10	I					V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$			0.30	I					V
BV_{cco}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I					V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I					V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	5			I	V
		$T_{MIN} < T_A < T_{MAX}$	5			I					V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I					nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I					nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA, < I_C < 2 mA T_A = 25°C		1		V		1		V	Ω

Parameter	Description	Test Conditions	EP2015A				EP2015AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA T_A = 25°C			1	I			1	I	mV
		$T_{MIN} < T_A < T_{MAX}$			2	I			2	III	mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C			5	I			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	I			10	III	%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA T_A = 25°C			5	I			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	I			10	III	%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C			5	I			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	I			10	III	%

EP2015/EP2015A
Fast Quad PNP Array

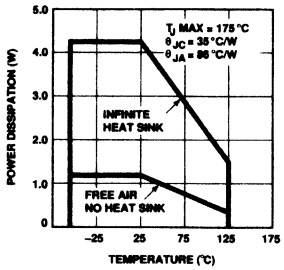
Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EP2015A				EP2015AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C	150			I	150			I	
		$T_{MIN} < T_A < T_{MAX}$	60			I	60			III	
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA T_A = 25°C	150			I	150			I	
		$T_{MIN} < T_A < T_{MAX}$	60			I	60			III	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	100			I	100			I	
		$T_{MIN} < T_A < T_{MAX}$	40			I	40			III	
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$			1.10	I			1.10	III	V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$			0.30	I			0.30	III	V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I	40			III	V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I	40			III	V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	5			I	V
		$T_{MIN} < T_A < T_{MAX}$	5			I	5			III	V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I			50	III	nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I			50	III	nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA < I_C < 2 mA T_A = 25°C		1		V		1		V	Ω

Note 1: ΔV_{BE} and ΔH_{fe} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{fe} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.
Note 4: Estimated from log conformity.

Typical Performance Curves

14-Lead CerDIP
Maximum Power Dissipation
vs Ambient Temperature



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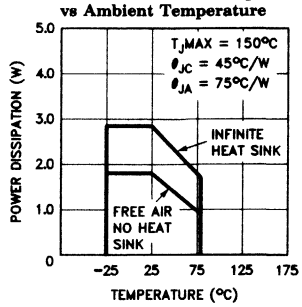
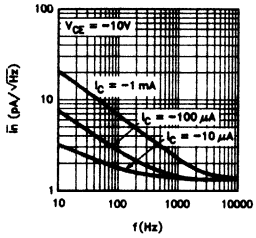
14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

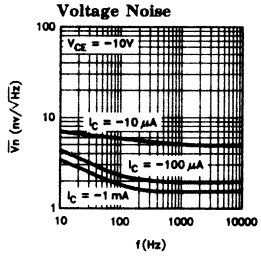


2015-12

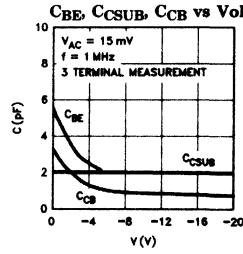
Current Noise



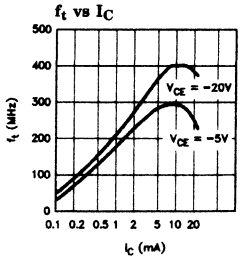
Voltage Noise



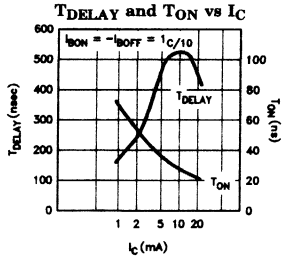
C_{BE}, C_{CSUB}, C_{CB} vs Voltage



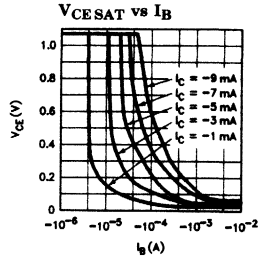
f_t vs I_C



T_{DELAY} and T_{ON} vs I_C

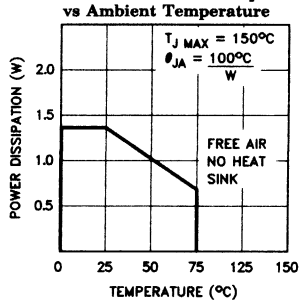


V_{CE}SAT vs I_B



2015-4

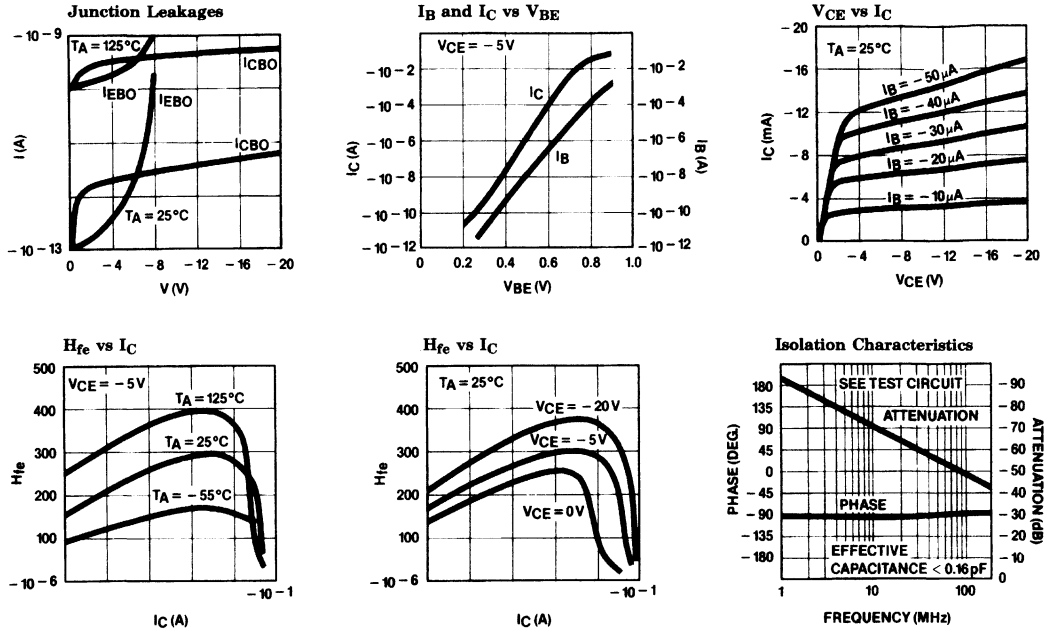
20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2015-14

EP2015/EP2015A
Fast Quad PNP Array

Typical Performance Curves — Contd.



2015-5

EP2015 PSPICE® Model

IS = 8E−15 BF = 300 VA = 47 IK = 0.03
XTB = 1.3 BR = 4.5 TF = 0.3N TR = 280N
RB = 230 RC = 170 ISE = 1E−15 NE = 1.24
CCS = 2P MS = 0 CJC = 3.7P PC = 0.5 MC = 0.45
CJE = 5.4P PE = 0.6 ME = 0.33 PTF = 15

Note that for the above model the maximum "soft" saturation collector RC is used. For "hard" saturation modeling set RC ≈ 9.

PSPICE® is a registered trademark of MicroSim Corporation.

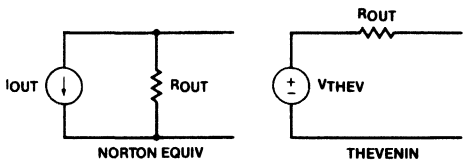
Matched NPN transistors have allowed system designers to make NPN current sinks. Now for the first time Elantec's fast matched PNP transistors are available. These make excellent, fast, matched current sources. The advantages of using current sources as active loads, instead of pullup resistors include:

- Faster, linear pull up (Not exponential)
- High output resistance (This increases voltage gain in many applications)

Current Sources and Current Mirrors

Current sinks and current mirrors have long been a tool available to the designer of monolithic ICs.

The Norton and Thevenin equivalent circuits of a current source are:



2015-6

And $V_{THEV} = I_{OUT} \times R_{OUT}$

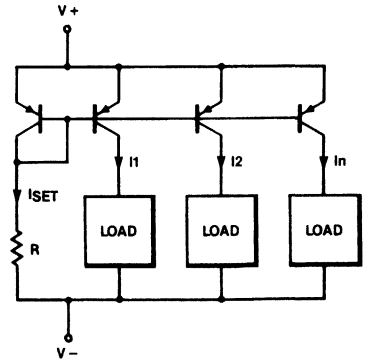
Four examples of current mirrors are shown, along with some of the advantages and limitations of each topology. For a more thorough discussion see "Analysis and Design of Analog Integrated Circuits" by Grey & Meyer (Wiley 1984), pages 233–247.

All current sources are only as good as the transistors that make them. If the transistors' V_{BE} match is 5 mV the output current would have a 20% error.

All current sources shown can be improved by putting a resistor in series with the topmost emitters. A 250 mV drop across these resistors reduces a 5 mV V_{BE} mismatch to a 2% current error. This has the added benefit of increasing output resistance. Elantec can guarantee a 1 mV V_{BE} match so resistors may not be necessary.

Basic Current Source

The Basic Current Mirror is simple and works well at low currents. Its limitations are low output resistance and it is not as fast as the Wilson.



2015-7

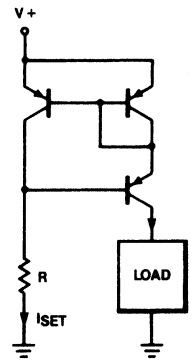
$$I_{SET} \approx \frac{((V+) - (V-)) - V_{BE}}{R}$$

$$I1 = I2 = In = \frac{\beta I1}{\beta + n + 1}$$

$$R_{OUT} = \frac{V_A}{I_{OUT}} = \frac{\text{EARLY VOLTAGE}}{I_{OUT}} = r_o$$

PNP Wilson Current Mirror

The Wilson is the best Current Mirror for high frequency applications, and it has plenty of output resistance.



$$I_{OUT} \approx I_{REF}\left(1 - \frac{2}{\beta^2 + 2\beta + 2}\right)$$

$$R_{OUT} \approx \frac{\beta r_o}{2}$$

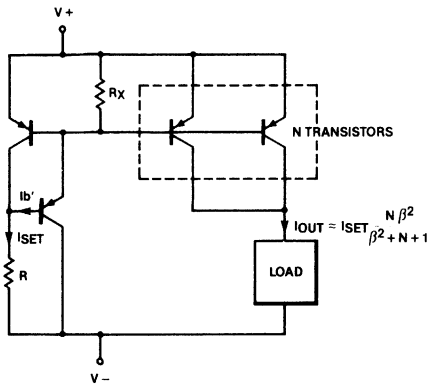
$$V_{THEV} \approx \frac{\beta V_A}{2}$$

2015-9

EP2015/EP2015A
Fast Quad PNP Array

Precision Current Source

The Precision Current Source has excellent current match since the error reduction is proportional to β^2. It is slow to turn off since it has no base turn off current. The turn off speed can be increased by using R_X, at the expense of reduced accuracy.



2015-8

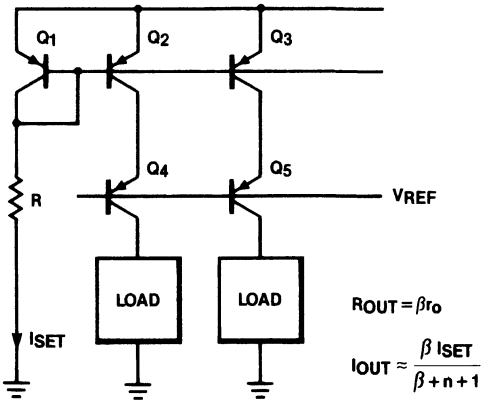
$$I_{SET} \approx \frac{((V+) - (V-)) - 2(V_{BE})}{R}$$

$$I_{OUT} \approx I_{SET} \frac{N\beta^2}{\beta^2 + N + 1}$$

$$R_{OUT} = \frac{V_A}{I_{OUT}}$$

Cascode Current Source

The Cascode Current Source is a basic current mirror with a common base transistor in the collector. This makes V_{CE} relatively constant for the mirror transistors and greatly increases the output resistance. This has good high frequency characteristics. Note that Q4 and Q5 can be in a package separate from Q1, Q2 and Q3.



2015-10

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EN2016/EN2016A
Fast Quad NPN Array

Features

- Four independent fast NPN's
- 350 MHz f_t
- Tight V_{be} matching—1 mV
- Tight H_{fe} matching—5%
- One chip construction with dielectric isolation
- Excellent thermal tracking
- High H_{fe}—150 minimum
- 40V minimum BV_{ceo}
- Each transistor similar to 2N3904
- Pin compatible with TPQ3904 and MPQ3904

Applications

- Current sources
- Current mirrors
- Log amplifiers
- Multipliers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EN2016CN	0°C to +75°C	P-DIP	MDP0031
EN2016ACN	0°C to +75°C	P-DIP	MDP0031
EN2016CJ	0°C to +75°C	CerDIP	MDP0014
EN2016ACJ	0°C to +75°C	CerDIP	MDP0014
EN2016CM	0°C to +75°C	20-Lead SOL	MDP0027
EN2016J	−55°C to +125°C	CerDIP	MDP0014
EN2016AJ	−55°C to +125°C	CerDIP	MDP0014
EN2016J/883B	−55°C to +125°C	CerDIP	MDP0014
EN2016AJ/883B	−55°C to +125°C	CerDIP	MDP0014

General Description

The EN2016 family are quad monolithic vertical NPN transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz f_t provides AC performance similar to 2N3904 class devices. Manufactured on Elantec's Complementary Bipolar process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete DC isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

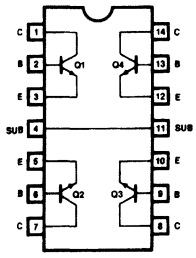
The low cost EN2016C is specified at 25°C. The EN2016AC is more tightly specified and guaranteed over the commercial temperature range of 0°C to +75°C. The EN2016 and the more stringently specified EN2016A are tested over the full military temperature range of −55°C to +125°C. The EN2016C and EN2016AC are available in either 14-pin plastic dual-in-line or ceramic dual-in-line packages. The EN2016 is also available in chip form for hybrid applications. Its large bonding pads provide for easy automated manufacturing.

For information on a complementary PNP transistor array, see Elantec's EP2015 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

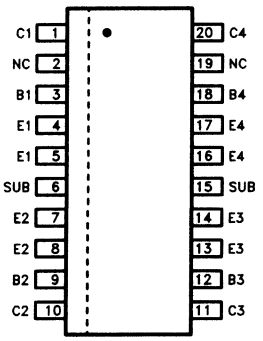
14-Lead DIP



2016-1

Top View

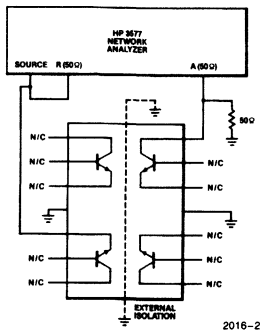
20-Lead SOL



2016-3

Top View

Isolation Characteristics Test Circuit



2016-2

EN2016/EN2016A
Fast Quad NPN Array

Absolute Maximum Ratings

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
	Total Package	1.25W (T_A = 25°C)
T_A	Operating Temperature Range	
	EN2016A/EN2016	−55°C to +125°C
	EN2016C/EN2016AC	0°C to +75°C
T_{ST}	Storage Temperature	−65°C to +150°C
T_J	Maximum Junction Temperature	150°C
	CerDIP	175°C
	Plastic DIP and SOL	150°C

Lead Temperature	
SOL Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
(Soldering, < 10 seconds)	300°C
V_{cb} MAX	40V
V_{eb} MAX	5V
V_{ce} MAX	40V
I_c MAX	50 mA
I_b MAX	100 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

Parameter	Description	Test Conditions	EN2016				EN2016C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA, T_A = 25°C			5	I			5	I	mV
		$T_{MIN} < T_A < T_{MAX}$			10	I					mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C			10	I			10	I	%
		$T_{MIN} < T_A < T_{MAX}$			20	I					%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C			10	I			10	I	%
		$T_{MIN} < T_A < T_{MAX}$			20	I					%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA, T_A = 25°C			10	I			10	I	%
		$T_{MIN} < T_A < T_{MAX}$			20	I					%
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C	75			I	75			I	
		$T_{MIN} < T_A < T_{MAX}$	50			I					
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C	75			I	75			I	
		$T_{MIN} < T_A < T_{MAX}$	50			I					

Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EN2016				EN2016C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	75			I	75			I	
		$T_{MIN} < T_A < T_{MAX}$	50			I					
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$			1.10	I					V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$			0.30	I					V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I					V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I					V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	5			I	V
		$T_{MIN} < T_A < T_{MAX}$	5			I					V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I					nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I					nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA < I_C < 2 mA T_A = 25°C		1		V		1		V	Ω

EN2016/EN2016A
Fast Quad NPN Array

Electrical Characteristics — Contd.

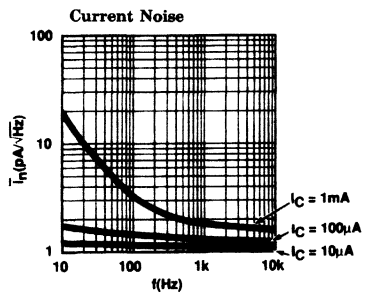
Parameter	Description	Test Conditions	EN2016A				EN2016AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA T_A = 25°C			1	I			1	I	mV
		$T_{MIN} < T_A < T_{MAX}$			2	I			2	III	mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C			5	I			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	I			10	III	%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1.0 mA T_A = 25°C			5	I			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	I			10	III	%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C			5	I			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	I			10	III	%
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C	150			I	150			I	
		$T_{MIN} < T_A < T_{MAX}$	100			I	100			III	
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA T_A = 25°C	150			I	150			I	
		$T_{MIN} < T_A < T_{MAX}$	100			I	100			III	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	100			I	100			I	
		$T_{MIN} < T_A < T_{MAX}$	75			I	75			III	
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$			1.10	I			1.10	III	V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$			0.30	I			0.30	III	V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I	40			III	V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I	40			III	V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_E = 0 mA T_A = 25°C	5			I	5			I	V
		$T_{MIN} < T_A < T_{MAX}$	5			I	5			III	V

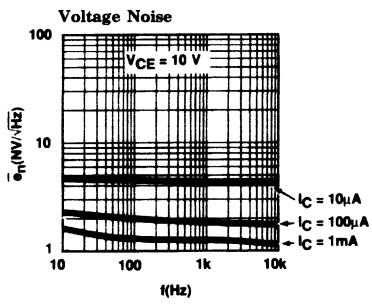
Electrical Characteristics — Contd.

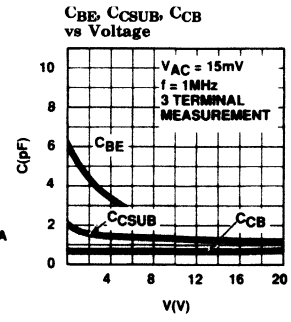
Parameter	Description	Test Conditions	EN2016A				EN2016AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I			50	III	nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	I			50	III	nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA < I_C < 2 mA T_A = 25°C		1		V		1		V	Ω

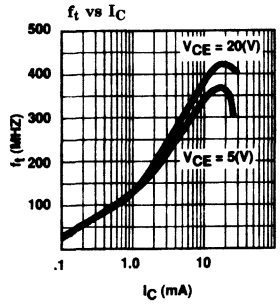
Note 1: ΔV_{BE} and ΔH_{FE} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{FE} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.
Note 4: Estimated from log conformity.

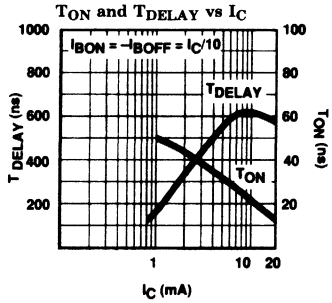
Typical Performance Curves

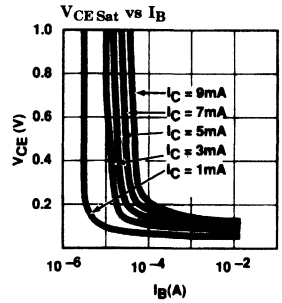










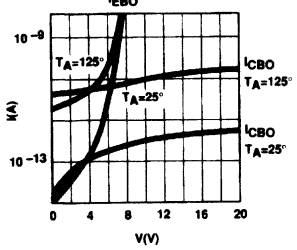


2016-4

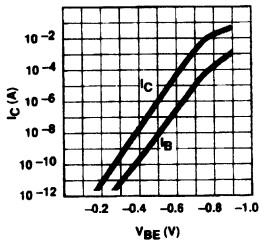
EN2016/EN2016A
Fast Quad NPN Array

Typical Performance Curves — Contd.

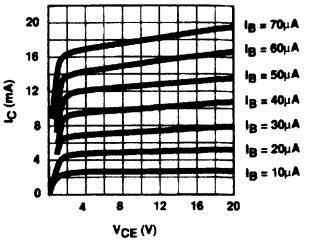
Junction Leakages



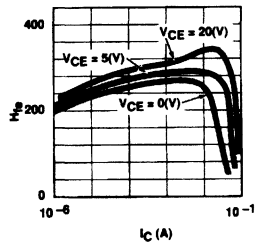
I_B and I_C vs V_{BE}



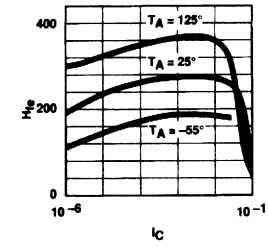
V_{CE} vs I_C



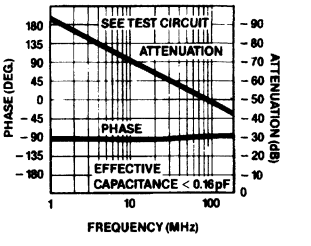
H_{fe} vs I_C



H_{fe} vs I_C

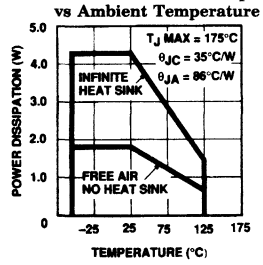


Isolation Characteristics



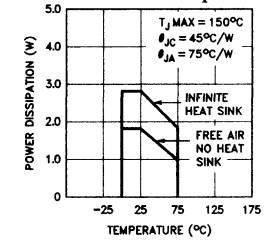
2016-5

14-Lead CerDIP
Maximum Power Dissipation
vs Ambient Temperature



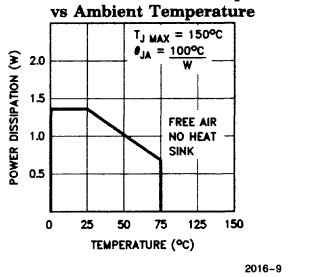
2016-6

14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



2016-7

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



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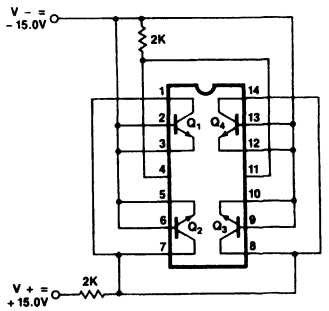
Note that for the above model the maximum "soft" saturation collector RC is used. For hard saturation set RC = 8.
PSPICE® is a registered trademark of Microsim Corporation.

EN2016 PSPICE® Model

NPN IS = 4E – 15 BF = 250 VA = 80 IK = 0.12
XTB = 1.1 BR = 10 TF = 0.35N TR = 80N
RB = 200 RC = 150 ISE = 3E – 14 NE = 2
CCS = 0.7P MS = 0 CJC = 2.4P XCJC = 0.3
PC = 0.32 MC = 0.19 CJE = 6P PE = 0.63
ME = 0.30 PTF = 15

Burn-In Circuit



2016-8

Quality and Military Programs

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Forward

This document summarizes Elantec's philosophy and policies towards Quality Assurance and Reliability for both MIL-STD-883 and commercial products. It is intended as an overview only, to give the reader a quick visualization of Elantec's capabilities and standard procedures.

Customers wishing more detail should refer to either "QRA-2, Elantec's 883B Program for Monolithic Integrated Circuits" or "QRA-3, Elantec's 883B program for Hybrid Integrated Circuits", or contact us at the factory. Also available are "QRA-4 Hybrid S-Flow" and "QRA-5 Monolithic Class S Flow". Our facilities and process documentation are available for customer inspection at any time. We welcome you to visit us at your earliest convenience, as we believe our factory to be "our best salesman".

Philosophy

Elantec was founded on the principle of supplying Analog Integrated Circuits of advanced performance with quality levels beyond that normally available from the semiconductor industry. Our product range has been intentionally limited to service commercial, industrial and Military/Areospace applications only. It is our firm belief that by placing quality and reliability over all other objectives, we will achieve our goal of providing our customers maximum cost-effectiveness and long term satisfaction.

Using both monolithic and hybrid technologies, Elantec provides leading edge Analog Integrated Circuit devices whose performance routinely exceeds that of most commercial manufacturers.

It is our policy to insure that each and every device is:

1) Designed to provide maximum long-term reliability.
2) Manufactured in strict compliance with thoroughly documented procedures in a tightly controlled environment.
3) Tested to insure that every device meets each parameter specified on the data sheet or customer specification.
4) Covered by a rigorous regularly scheduled Quality and Reliability Audit Program.

Military/Aerospace Program Summary

Elantec:

- Provides product screened and quality performance tested in accordance with MIL-STD-883.
- Is an approved supplier to DESC/SMD drawing numbers:

  78013—similar to ELH0002H/883B
  80013—similar to ELH0032G/883B
  80014—similar to ELH0033G/883B
  85087—similar to ELH0041G/883B
  85088—similar to ELH00021K/883B
  85089—similar to ELH0101K/883B or ELH0101AK/883B
  * 5962-89620—similar to EL2020
  * 5962-89623—similar to EL2003
  5962-87783—similar to EHA2400/883B
  * 5962-87787—similar to EHA2539/883B
  * 5962-89648—similar to EHA2540/883B
  * 5962-87784—similar to EHA5190/883B
  * Note: Pending DESC release

This list will be updated as new devices are added or as completion of the qualification cycle at DESC is reached.

- Maintains an on-going product qualification and reliability monitor program. Current quality conformance data is always available to support military product.
- Manufactures MIL-STD-883 Hybrid products 100% in the United States in our facility in Milpitas, California.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Facilities have been surveyed and approved by major military/aerospace customers—names available upon request.
- Maintains complete traceabilty and manufacturing history on each production lot.
- Has been audited and certified by DESC to MIL-STD-1772.

Summary of Elantec's Reliability and Quality Assurance Policy and Procedures QRA-1

- Maintains shelf stock of MIL-STD-883 product for rapid delivery at competitive prices.
- Welcomes customer Source Control Drawings, special selections and custom reliability processing.

Commercial Program Summary

Elantec:

- Provides the most thoroughly tested product available.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Provides 100% Temperature Cycling, Centrifuge, Fine and Gross Leak checks on all hermetic package commercial devices (see Table II).
- Uses superior manufacturing processes for hybrid devices to eliminate failure modes inherent in conventional assembly techniques.
- Maintains traceability on production lots.
- Manufactures thick film substrates and performs final electrical testing of commercial devices 100% in our Milpitas, California facility.

Facility

All military hybrid product manufactured by Elantec is completely built in the U.S.A. at our factory in Milpitas, California. Military monolithic product may be assembled onshore or offshore, however, all testing is performed in Milpitas. Commercial product thick film processing and all electrical testing is done in Milpitas. Commercial assembly may be done either in Milpitas or offshore.

The Milpitas factory has been certified by many customers to meet the requirements of MIL-I-45208. Defense Electronics Supply Center (DESC) has performed an audit and certified Elantec to the Hybrid Line Certification Specification, MIL-STD-1772.

The factory has 21,000 square feet of space. 5000 square feet is a Class 1000 clean room (Fed. Std 209) where assembly and electrical test are performed. All assembly operations are done under Class 100 laminar flow hoods. Temperature and humidity are monitored and controlled in accordance with MIL-STD-883. Gases are filtered at point of use. De-ionized water is filtered and bacteria controlled, and resistivity is continuously monitored. All semiconductor work-in-process is stored in nitrogen-purged dessicators.

A comprehensive ESD program is in effect. All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements. Shelving at all inventory locations is grounded. Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement. Conductive heel straps are worn by all operators. All product, commercial and military, is marked with an equalateral triangle to indicate static sensitivity in accordance with MIL-M-38510. Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes or conductive bags.

Elantec maintains complete *in-house* capability to 100% process devices to the requirements of MIL-STD-883 Class B. Additional in-house capability includes Particle Impact Noise Detection (PIND). All testing for initial product qualification and periodic quality conformance is performed in-house except for moisture resistance, internal water vapor, mechanical shock and vibration which are performed at DESC certified laboratories.

All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by Appendix A, paragraph 30.1.1.9 of MIL-M-38510.

Elantec maintains a complete Program Plan in accordance with MIL-M-38510. The plan is available for review by customers at Elantec. Included within the Program Plan is a complete equipment and facilities list.

Quality System

All quality assurance functions at Elantec report to the President and are totally independent of the manufacturing organization. These functions include Incoming Quality Control, In-Process Quality Control, Product Qualification, Quality Conformance, Document Control, Customer Specification Review, Internal Quality Audit, and Failure Analysis.

Elantec's operation is controlled by a thorough documentation system. Peripheral support systems such as document control, calibration, customer specification review, the ESD program, and archives are fully documented as to procedure and responsibility. All manufacturing operations have specifications describing the equipment operation and procedures. Product manufacturing flow charts define precise operational sequences to insure each lot is built in conformance to Elantec and Military requirements. All raw materials are purchased to Elantec Procurement Documents. Military package materials and finishes are in accordance with MIL-M-38510.

Raw materials are inspected to rigorous requirements by Incoming Quality Control prior to release for manufacture. Minimum inspections for hybrid military products are those specified in MIL-STD-883 Method 5008 for Element Evaluation. Many of these tests are performed more often than required by the military standards. In addition, various other tests are performed to insure the integrity of each raw material. Similar tests are performed on raw materials destined for commercial products.

Travelers used throughout Elantec are structured to maintain traceability of raw materials and operators to each manufacturing lot. Lots are shipped with accurate lot numbers on the containers to provide backward traceability should this ever be required.

In-line Quality Control gates monitor the process to insure critical manufacturing operations are under control. These include wire bond pull, die shear, die and preseal visual inspection, mark permanency, and electrical test.

Before release of any Elantec product, an exhaustive product qualification is performed. This includes life testing on multiple lots and various mechanical package tests. Military products subsequently receive complete Group A, B, C, and D testing per MIL-STD-883 prior to shipment of the first part. On-going Quality Conformance testing is done on military parts in compliance with Method 5008 or Method 5005. This on-going military Quality Conformance testing provides device history for similiar commercial products. Products which do not have military versions receive periodic commercial Quality Conformance testing.

In Conclusion

It has been and continues to be Elantec's goal to provide product of the highest quality available. We believe the extra effort we have expended in the design, construction techniques, testing and quality control procedures results in a product which is observably superior in performance, consistently higher in quality, and provides greater reliability in the actual application. We also believe such product will provide the overall lowest cost and greatest long term satisfaction to the customer.

We at Elantec are proud and confident of our product and therefore offer our unique "Two-for-One" policy in addition to our standard warranty:

IF YOU RECEIVE ANY ELANTEC DEVICE THAT DOES NOT MEET OUR CURRENT PUBLISHED ELECTRICAL SPECIFICATIONS, ELANTEC WILL REPLACE IT WITH TWO GOOD DEVICES.

Summary of Elantec's Reliability and Quality Assurance Policy and Procedures QRA-1

Table I. QA Inspection Sampling Plan

Die Visual:	0.25% AQL			
Precap Visual:	0.25% Military, 1.5% Commercial			
Mark Permanency:	4 Parts/Day/Package			
Electrical Test (All Products):				
Non-Military Lots	**LTPD (%)**	**Sample Size**	**Accept No.**	**Equiv. AQL(%)**
Computer Tests at Room Temp	2	116	0	0.04
Computer Tests Hot	3	76	0	0.07
Computer Tests Cold	5	45	0	0.11
A.C. Bench Tests at Room Temp	2	116	0	0.04
Military Lots				
Computer Tests at Room Temp		116	0	0.04
Computer Tests Hot		116	0	0.04
Computer Tests Cold		116	0	0.04
A.C. Bench Tests at Room Temp		116	0	0.04

Note 1: Computer tests are all D.C. tests plus A.C. on those products where A.C. can be tested on the enhanced LTX automatic tester.

Note 2: All military lots are Q.A. sampled at all temperatures.

Note 3: All non-military lots (E+, Prime, Commercial) are Q.A. sampled at room temperature (D.C.) Until adequate history is developed on these new products, each lot is sample tested at temperatures and on the bench. Non-military lots of mature products with adequate history are skip lot tested at temperatures or on the bench, e.g., they are Q.C. sampled every fourth or fifth lot. (This frequency may change with time as more product history is developed.)

Note 4: If a device which is in skip lot mode should suffer a lot failure, every lot is then tested until three lots in succession are passed before returning to skip lot mode.

Table II. Elantec Hybrid Metal Can Process Flow Summary

Operation	Commercial	Prime(1)	/883B(2)
Incoming QC			
Die Evaluation	X	X	X
Package Evaluation	X	X	X
Raw Material Evaluation	X	X	X
Assembly			
Wire Bond Pull QC	X	X	X
Die Shear QC	X	X	X
Internal Visual	X	X	X
Seal	X	X	X
Stabilization Bake	2 Hours	2 Hours	24 Hours
Temperature Cycling	5 Cycles	5 Cycles	10 Cycles
Constant Accel.			
TO-3, LCC (5KG)	X	X	X
TO-5 (30KG)	X	X	X
TO-8 (20KG)	X	X	30KG
Fine Leak			
TO-3 ($2x10^7$ cc/sec)	X	X	X
TO-5 ($5x10^8$ cc/sec)	X	X	X
TO-8, LCC ($5x10^8$ cc/sec)	X	X	X
Gross Leak			
With Pressurization			X
No Pressurization	X	X	
Class Test		X	X
Burn-in			160 Hours
Electrical Test 25°C(3)	X	X	X
Q.C. 25°C(3)	X	X	X
Electrical Test Cold(3)		X	X
Q.C. Cold(3)	X	X	X
Electrical Test Hot(3)		X	X
Q.C. Hot(3)	X	X	X
External Visual	X	X	X
Group B, C, D Testing			X

Note 1: A prime part is a commercial part tested over the range of −55°C to +125°C.

Note 2: For complete details of Elantec's "/883B" military program see "QRA-3, Elantec's 883B Program for Hybrid Integrated Circuits."

Note 3: Electrical tests performed are as documented on the individual device data sheet.

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Summary of Elantec's Reliability and Quality Assurance Policy and Procedures QRA-1

Table III. Elantec Monolithic Process Flow Summary

Operation	Commercial	Prime(1)	/883B(2)
Incoming QC			
Package Evaluation	X	X	X
Raw Material Evaluation	X	X	X
Assembly			
Wire Bond Pull QC	X	X	X
Die Shear QC	X	X	X
Internal Visual	X	X	X
Seal	X	X	X
Temperature Cycling	5 Cycles	5 Cycles	10 Cycles
Constant Accel. (30KG)(3)	X	X	X
Fine Leak ($5x10^8$ cc/sec)(3)	X	X	X
Gross Leak(3)			
With Pressurization			X
No Pressurization	X	X	
Class Test		X	X
Burn-in			160 Hours(4)
Electrical Test 25°C(5)	X	X	X
Q.C. 25°C(5)	X	X	X
Electrical Test Cold(5)		X	X
Q.C. Cold(5)	X	X	X
Electrical Test Hot(5)		X	X
Q.C. Hot(5)	X	X	X
External Visual	X	X	X
Group B, C, D Testing			X

Note 1: A prime part is a commercial part tested over the range of −55°C to +125°C.

Note 2: For complete details of Elantec's "/883B" military program, see "QRA-2, Elantec's Military Processing-Monolithic Integrated Circuits."

Note 3: Applies to all packages except plastic packages.

Note 4: Military burn-in may be either 150°C for 80 hours or 125°C for 160 hours.

Note 5: Electrical tests performed are as documented on the individual device data sheet.

Elantec manufactures a standard family of monolithic integrated circuits for military applications. Screening and Quality Conformance testing is performed to MIL-STD-883 Class B. Specifics of this program are outlined herein. Parenthetical references utilized in this document indicate applicable Elantec internal specifications.

I. CONTROL SYSTEMS

1.0 Quality Organization

1.1 The Quality Organization at Elantec reports to the President of the corporation. All quality functions are independent of the manufacturing organization.

1.2 Functions under the Quality Organization's control include:

Incoming Inspection
In-Process Quality Control
Internal Audit
Qualification Testing
Quality Conformance Testing
Document Control
Customer Specification Review
Failure Analysis
Material Returns

2.0 ESD (QAP0016) at Elantec

2.1 All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements.

2.2 Shelving at all inventory locations is grounded.

2.3 Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement.

2.4 All operators wear conductive heel straps.

2.5 All product is marked with an equilateral triangle to indicate static sensitivity in accordance with MIL-M-38510.

2.6 Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes or conductive bags.

3.0 Calibration (QAP0003)

3.1 All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by Appendix A paragraph 30.1.1.9 of MIL-M-38510.

4.0 Inspection Systems

4.1 Inspection System Requirements are in accordance with MIL-I-45208.

5.0 Program Plan (QAP0039)

5.1 Elantec maintains a complete Program Plan in accordance with MIL-M-38510. The plan is available for review by customers at Elantec.

5.2 Included within the Program Plan is a complete equipment and facilities list.

6.0 Failure Analysis (QCX0010)

6.1 Elantec has in-house capabilities to perform failure analysis in accordance with MIL-STD-883 Method 5003 Condition A.

II. MANUFACTURING

1.0 Location

1.1 All electrical test, burn-in, and Quality Conformance Testing is performed at Elantec owned facilities located in the United States except moisture resistance, mechanical shock, vibration variable frequency and internal water vapor testing which are performed at DESC certified laboratories. Assembly and mechanical screening operations may be performed at Elantec's facility in Milpitas, Ca. or may be performed at contractors whose procedures are under the control of Elantec.

1.2 Customers desiring all USA manufacture can obtain this service upon special order.

2.0 Incoming Inspection (QAP0006)

2.1 All raw materials used in the manufacture of Elantec circuits are specified by procurement documents. They are inspected by the Incoming Inspection Department prior to release for manufacture.

3.0 Materials

3.1 All package materials and finishes are in accordance with MIL-M-38510.

Elantec 883B Program for Monolithic Integrated Circuits QRA-2

II. MANUFACTURING — Contd.

4.0 Seal

4.1 Prior to package seal on metal can packages, each device is baked in a vacuum oven which is connected to the welder dry box. The seal is performed in a nitrogen purged dry box which is continuously monitored for moisture content. Periodic internal water vapor tests are performed to insure compliance to the 5000 PPM limit.

4.2 Frit seal packages or solder seal packages are sealed in moisture controlled environments. Periodic internal water vapor tests are performed to insure compliance with the 5000 PPM limit.

5.0 Screening (QAP0052)

5.1 Screening is performed in accordance with Method 5004 of MIL-STD-883. A summary of the screening operations is shown in Table I.

5.2 Burn-in is done for 160 hours at 125°C or 80 hours at 150°C. Post-burn-in electrical testing is done within 96 hours of removal of bias. PDA is 5%. Cool-down is performed under bias.

5.3 Electrical test limits, conditions, temperatures, and burn-in circuits are as specified in the appropriate Elantec data sheet. Elantec data sheets show their current revision letter and are fully controlled documents. The latest revision of any data sheet is available from Elantec Specification Control. All 100% test operations are guardbanded, i.e., tested to limits tighter than required by the specification to provide margin for test system variations with time and between machines.

6.0 Marking (MPX0047)

6.1 All devices are marked with the Elantec part number, Elantec logo, 7 character date code indicating Fab quarter code, year and week of seal, the lot within the week of seal, ESD equilateral triangle, and the country of origin, Compliant "C" mark.

6.2 Elantec's standard military devices which comply with the program outlined herein have part numbers which end with "/883B".

III. QUALITY

1.0 Process Quality Control

1.1 Following 100% inspection by manufacturing, die visual and precap visual are Q.C. sample inspected by Quality Control prior to release to the next manufacturing operation.

2.0 Qualification (QAP0055)

2.1 Each Elantec device is tested to the requirements of MIL-M-38510. Elantec Quality and Reliability Assurance performs the function of Qualifying Activity per paragraph 1.2.1 of MIL-STD-883.

3.0 Quality Conformance (QAP0055)

3.1 Group A testing is performed in-line, after each temperature screening test.

3.2 Group B testing is performed per Method 5005 on every inspection lot for each package type. See Table II.

3.3 Group C testing is performed per Method 5005 of MIL-STD-883 which requires Group C be performed at least within 4 calendar quarters prior to the die fabrication date code of product being submitted for acceptance by microcircuit group. Elantec splits its products into several microcircuit groups as is specified by Appendix E of MIL-M-38510 for monolithic devices. Lifetest end point electrical testing is to limits and conditions as specified in the Elantec data sheet and is done at three temperatures within 96 hours of removal of bias. Cooldown is down under bias. See Table III.

3.4 Group D is performed on one lot date code at least once every 52 weeks for each package type. See Table IV.

3.5 All military products are fully qualified by Groups A, B, C, and D Quality Conformance inspections prior to shipment.

IV. PROCESS CHANGES (QAP0002)

1.0 Elantec maintains a fully documented change control system. All manufacturing changes, including those specified by MIL-M-38510, must be submitted to and approved by Elantec Engineering and Quality and Reliability Assurance prior to implementation. Elantec Quality and Reliability Assurance performs the function of "Qualifying Activity" for changes of qualified product as per paragraph 3.4.2 of MIL-M-38510.

V. SPECIFICATION COMPLIANCE

1.0 Elantec "/883B" monolithic military products are manufactured in strict compliance with MIL-M-38510 and MIL-STD-883 with no exceptions or deviations.

Table I. Device Screening

Operation	883 Method	Conditions
Assembly		
Internal Visual	2010 Cond. B	
Seal		
Temperature Cycling	1010 C	
Constant Acceleration	2001 E	
Fine Leak	1014 A1	
Gross Leak	1014 C1	
Class Test		
Mark	Note 1	
Burn-In	1015	125°C, 160 Hours, or 150°C, 80 Hours
Electrical Test		25°C, Elantec Data Sheet (Guardbanded), 96 Hour Window, PDA = 5%
Q.C. (Group A)	5005	25°C, Elantec Data Sheet
Electrical Test		Cold, Elantec Data Sheet (Guardbanded)
Q.C. (Group A)	5005	Cold, Elantec Data Sheet
Electrical Test		Hot, Elantec Data Sheet (Guardbanded)
Q.C. (Group A)	5005	Hot, Elantec Data Sheet
External Visual	2009	
Group B, C, D Hold	5005	Verify Group B, C, and D Data

Note 1: May be performed in any sequence prior to Group B testing.

Table II. Group B Test Outline

Subgroup	Test	883 Method	Sample Size	Acc. No.
2	Resistance to Solvents	2015	4 Devices	0
3	Solderability	2003	3 Devices, 22 Leads Min.	LTPD = 10
5	Bond Strength	2011	4 Devices, 15 Wires Min.	LTPD = 15

Table III. Group C Test Outline

Subgroup	Test	883 Method	Sample Size/LTPD	Acc. No.
1	Pre-Life Electricals		5	
	Steady State Life Test	1005		
	End Point Electricals	Subgroups 1, 2, and 3		

Table IV. Group D Test Outline

Subgroup	Test	883 Method	Sample Size/LTPD	Acc. No.
1	Physical Dimensions	2016	15	
2	Lead Integrity	2004	15	
	Fine Leak	1014		
	Gross Leak	1014		
3	Thermal Shock	1011	15	
	Temperature Cycling	1010		
	Moisture Resistance	1004		
	Fine Leak	1014		
	Gross Leak	1014		
	Visual	1010		
	End Point Electricals	Subgroups 1, 2, and 3		
4	Mechanical Shock	2002	15	
	Vibration, Variable Freq.	2007		
	Constant Acceleration	2001		
	Fine Leak	1014		
	Gross Leak	1014		
	Visual	1011		
	End Point Electricals	Subgroups 1, 2, and 3		
5	Salt Atmosphere	1009	15	0
	Fine Leak	1014		
	Gross Leak	1014		
	Visual	1009		
6	Internal Water Vapor Content	1018	3 or 5	0 or 1
7	Adhesion of Lead Finish	2025	15	0
8	Lid Torque	2024	5	0

Elantec manufactures a standard family of hybrid circuits for military applications in accordance with MIL-M-38534 and MIL-STD-883. Testing is performed to Class B. All manufacturing is done on Elantec's MIL-STD-1772 Certified Line. Specifics of this program are outlined herein. Parenthetical references utilized in this document indicate applicable Elantec internal specifications.

I. CONTROL SYSTEMS

1.0 Certified Line

1.1 Elantec's factory located at 1996 Tarob Ct., Milpitas, Ca. is certified by the Defense Electronics Supply Center (DESC) to the requirements of MIL-STD-1772 (Certification Requirements for Hybrid Microcircuit Facilities and Lines). All Elantec Military Hybrid Products are manufactured at this facility and under the controls of MIL-STD-1772.

2.0 Quality Organization

2.1 The Quality Organization at Elantec reports to the President of the corporation. All quality functions are independent of the manufacturing organization.

2.2 Functions under the Quality Organization's control include:

- Incoming Inspection
- In-Process Quality Control
- Internal Audit
- Qualification Testing
- Quality Conformance Testing
- Document Control
- Customer Specification Review
- Failure Analysis
- Material Returns

3.0 Facility (QAP0030)

3.1 Method 5008 requires that hybrid assembly be performed under Class 100,000 conditions per Fed. Std. No. 209. Elantec assembly and test are performed in a Class 1000 clean room. In addition, all assembly operations from die visual inspection through precap visual are performed under Class 100 laminar flow hoods. The area and hoods are routinely monitored per Fed. Std. No. 209. Temperature and humidity are monitored and controlled in accordance with MIL-STD-883.

3.2 Gases are filtered at point of use.

3.3 De-ionized water is filtered and bacteria controlled and resistivity is continuously monitored.

3.4 All semiconductor work-in-process is stored in nitrogen purged desiccators.

4.0 ESD (QAP0016)

4.1 All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements.

4.2 Shelving at all inventory locations is grounded.

4.3 Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement.

4.4 All operators wear conductive heel straps.

4.5 All product is marked with an equilateral triangle to indicate static sensitivity in accordance with MIL-M-38534.

4.6 Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes.

5.0 Calibration (QAP0003)

5.1 All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by Appendix A paragraph 30.1.1.9 of MIL-M-38534.

6.0 Inspection Systems

6.1 Inspection System Requirements are in accordance with MIL-Q-9858.

7.0 Program Plan (QAP0039)

7.1 Elantec maintains a complete Program Plan in accordance with MIL-M-38534. The plan is available for review by customers at Elantec.

7.2 Included within the Program Plan is a complete equipment and facilities list.

8.0 Failure Analysis (QCX0010)

8.1 Elantec has in-house capabilities to perform failure analysis in accordance with MIL-STD-883 Method 5003 Condition A.

II. MANUFACTURING

1.0 Location

1.1 All Elantec thick film work, assembly, electrical test, and 100% environmental testing is performed at Elantec owned facilities located in the United States. Moisture resistance and internal water vapor testing are performed at DESC certified laboratories.

2.0 Incoming Inspection (QAP0006)

2.1 All raw materials used in the manufacture of Elantec hybrids are specified by procurement documents. They are inspected by the Incoming Inspection Department prior to release for manufacture. Minimum inspections are those specified by Method 5008 of MIL-STD-883 for Element Evaluation. Many tests are performed more often than required by 5008. In addition, various other tests are performed to insure the integrity of the raw materials.

3.0 Materials

3.1 All package materials and finishes are in accordance with MIL-M-38534.

4.0 Seal

4.1 Prior to package seal on metal can packages, each device is baked in a vacuum oven which is connected to the welder dry box. The seal is performed in a nitrogen purged dry box which is continuously monitored for moisture content.

5.0 Screening (QAP0052)

5.1 Screening is performed in accordance with Method 5008 of MIL-STD-883. A summary of the screening operations is shown in Table I.

5.2 Burn-in is done for 160 hours at 125°C. Post-burn-in electrical testing is done with 96 hours of removal of bias. PDA is 10%. Cool-down is performed under bias.

5.3 Electrical test limits, conditions, temperatures, and burn-in circuits are as specified in the appropriate Elantec data sheet. Elantec data sheets show their current revision letter and are fully controlled documents. The latest revision of any data sheet is available from Elantec Specification Control. All 100% test operations are guardbanded, i.e., tested to limits tighter than required by the specification to provide margin for test system variations with time and between machines.

6.0 Marking (MPX0047)

6.1 All devices are marked with the Elantec part number, Elantec logo, 5 character date code indicating year and week of seal, and the lot within the week of seal, ESD equilateral triangle, and USA for country of origin.

III. QUALITY

1.0 Process Quality Control

1.1 Die visual and precap visual are Q.C. sampled to a 0.25% AQL. (QCX0004, QCX0005)

1.2 Wire bond pull testing, both destructive and non-destructive, are performed to limits and with the frequency specified by Method 5008 of MIL-STD-883. (QCX0001)

1.3 Production lots are sample die shear tested during assembly in addition to the testing required by Group B. (QCX0003)

2.0 Qualification (QAP0038)

2.1 Each Elantec device is tested to the requirements of MIL-M-38534. Elantec Quality and Reliability Assurance performs the function of Qualifying Activity per paragraph 1.2.1 of MIL-STD-883.

3.0 Quality Conformance (QAP0038)

3.1 Group A testing is performed in-line, after each temperature screening test. See Table I. (QCX0002).

3.2 Group B testing is performed per Method 5008 on every inspection lot for each package type. See Table II.

III. QUALITY — Contd.

3.3 Group C testing is performed more frequently than required by MIL-M-38534 4.6.2.2.3, which requires it to be done only once in the life of the product for Class B. Elantec performs Group C at least every 26 weeks of seal date code by microcircuit group. Life test endpoint electrical testing is to limits and conditions as specified in the Elantec data sheet and is done at three temperatures within 96 hours of removal of bias. See Table III.

3.4 Group D is performed as required by Method 5008. Testing is done at least once per 6 month period for each package type. See Table IV.

3.5 All 883B products are fully qualified by Groups, A, B, C, and D Quality Conformance inspections prior to shipment.

IV. PROCESS CHANGES (QAP0002)

1.0 Elantec maintains a fully documented change control system. All manufacturing changes, including those specified by MIL-M-38534, must be submitted to and approved by Elantec Engineering and Quality and Reliability Assurance prior to implementation. Additionally, Elantec utilizes multiple sources for semiconductor die to insure availability. Each die type from each vendor is fully qualified for form, fit and function as well as reliability. Internal documentation completely specifies each manufacturing alternative. Elantec Quality and Reliability Assurance performs the function of "Qualifying Activity" for changes of qualified product as per paragraph 4.1.1.1 of MIL-M-38534 and Appendix A.

V. SPECIFICATION COMPLIANCE

1.0 Elantec hybrid military products are manufactured in strict compliance with MIL-M-38534 and MIL-STD-883 with no exceptions or deviations.

Table I. Device Screening

Operation	883 Method	Conditions
Incoming Q.C.	5008 Element Evaluation	
Assembly		
Wire Bond Pull	5008, 2011	
	5008, 2023	
Die Shear Strength	2019	
Internal Visual	2017 Class B	
Seal		
Stabilization Bake	1008C	
Temperature Cycling	1010C	
Constant Acceleration	2001A	(TO-3, LCC)
	2001E	(TO-5, TO-8)
Fine Leak	1014 A1	(TO-3 Limit = 2×10^7 cc/sec)
		(TO-5 Limit = 5×10^8 cc/sec)
		(TO-8 Limit = 5×10^8 cc/sec)
Gross Leak	1014 C1	
Class Test		
Mark	Note 1	
Burn-In	1015	125°C, 160 Hours
Electrical Test		25°C, Elantec Data Sheet (Guardbanded), 96 Hour Window, PDA = 10%
Q.C. (Group A)	5008	25°C, Elantec Data Sheet
Electrical Test		Cold, Elantec Data Sheet (Guardbanded)
Q.C. (Group A)	5008	Cold, Elantec Data Sheet
Electrical Test		Hot, Elantec Data Sheet (Guardbanded)
Q.C. (Group A)	5008	Hot, Elantec Data Sheet
External Visual	2009	
Group B, C, D Hold	5008	Verify Group B, C, and D Data

Note 1: May be performed in any sequence prior to Group B testing.

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Table II. Group B Test Outline

Subgroup	Test	883 Method	Sample Size	Acc. No.
1	Physical Dimensions	2016	2 Devices	0
3	Resistance to Solvents	2015	4 Devices	0
4	Internal Vis. and Mech.	2014	1 Device	0
5	Bond Strength	2011	2 Devices, 11 Wires Ea. Min.	0
6	Die Shear	2019	2 Devices Min.; 22 Internal Elements	0
7	Solderability	2003	1 Device, 15 Leads Min.	0
8	Seal—Fine Leak Gross Leak	1014A1 1014C1	15 Devices	0

Table III. Group C Test Outline

Subgroup	Test	883 Method	Sample Size	Acc. No.
1	External Visual Temperature Cycling Constant Acceleration Fine Leak Gross Leak Visual End Point Electricals	2009 1010C 2001 1014A1 1014C1 1010 Subgroups 1, 2 and 3	15 Devices	0
2	Pre-Life Electricals Steady State Life Test End Point Electricals	 1005 Subgroups 1, 2 and 3	22 Devices	0
3	Internal Water Vapor	1018	3 Devices or 5 Devices	0 1

Table IV. Group D Test Outline

Test	883 Method	Sample Size	Acc. No.
Thermal Shock	1011C	5 Devices	0
Stabilization Bake	1008 (1 Hr.)	5 Devices	0
Lead Integrity	2004B2 or D	1 Device	0
Seal	1014A1 1014C1	5 Devices	0

1.0 Purpose

1.1 To define Elantec's standard Class S Minus process flow for Hybrid products. This flow meets or exceeds all the requirements of MIL-M-38534 for Class B Hybrids but is not fully compliant with the Class S requirements.

2.0 Scope

2.1 This specification applies to Hybrid products processed to Elantec's standard Class S Minus flow.

3.0 Associated Specifications

3.1 Documents specified herein, of the issue in effect on the date of processing, form a part of this drawing to the extent specified herein.

3.2 MIL-STD-883 Test Methods and Procedures for Microelectronics

3.3 MIL-STD-38534 General Military Specification for Hybrid Microcircuits

4.0 Procedure

4.1 Microcircuit and semiconductor dice evaluation requirements shall be per MIL-STD-883, Method 5008, *Class B.*

4.2 Package evaluation shall be per MIL-STD-883, Method 5008, *Class B.*

4.3 In process controls shall be per MIL-STD-883, Method 5008, *Class B.*

4.4 Device screening shall be as specified in Table I herein.

4.5 Qualification/Quality Conformance evaluation shall be performed when specified on the purchase order and shall be per MIL-STD-883 Method 5008, Class S, Groups B, C and D.

4.6 All screening and Quality Conformance testing shall be controlled by an Elantec Custom Process Instruction (CPI).

4.7 If specified on the Purchase Order, data to be shipped shall include: (Otherwise data will be kept on file per MIL-H-38534).

4.7.1 C of C

4.7.2 Pre and Post Burn-in variables. Delta data (if applicable).

4.7.3. Attributes data for Table I Screening.

4.7.4 X-ray Report

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Class S Minus Hybrid Flow QRA-4

Table I. Class S Minus Hybrid Device Flow USA Build

Assembly

Standard MIL Assembly: With the following additional requirements:

1) Wafer Traceability:
2) Piece part traceability and control:
3) Die attach and lead bond monitor every 2 hours plus other standard requirements/shift change, operator change, spool change, machine down, etc.
4) 100% bond pull per MIL-STD-2023 with a 2% PDA (MIL-H-38534 4.5.4).
5) 100% Internal Visual per MIL-STD-2017 Condition A.
6) QA Internal Visual per MIL-H-38534 4.1.2.3 Sample Size 22 accept # = 0.

PRODUCT SCREENING per MIL-STD-883	Method 5008
	|
	Stabilization Bake
	|
	Temp. Cycle
	|
	Constant Acceleration
	|
25% PDA on a max of 5 Passes	PIND Condition A
	|
Elantec imposed electrical screen	25°C
	|
	−55°C
	|
	125°C
	|
	Serialization (serial # and Date code is the device ID)
	|
	XRay
	|
Test read/record if delta's are req'd	25°C electrical Read and Record
	|
Burn/in board 100% socket check *Junction temp max 175°C	Burn-in 160 hours *125°C
	|
	|
96 hour test window	25°C electrical test Go-no-go
	|
Burn/in board 100% socket check	Burn-in 160 Hours *125°C
	|

96 hour test window

25°C electrical Group A
Subgroup 1 parameters Read
and Record
|
Pre Read/Record to post Read/Record
Compute delta's if required
|
PDA check 2% Group A
subgroup 1 & delta parameters
PDA is Base on the # of failures
from the 2nd 160 hours of
burn-in
(F/A required on all functional failures)
|
QA sample 25°C
|
−55°C electrical Go-no-go
|
QA sample −55°
|
125°C electrical Go-no-go
|
QA sample 125°C
|
100% AC tests if applicable
|
QA sample AC tests
|
Mark (remark serial # − if
necesray to keep serial # ID)
|
Solder DIP (if applicable)
|
25°C electrical test
|
Fine/Gross leak 100%
|
100% external Visual
|
Pull QCI Group B, C, & D
samples if applicable
|
Pack
|
Hold or completion of QCI's

Class S Minus Hybrid Flow QRA-4

Group B	MIL-STD-883 Method-5008 TABLE XI	Sample Size
Subgroup 1	Physical Dimensions	2
Subgroup 2	PIND condition A	15
Subgroup 3	Resistance to solvents	4
Subgroup 4	Internal Visual and Mechanical	1
Subgroup 5	Bond Strength min 2 devices (# wires)	45
Subgroup 6	Die shear test	2
Subgroup 7	Solderability min 1 devices (# leads)	15
Subgroup 8	N/A for Class S	
Subgroup 9	Electrostatic Test	3
	Note: Devices are marked with an equilateral triangle.	
	(Note: tested per MIL-H-38534 3.6.8.2)	
Group C	**MIL-STD-883 Method 5008 TABLE XII**	
Subgroup 1	External visual, Temperature cycling	
	Constant Acceleration, Seal Fine/Gross Leak, X-ray	15
	Visual examination external, Electrical test 25°C, −55°C and +125°C	
Subgroup 2	a. Electrical read and record, 25°C, −55°C and +125°C	22
	Group A subgroup 1, 2, 3	
100% board	b. Burn in 1000 hours @ 125°C or 500 Hours @ 150°C	
Socket check	(Note: Must be the same temp as 100% Burn-in)	
	All testing must be completed in 96 hours after removal from burn-in	
	c. Electrical read and record 25°C, −55°C and +125°C	
	Group A subgroup 1, 2, 3	
	d. Complete delta's if applicable	
Subgroup 3	Internal Water Vapor	3
Group D	**MIL-STD-883 Method 5008 TABLE XIII**	
	Thermal Shock	5
	Stabilization Bake	5
	Lead integrity 1 device (# of Leads)	15
	Seal: Fine and Gross Leak	5

Min: samples required Group B 30 devices
Group C 40 devices 15 are Shippable
Group D 16 devices 5 are Shippable

1.0 Purpose

1.1 To define Elantec's standard Class S process flow for Monolithic products.

2.0 Scope

2.1 Applies to Monolithic products processed to Elantec's standard Class S flow.

3.0 Associated Specifications

3.1 Documents specified herein, of the issue in effect on the date of processing, form a part of this drawing to the extent specified herein.

3.2 MIL-STD-883 Test Methods and Procedures for Microelectronics

3.3 MIL-M-38510 General Military Specification for Microcircuits

4.0 Procedure

4.1 Wafer lot acceptance shall be per MIL-STD-883 Method 5007.

4.2 Device Screening shall be as specified in Table I herein.

4.3 Qualification/Quality Conformance shall be performed when specified on the purchase order and shall be per MIL-STD-883 Method 5005, Class S, Groups B and D.

4.4 All screening and Quality Conformance testing shall be controlled by an Elantec Custom Process Instruction (CPI).

4.5 If specified on the Purchase Order, data to be shipped shall include: (Otherwise data will be kept on file per MIL-M-38510)

4.5.1 C of C

4.5.2 Pre and Post Burn-In variable. Delta data (if applicable).

4.5.3 Attributes data for Table I Screening.

4.5.4 X-ray report.

Class S Monolithic Flow QRA-5

Table I. Class S Monolithic Device Flow—USA Build

WAFER LOT ACCEPTANCE PER MIL-S-883 A completed form which contains the data required by method 5007: for each wafer lot. MIL-STD-976 5.1.1.1.1/Rework limitations per M-M-38510 3.7.1	M-5007 | WAFER TRACEABILITY | WAFER THICKNESS | METALIZATION THICKNESS | THERMAL STABILITY | SEM | GLASSIVATION THICKNESS | GOLD BACKING THICKNESS (when applicable)

Assembly

Standard Mil Assembly, with the following additional requirements:

1) Wafer traceability.
2) Piece part traceability and control.
3) Die attach and lead bond monitor every 2 hours plus other standard requirements/shift change, operator change, spool change, machine down, etc.
4) 100% bond pull per MIL-STD-2023 with a 2% PDA (M-M-38510 4.6.5).
5) 100% Internal Visual per MIL-STD-2010 Condition A..
6) The start of assembly to final seal must be completed within 6 weeks.

Product Screening Per MIL-STD-883 Method 5004

	Temp. Cycle
	Constant Acceleration
25% PDA on a max of 5 Passes	PIND Condition A
Elantec imposed electrical screen	+25°C
	−55°C
	+125°C
	Serialization (Serial # and Date Code is the device ID)
	X Ray
Test read/record if delta's are required	25°C Electrical Read and Record
Burn-In board 100% socket check	Burn-In 72 hours *150°C (Reverse bias if applicable)
96 hour test window	25°C Electrical Test Go-No-Go
Burn-In board 100% socket check	Burn-In 240 hours *125°C or 120 hours *150°C
96 hour test window	25°C Electrical Group A Subgroup 1 parameters Read and Record

*Junction temp max 175°C

Product Screening Per MIL-STD-883 Method 5004 — Contd.

Pre Read/Record to post Read/Record

Compute delta's if required
|
PDA check 5% Group A
subgroup 1 and delta parameters
and 3% for functional failures
(F/A required on all functional failures)
|
QA sample 25°C
|
−55°C Electrical Go-No-Go
|
QA sample −55°C
|
125°C Electrical Go-No-Go
|
QA sample 125°C
|
100% AC tests if applicable
|
QA sample AC tests
|
Mark (remark serial #—if
necessary to keep serial #ID)
|
Solder DIP (if applicable)
|
25°C Electrical Test
|
Fine/Gross Leak 100%
|
100% External Visual
|
Pull QCI Group B
|
Pull QCI Group D (or check for generic data)
|
Pack
|
Hold for completion of QCI's

Group B M-5005 Table IIa

Subgroup	Description	Sample Size
Subgroup 1	* a. Physical Dimensions * b. Internal Water Vapor (cerDIPs only)	2 3
Subgroup 2	a. Resistance to solvents b. Internal Visual and Mech. c. Bond Strength min 4 devices (# wires) d. Die shear test	4 2 22 3
Subgroup 3	a. Solderability min 3 devices (# leads)	22
Subgroup 4	* a. Lead Integrity b. Fine and Gross leak c. Lid Torque (cerDIPs only)	2
Subgroup 5	a. Electrical read and record LTPD = 5 25°C, −55°C and 125°C Group A subgroup 1, 2, 3	45
100% board socket check	b. Burn-In 1000 hours @ 125°C or 500 hours @ 150°C (Note: Must be the same temp. as 100% Burn-In)	
All testing must be completed in 96 hrs. after removal from burn-in	c. Electrical read and record 25°C, −55°C and 125°C Group A subgroup 1, 2, 3 b. Compute delta's if applicable	
Subgroup 6	a. Electrical read and record LTPD = 5 25°C, −55°C and 125°C Group A subgroup 1, 2, 3 Temperature cycling 100 cycles b Temperature cycling 100 cycles (see copy) c. Constant acceleration d. Fine and Gross leak e. Electrical read and record 25°C, −55°C and 125°C Group A subgroup 1, 2, 3	15

* Not required if Group D is performed on the same lot.

Group D Method 5005 Table IV Group D requirements are the same as Class B processing.

Min. Samples Required Group B 67 Devices 45 may be shippable
Group D 65 Devices All destructive

Elantec is an active participant in the DESC Drawing standardization program. This is a program administered by the Defense Electronics Supply Center (DESC) in Dayton, Ohio. Under this program, a MIL-STD-1772 certified manufacturer, such as Elantec, may supply hybrid devices to many customers using one government controlled specification instead of having each customer create his own Source Control Drawing (SCD). Elantec treats these devices as standard parts, i.e., they are built to be inventoried at both Elantec and our distributors in anticipation of customer orders rather than being built to order. This practice lowers costs, shortens lead times, and improves quality.

At publication time, this is the list of devices for which Elantec is an approved supplier: (*Devices pending DESC release)

DESC/SMD Drawing Number	Generic Part Number
7801301GX	Obsolete—See 7801301XX
7801301XX	ELH0002H/883B
8001301ZX	ELH0032G/883B
8001401ZX	ELH0033G/883B
8508701ZX	ELH0041G/883B
8508801YX	ELH0021K/883B
8508901YX	ELH0101AK/883B
8508902YX	ELH0101K/883B
*5962-89620	EL2020
*5962-89623	EL2003
5962-87783	EHA2400/883B
*5962-87787	EHA2539/883B
*5962-89648	EHA2540/883B
*5962-87784	EHA5190/883B

Electro Static Discharge (ESD) Sensitivity

All semiconductor devices are sensitive to Electro Static Discharge (ESD) to some degree. For this reason, Elantec treats *all* of our devices as sensitive. Customers are urged to use similar controls throughout their facilities. This will optimize yields, prevent latent reliability problems, and eliminate component quality complaints which are due to ESD. Even components which are returned to Elantec for analysis should be handled with proper ESD procedures.

Device Design and Processing

Wherever possible, ESD protection networks are used on device pins. Metal routing and oxide thicknesses are carefully considered for optimum ESD performance. Testing per MIL-STD-883 Method 3015 is used to determine device and process performance.

Work Areas

Floors are covered with conductive tiles, attached with conductive adhesive.

Operators wear non-static generating or static dissipative smocks. Heel straps are used to ground the operators. Heel straps are checked daily for effectiveness.

Work station surfaces are conductive laminates or stainless steel. These are tied to Earth ground through protective resistors. Grounds are routinely inspected. Air ionizers are used to neutralize charges in areas which may generate static.

Storage shelving is grounded through protective resistors.

Handling

All handling containers (boxes, bags, etc.) are conductive. Pink poly which depends on surface properties and may wear out is not used. Common plastics (such as polystyrene and polypropylene) which are nasty static generators are *never* used in the work area.

Marking

All devices are marked with an equalateral triangle to warn the user that they are ESD sensitive.

Packaging

Devices are packed in either antistatic materials which are surrounded by a conductive Faraday shield or directly in conductive materials. The shielded containers are labeled with a yellow ESD warning label. Only antistatic treated "popcorn" is used as filler material in shipping boxes.

élantec HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS *A Quality Approach:*

How Analog IC Data Sheets Support A Commitment to Excellence

Preface

Elantec is a manufacturer of high performance analog integrated circuits. The company was founded in 1983 to design, manufacture and market high performance analog devices for military and high performance commercial applications. The company offers high speed analog devices with both hybrid and monolithic processes.

Attaining Excellence

"Communication—such as that provided by data sheets—is one of the cornerstones of a quality platform."

Quality—the word is no newcomer to the American semiconductor industry, but realizing a state of quality has been a long and arduous path marked by some much-publicized pitfalls.

It's a common enough term, but quality is a big issue. The goal of realizing AOQL's (Average Outgoing Quality Levels) to satisfy commercial users or the Department of Defense is elusive enough to warrant revisiting what is meant by the word quality and what steps can be taken before a device leaves its homefront to ensure satisfaction.

Communication—such as that provided by data sheets—is one of the cornerstones of a quality platform. The industry relies on data sheets for critical device characterization and testing information. This form of communication is the lifeblood of a device's utility to the customer, and of the manufacturer-customer relationship.

... And Guaranteeing the Quality Commitment

Elantec realized at its inception in 1983 that customers want up-to-date, complete and accurate data on each part, and has turned this need into an opportunity to differentiate itself in the marketplace by providing data sheets that really add value. The benefit for the customer: cost savings by avoiding time-consuming dialog with the manufacturer resulting from inadequate information. And, of course, further savings provided by parts that work as promised.

The Quality Cycle

"... thorough test development and characterization ..."

At Elantec, the quality cycle begins in design, is reinforced by thorough test development and characterization, and is ensured with diligent testing—often more than is required—and extends throughout our relationship with the customer. The data sheets initially available with the product are labeled "Rev A" (Revision A), letting customers know from the outset that literature updates—labeled "Rev B," and so on—will be available on the product over time. Further, "Engineering Change Notices" (ECNs) may supplement the initial product literature when a specification change is necessary or if a misunderstanding results from ambiguous wording in the original data sheet, and clarification is necessary.

Data Sheets as a Communications Vehicle

"A data sheet is a user's owner's manual..."

A data sheet is a user's "owner's manual" to that device. Clearly, a person wouldn't use a 1986 car owner's manual as a guideline to set the valve clearance on a 1987 model—but that, in effect, is what the engineering community does every day with the data sheets provided them by many manufacturers. The trouble is, the data sheet seems to match the part, when actually it may be out of date, ambiguous or lacking in critical information necessary for accurate device characterization.

Many users end up testing parts to specs for which they were never guaranteed simply because the data sheet didn't tell them otherwise. The result can render good parts "rejects" and cause unnecessary tension and costly dialog. Elantec publishes more information in its data sheets than is commonly found, ensuring that the customer fully understands the parameters within which the part has been tested. This avoids misunderstanding about what Elantec has promised the part will do.

Elantec differentiates its data sheets—and by extension, the way it approaches quality and service—by publishing test levels and test conditions, and by stating the sample test plan on which those tests are based. Test levels on *each* parameter precisely defines the stringent testing. The entire sample test plan is a controlled document which is available upon request.

Many data sheets offered in the industry are difficult to interpret, and can force a dialog between the customer and manufacturer that costs time and money. Often, important electrical test conditions are omitted, paving the way for the customer to be led astray.

A Quality Approach:

For instance, a data sheet may guarantee minimum and maximum values for critical parameters, but not specify whether the parameters are tested over the operating temperature range or limited to room temperature testing. Elantec's test levels state whether the lot was tested 100% (every part), sample tested or not tested at all.

"... ambiguities cost the user money..."

Such ambiguities can create design and test problems. Most analog ICs, especially hybrid circuits, cannot be guaranteed to operate within the minimum and maximum specifications over the full operating range without being tested at the temperature extremes. These ambiguities cost the user money, and those costs escalate as the part moves further into the manufacturing cycle. The Air Force Systems Command conservatively estimates that a $5 part costs as much as $5000 to replace at the systems level, and can soar to $15,000 once the part is in its final application.

Further, the price of ambiguities can be born out when designers use data sheet information to develop source control drawings (SCDs), and the more generations away from the original document that the misinformation gets, the harder it is to track to the source and correct. That is why we provide data sheets with more than the typical amount of information. As stated, the quality commitment at Elantec begins long before the device is shipped. Stringent in-house specifications and test methods are employed to eliminate guesswork on the customer's part.

Guardbanding— A Margin of Insurance

One of these stringent test methods is guardbanding, or the practice of testing to tighter limits than specified to the customer. Elantec practices guardbanding to provide for the limits of machine tolerance, or the tendency for machines to vary slightly when testing the same device. One machine will vary slightly in its testing results from day to day. Or, one machine's performance will vary a little from that of a similar machine.

"... to provide for the limits of machine tolerance..."

For instance, the customer may use the same type of machine as we do, such as an LTX 77, but there can be variations even within like machines. Or the customer may use a machine from a different test equipment manufacturer, and of course, there will be certain variations within dissimilar machines. So, since we test beyond what we publish in the data sheet, the customer gains a "margin of insurance" that the part will perform to stated test levels.

Double Guardbanding— A Unique Value-Added

At Elantec, both the production and quality assurance departments test our parts. "Production" tests three machine tolerances tighter than stated on the data sheets. Then, as yet another precaution, QA sample tests one machine tolerance tighter than the data sheet. This eliminates the possibility of a customer finding a part not within a given spec because of normal machine variances.

"... tests three machine tolerances tighter..."

Every MIN/MAX Limit is Tested and Published

"Thus, the user knows . . . "

Elantec publishes any and all test conditions whose absence may foster ambiguity. For instance, as the area of temperature testing can be particularly thorny in the analog IC world, Elantec takes care to state the ranges or limits to which parts have been tested. In the case of AC temperature testing, these tests are normally performed at room temperature for off the shelf parts, so the headings of the AC characteristics table on the data sheet list 25°C as the test temperature. We do not imply that AC testing applies over the operating temperature range. Thus, the user knows that min/max guarantees are for this temperature and that full range tests must be additionally ordered before min/max guarantees can apply over the full operating range.

Many analog ICs inherently have certain parameters that never fail if other parameters pass their tests. Industry-wide, such parameters are said to be "guaranteed by design and characterization data." To ensure no misunderstanding, however, Elantec calls these parameters out on the data sheet. Every part is tested on each min/max limit, either 100 percent of the lot, by samples, or by direct mathematical correlation to another test performed. Whichever the case, the test level defines it completely.

On commercial parts, if historical data shows a parameter has never failed on a particular type of IC, we may sample test every fifth lot or every tenth lot, depending on the parameter. If we detect a failure, however, we sample test every lot until three consecutive lots have passed. Lots which fail are tested 100 percent.

Rejects as an Opportunity

". . . to determine where the problem lies . . . "

Inherent in any cycle is a return to the starting point. Naturally, some customers do find it necessary to return parts that didn't pass their tests. We view the customer's input as an opportunity to improve, and work diligently to find out why the part didn't perform as expected. Sometimes there was a discrepancy between the way we tested and the way the customer tested, or an attempt was made by the customer to test the part to rigors for which it wasn't intended. Whichever the case, we invest the required effort to determine where the problem lies and work the issue with the customer.

The Quality Cycle—Completed

"quality is more than a part that works."

Data sheets are too critical a part of quality to allow them to be just marketing tools or lip service. Clearly, quality is more than a part that "works." Accurate device characterization and system design cannot happen without complete and accurate communication as an integral part of the supplier-customer relationship. Data sheets, then, can and should be a vital link in the quality cycle.

Elantec Die Sales, Policies/Procedures

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

The following information applies to Elantec's Complementary Bipolar processed devices. For products manufactured with alternate technologies, contact factory for further information.

Elantec's monolithic high performance products are well suited to hybrid assembly applications and are available in die form. Following are Elantec's die sales policies and procedures.

1. Construction

   Elantec Complementary Bipolar dice are nominally 20 mils thick. Backsides are polysilicon which is suitable to either epoxy or eutectic die attach. Gold backing is not available.

2. Die Attach Recommendations

   The back side of all Elantec integrated circuits are electrically isolated from the active circuitry. It is not, therefore, necessary to make explicit connection to V−. There are, however, some devices whose AC characteristics are enhanced by connection to V−. See commercial datasheets for packaged device connections.

   Eutectic die attach can be implemented in metal cans without the requirement of a preform. Die attach should be done on a heater block at 440 ±10°C for a duration not to exceed 1 minute. In general, eutectic die attach to a ceramic substrate with gold die attach pads will not require a preform as well. In the LCC and CerDIP, die attach is abetted by the use of Gold Silicon preform.

3. Wafer Sort

   All die are 100% electrically tested at 25°C to test limits and conditions specified in each die data sheet. Due to variations in assembly methods and normal yield loss, Elantec does not guarantee specifications after packaging for standard dice. Some devices are not available in die form for all packaged grades offered due to the electrical selection used on the package parts which cannot be done at the die level.

4. Die Separation

   All wafers are sawn 100% through to minimize silicon chipping which may cause subsequent particles in the packaged device. Inked reject dice are removed.

5. Visual Inspection

   Each die is inspected to MIL-STD-883 Method 2010 Condition B. Visual rejects are removed. Quality control visually inspects each lot to a 0.25% AQL sample. Elantec guarantees the visual quality to this level.

6. Passivation

   Elantec uses a three-layer passivation process which provides the best reliability and protection available for our integrated circuits. First, a layer of undoped silicon dioxide is deposited. Next, a layer of doped silicon dioxide is applied. The third layer constitutes another deposition of undoped silicon dioxide. This glassivation protects the die from environmental conditions and damage during assembly.

7. Mechanical Information

   Aluminum metallization with a nominal thickness of 10,000 angstroms is standard for all devices. Die thickness is 20 mils nominal, and bonding pad size is typically 4.0 mils x 4.0 mils. See individual die data sheets for specific pad size.

8. Wire Bonding Recommendations

   The use of 1.25 mil Aluminum ultrasonic wire bonds is recommended. (For power products, 2 mil Aluminum ultrasonic wire bonds should be used.) The package holding fixture should not be heated. For hybrid applications on ceramic substrates, thermosonic 1 mil Gold wire may be used.

9. Shipping

   Die are packed in conductive waffle packs. All waffle packs are full, except for the last waffle pack in a lot, which may be a partial. Each waffle pack may be separated and fastened together with a two piece clip or groups of 5 to 10 waffle packs may be stacked and fastened together with a two piece clip. Each waffle pack or stack of waffle packs is identified with the device part number, wafer lot number, inspection level, quantity, and a QC stamp to indicate the lot was QC visual accepted. Each pack, or stack, is then heat sealed in a conductive bag. Only one wafer lot is placed in each bag.

10. Traceability

    Each waffle pack, or stack, has a wafer lot number which is traceable to the wafer manufacturing lot. The wafer fabrication paperwork is archived at Elantec for a period of 5 years. This documentation is proprietary and is not available for shipment to customers.

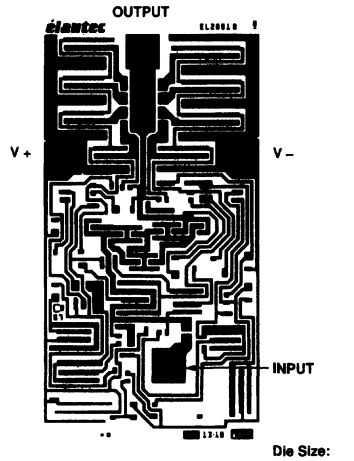
EL2001D Die
Low Power, 70 MHz Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ – V–)	±18V or ±36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
T_{ST}	Storage Temperature	–65°C to +150°C
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



Die Size:
35 x 59 MILS

DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, T_A = 25°C

Parameter	Description	Test Conditions		Limits			Test Level	Units
		V_{IN}	Load	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	–10	2	10	I	mV
I_{IN}	Input Current	0	∞	–3	1	3	I	µA
R_{IN}	Input Resistance	±12	100Ω	3	8		I	MΩ
A_{V1}	Voltage Gain	±12	∞	0.990	0.998		I	V/V
A_{V2}	Voltage Gain	±10	100Ω	0.83	0.93		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	100Ω	0.82	0.89		I	V/V
V_O	Output Voltage Swing	±12V	100Ω	±10	±11		I	V
R_{OUT}	Output Resistance	±2V	100Ω		10	15	I	Ω
I_{OUT}	Output Current	±12V	(Note 2)	±100	±160		I	mA
I_S	Supply Current	0	∞		1.3	2	I	mA
PSRR	Supply Rejection (Note 3)	0	∞	60	75		I	dB

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: Force the input to +12V and the output to +10V and measure the output current. Repeat with –12V in and –10V on the output.

Note 3: V_{OS} is measured at V_S+ = +4.5V, V_S– = –4.5V and at V_S+ = +18V, V_S– = 18V. Both supplies simultaneously.

EL2002D Die

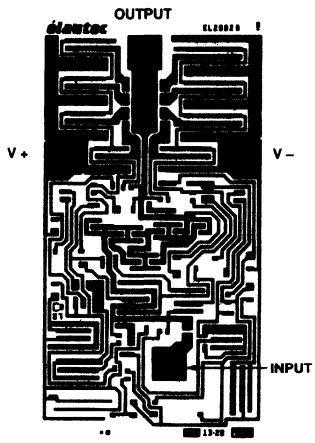
Low Power, 180 MHz Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ – V–)	±18V or ±36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
T_{ST}	Storage Temperature	–65°C to +150°C
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



Die Size:
35 x 59 MILS

DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, T_A = 25°C

Parameter	Description	Test Conditions		Limits			Test Level	Units
		V_{IN}	Load	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	–15	5	15	I	mV
I_{IN}	Input Current	0	∞	–10	3	10	I	µA
R_{IN}	Input Resistance	±12	100Ω	1	3		I	MΩ
A_{V1}	Voltage Gain	±12	∞	0.990	0.998		I	V/V
A_{V2}	Voltage Gain	±10	100Ω	0.85	0.93		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	100Ω	0.83	0.91		I	V/V
V_O	Output Voltage Swing	±12V	100Ω	±10	±11		I	V
R_{OUT}	Output Resistance	±2V	100Ω		8	13	I	Ω
I_{OUT}	Output Current	±12V	(Note 2)	±100	±160		I	mA
I_S	Supply Current	0	∞		5	7.5	I	mA
PSRR	Supply Rejection (Note 3)	0	∞	60	75		I	dB

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: Force the input to +12V and the output to +10V and measure the output current. Repeat with –12V in and –10V on the output.

Note 3: V_{OS} is measured at V_S+ = +4.5V, V_S– = –4.5V and at V_S+ = +18V, V_S– = 18V. Both supplies simultaneously.

EL2003D Die

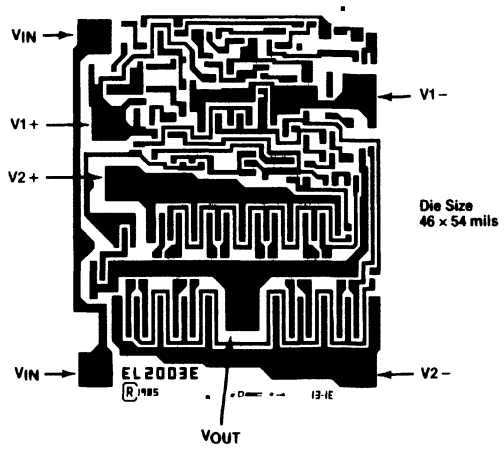
100 MHz Video Line Driver

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ – V–)	±18V or ±36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
	Output Short Circuit Duration (Note 3)	Continuous
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, T_A = 25°C

Parameter	Description	Test Conditions		Limits			Test Level	Units
		V_{IN}	Load	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	−40	5	40	I	mV
I_{IN}	Input Current	0	∞	−25		25	I	µA
R_{IN}	Input Resistance	±12V	100Ω	1	2		I	MΩ
A_{V1}	Voltage Gain	±12V	1 kΩ	0.98	0.99		I	V/V
A_{V2}	Voltage Gain	±6V	50Ω	0.83	0.90		I	V/V
A_{V3}	Voltage Gain, V_S = ±15V	±3V	50Ω	0.82	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	1 kΩ	±13	±13.5		I	V
V_{O2}	Output Voltage Swing	±12V	100Ω	±10.5	±11.3		I	V
R_{OUT}	Output Resistance	±2V	50Ω		7	10	I	Ω
I_{OUT}	Output Current	±12V	(Note 2)	±105	±230		I	mA
I_S	Supply Current	0	∞		10	15	I	mA
PSRR	Supply Rejection (Note 3)	0	∞	60	80		I	dB

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

Note 3: V_S = ±4.5V to ±18V.

EL2008D Die

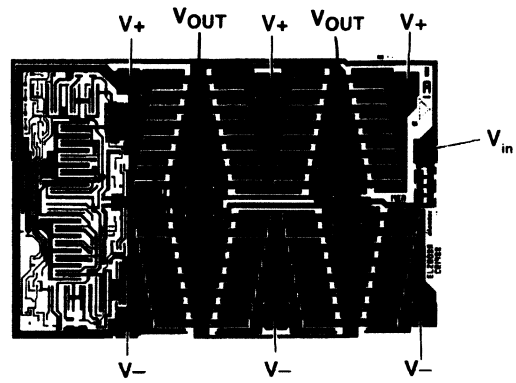
55 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ – V–)	±18V or ±36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
t_{SH}	Output Short Circuit Duration (Note 2)	Continuous
T_A	Operating Temperature Range	−55°C to +125°C
T_J	Operating Junction Temp.	+175°C
T_{ST}	Storage Temp. Range	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 94 x 141 MILS

DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, T_A = 25°C

Parameter	Description	Test Conditions		Limits			Test Level	Units
		V_{IN}	Load	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	−40	10	40	I	mV
I_{IN}	Input Current	0	∞	−35	−5	35	I	µA
R_{IN}	Input Impedance	±12V	100Ω	0.5	2		I	kΩ
A_{V1}	Voltage Gain	±10V	∞	0.985	0.9995		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	0.88	0.91		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	10Ω	0.87	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	100Ω	±13			I	V
V_{O2}	Output Voltage Swing	±12V	10Ω	±10.5	±11		I	V
R_{O1}	Output Impedance	±10V	±10 mA		1.8	2.5	I	Ω
R_{O2}	Output Impedance	±10V	±1A		0.8	1.0	I	Ω
I_O	Output Current	±12V	(Note 3)	1.4	1.8		I	A
I_S	Supply Current	0	∞	9	13	22	I	mA
PSRR	Supply Rejection (Note 4)	0	∞	60			I	dB
V_S+, V_S-	Supply Sensitivity (Note 5)		∞			2	I	mV/V

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: During Output Short Circuit test the junction temperature rises and can activate the Thermal Shutdown circuit. A heat sink will lower the junction temperature below the trip point.

Note 3: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

Note 4: V_S + = ±4.5V then V_S is changed to ±18V.

Note 5: V_S+ = +15V, V_S− = −4.5V then V_S− is changed to −18V and V_S− = −15V, V_S+ = +4.5V then V_S+ is changed to +18V.

EL2009D Die

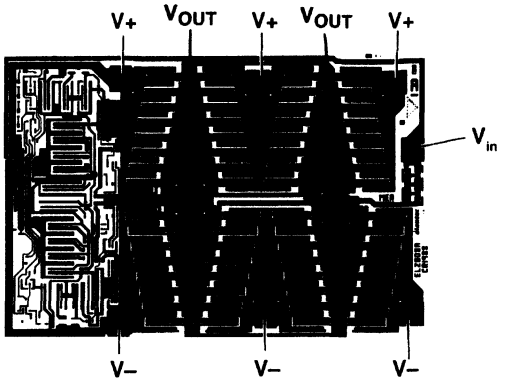
90 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ –V–)	±18V or ±36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
t_{SH}	Output Short Circuit Duration (Note 2)	Continuous
T_A	Operating Temperature Range	−55°C to +125°C
T_J	Operating Junction Temp.	175°C
T_{ST}	Storage Temp. Range	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 94 x 141 MILS

DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, T_A = 25°C

Parameter	Description	Test Conditions		Limits			Test Level	Units
		V_{IN}	Load	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	−60		60	I	mV
I_{IN}	Input Current	0	∞	−125	−5	125	I	µA
R_{IN}	Input Impedance	±12V	100Ω	250	900		I	kΩ
A_{V1}	Voltage Gain	±10V	∞	0.985	0.999		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	0.88	0.90		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	10Ω	0.87	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	100Ω	±13			I	V
V_{O2}	Output Voltage Swing	±12V	10Ω	±10.5	±11		I	V
R_{O1}	Output Impedance	±10V	±10 mA			1.5	I	Ω
R_{O2}	Output Impedance	±10V	±1A		0.9	1.0	I	Ω
I_O	Output Current	±12V	(Note 3)	1.4	1.8		I	A
I_S	Supply Current	0	∞	30	45	65	I	mA
PSRR	Supply Rejection (Note 4)	0	∞	60			I	dB
V_S+, V_S−	Supply Sensitivity (Note 5)		∞			2	I	mV/V

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: During Output Short Circuit test the junction temperature rises and can activate the Thermal Shutdown circuit. A heat sink will lower the junction temperature below the trip point.

Note 3: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V input and −10V on the output.

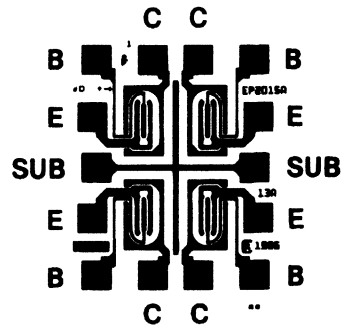
Note 4: V_S = ±4.5V then V_S is changed to ±18V.

Note 5: V_S+ = +15V, V_S− = −4.5V then V_S− is changed to −18V and V_S− = −15V, V_S+ = +4.5V then V_S+ is changed to +18V.

EP2015D Die
Fast Quad PNP Array

Absolute Maximum Ratings (T_A = 25°C)

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
T_A	Operating Temperature Range	−55°C to +125°C
T_S	Storage Temperature	−65°C to +150°C
T_J	Maximum Junction Temperature	150°C
V_{CB}max	40V	
V_{EB}max	5V	
V_{CE}max	40V	
$I_C$max	50 mA	
$I_B$max	10 mA	



DIE SIZE: 38 x 45 MILS

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.

DC Electrical Characteristics T_A = 25°C

Parameter	Test Conditions	Min	Typ	Max	Test Level	Units
ΔV_{BE} (Note 1)	V_{CE} = 4V, I_C = 1 mA			5	I	mV
ΔH_{fe1}(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA			10	I	%
ΔH_{fe2}(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA			10	I	%
H_{fe1}(Note 3)	V_{CE} = 1V, I_C = 0.1 mA	75			I	
H_{fe2}(Note 3)	V_{CE} = 1V, I_C = 0.1 mA	75			I	
V_{BEsat} (Note 3)	I_C = 10 mA, I_B = 1 mA			0.90	I	V
V_{CEsat} (Note 3)	I_C = 10 mA, I_B = 1 mA			0.20	I	V
BV_{ceo} (Note 3)	I_C = 1 mA, I_B = 1 mA	40			I	V
BV_{cbo} (Note 3)	I_C = 10 μA, I_E = 0 mA	40			I	V
BV_{ebo} (Note 3)	I_B = 10 μA, I_C = 0 mA	5			I	V
I_{cbo} (Note 3)	V_{CB} = 30V, I_E = 0 mA			50	I	nA
I_{ebo} (Note 3)	V_{CB} = 4V, I_C = 0 mA			50	I	nA

Note 1: ΔV_{BB} and ΔH_{fe} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{fe} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.

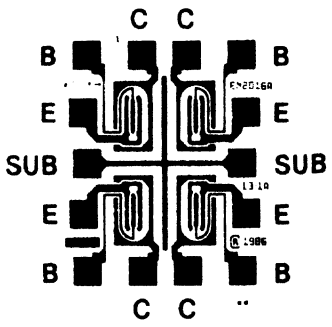
EN2016D Die
Fast Quad NPN Array

Absolute Maximum Ratings (T_A = 25°C)

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
T_A	Operating Temperature Range	−55°C to +125°C
T_S	Storage Temperature	−65°C to +150°C
T_J	Maximum Junction Temperature	150°C
V_{CB}max	40V	
V_{EB}max	5V	
V_{CE}max	40V	
$I_C$max	50 mA	
$I_B$max	10 mA	

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 38 x 45 MILS

DC Electrical Characteristics T_A = 25°C

Parameter	Test Conditions	Min	Typ	Max	Test Level	Units
ΔV_{BE} (Note 1)	V_{CE} = 4V, I_C = 1 mA			5	I	mV
ΔH_{fe1}(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA			20	I	%
ΔH_{fe2}(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA			20	I	%
H_{fe1}(Note 3)	V_{CE} = 1V, I_C = 0.1 mA	75			I	
H_{fe2}(Note 3)	V_{CE} = 1V, I_C = 1.0 mA	75			I	
V_{BEsat} (Note 3)	I_C = 10 mA, I_B = 1 mA			0.90	I	V
V_{CEsat} (Note 3)	I_C = 10 mA, I_B = 1 mA			0.20	I	V
BV_{ceo} (Note 3)	I_C = 1 mA, I_B = 1 mA	40			I	V
BV_{cbo} (Note 3)	I_C = 10 μA, I_E = 0 mA	40			I	V
BV_{ebo} (Note 3)	I_B = 10 μA, I_C = 0 mA	5			I	V
I_{cbo} (Note 3)	V_{CB} = 30V, I_E = 0 mA			50	I	nA
I_{ebo} (Note 3)	V_{CB} = 4V, I_C = 0 mA			50	I	nA

Note 1: ΔV_{BE} and ΔH_{fe} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{fe} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.

EL2018D Die

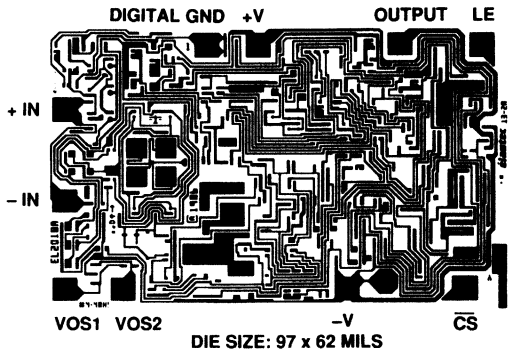
Fast, High Voltage Comparator with Transparent Latch

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V
V_{IN}	Input Voltage	$+V_S$ to $-V_S$
ΔV_{IN}	Differential Input Voltage	Limited Only by Power Supplies
I_{IN}	Input Current	±10 mA
I_{INS}	Input Current	±5 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 97 x 62 MILS

DC Electrical Characteristics V_S = ±15V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_{OS} = 1.4V		1	3	I	mV
I_B	Input Bias Current V_{CM} = 0V, pin 2 or 3		100	300	I	nA
I_{OS}	Input Offset Current V_{CM} = 0V		30	150	I	nA
CMRR	Common Mode Rejection Ratio (Note 2)	85	105		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	85	100		I	dB
V_{CM}	Common Mode Input Range	±12	±13		I	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	15	40		I	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	−0.05	0.15	0.4	I	V
V_{OH}	Output Voltage Logic High V_S = ±15V	3.5	4	4.5	I	V
	V_S = ±5V	2.7	3	3.3	I	V

EL2018D Die
Fast, High Voltage Comparator with Transparent Latch

DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
Vodis1	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA					
	$V_S = \pm 15V$	4.8			I	V
	$V_S = \pm 5V$		3.5		I	V
Vodis2	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $\pm 15V$	−0.3	−1		I	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	2			I	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage			1	I	V
I_{IN}	LE or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ to 5V			300	I	μA
I_{S+en}	Positive Supply Current Enabled		8.4	10	I	mA
I_{S+dis}	Positive Supply Current Disabled		4.7	6	I	mA
I_{S-en}	Negative Supply Current Enabled		13	17	I	mA
I_{S-dis}	Negative Supply Current Disabled		5	6.5	I	mA

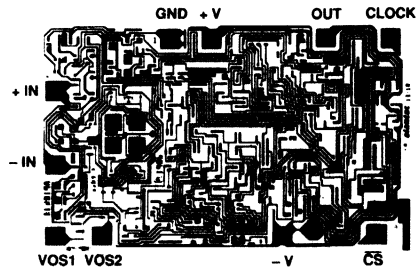
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = +12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to 15V.

EL2019D Die

Fast, High Voltage Comparator with Master Slave Flip-Flop

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V
V_{IN}	Input Voltage	$+V_S$ to $-V_S$
ΔV_{IN}	Differential Input Voltage	Limited Only by Power Supplies
I_{IN}	Input Current	±10 mA
I_{INS}	Input Current	±5 mA
T_J	Maximum Junction Temperature	175°C



DIE SIZE:
97 x 62 MILS

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.

DC Electrical Characteristics V_S = ±15V, T_A = 25°C, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_{OS} = 1.4V		1.5	5	I	mV
I_B	Input Bias Current V_{CM} = 0V, pin 2 or 3		100	300	I	nA
I_{OS}	Input Offset Current V_{CM} = 0V		30	150	I	nA
CMRR	Common Mode Rejection Ratio (Note 2)	75	105		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	75	100		I	dB
V_{CM}	Common Mode Input Range	±12	±13		I	V
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	−0.05	0.15	0.4	I	V
V_{OH}	Output Voltage Logic High V_S = ±15V V_S = ±5V	 3.5 2.4	 4	 4.65	 I I	 V V

EL2019D Die

Fast, High Voltage Comparator with Master Slave Flip-Flop

DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise specified — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
Vodis1	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA $V_S = \pm 15V$	4.6			I	V
	$V_S = \pm 5V$		3.65		I	V
Vodis2	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $\pm 15V$	−0.3	−1		I	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	2			I	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage			0.8	I	V
I_{IN}	LE or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ to 5V			200	I	μA
I_{S+en}	Positive Supply Current Enabled		8.8	11	I	mA
I_{S+dis}	Positive Supply Current Disabled		4.9	6	I	mA
I_{S-en}	Negative Supply Current Enabled		14.5	17	I	mA
I_{S-dis}	Negative Supply Current Disabled		6.4	8	I	mA

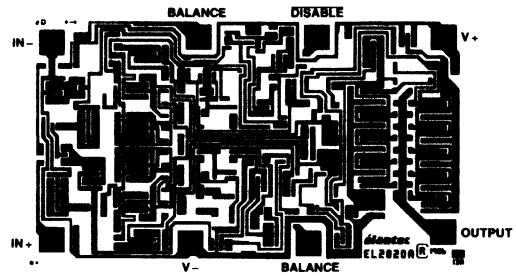
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = +12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to 15V.

EL2020D Die

50 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V
V_{IN}	Input Voltage	±15V or V_S
ΔV_{IN}	Differential Input Voltage	±10V
I_{IN}	Input Current (Pins 2 or 3)	±10 mA
I_{INS}	Input Current (Pins 1, 5, or 8)	±5 MA
I_{OP}	Peak Output Current	Short Circuit Protected
	Output Short Circuit Duration	Continuous
T_J	Maximum Junction Temperature	175°C



DIE SIZE: 80 x 48

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.

Open Loop Characteristics V_S = ±15V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS} (Note 1)	Input Offset Voltage	−10	3	10	I	mV
CMRR (Note 3)	Common Mode Rejection Ratio	50	60		I	dB
PSRR (Note 4)	Power Supply Rejection Ratio	65	75		I	dB
$+I_N$	Non-Inverting Input Current	−15	5	15	I	µA
$+R_{IN}$	Non-Inverting Input Resistance	1	5		I	MΩ
+IPSR (Note 4)	Non-Inverting Input Current Power Supply Rejection		0.05	0.5	I	µA/V
$-I_N$ (Note 1)	− Input Current	−40	10	40	I	µA
−ICMR (Note 3)	−Input Current Common Mode Rejection		0.5	2.0	I	µA/V
−IPSR (Note 4)	−Input Current Power Supply Rejection		0.05	0.5	I	µA/V
R_{OL}	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$) R_L = 4000Ω, V_{OUT} = ±10V	300	1000		I	V/mA

EL2020D Die
50 MHz Current Feedback Amplifier

Open Loop Characteristics $V_S = \pm 15V, T_A = 25°C$ — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
A_{VOL1}	Open Loop DC Voltage Gain $R_L = 400\Omega, V_{OUT} = \pm 10V$	70	80		I	dB
A_{VOL2}	Open Loop DC Voltage Gain $R_L = 100\Omega, V_{OUT} = \pm 2.5V$	60	70		I	dB
V_O	Output Voltage $R_L = 400\Omega$	±12	±13		I	V
I_{OUT}	Output Current $R_L = 400\Omega$	±30	±32.5		I	mA
I_S	Quiescent Supply Current		9	12	I	mA
$I_{S\ OFF}$	Supply Current, Disabled, $V_8 = 0V$		5.5	7.5	I	mA
I_{LOGIC}	Pin 8 Current to Disable		1.1	1.5	I	mA
I_D	Min Pin 8 Current to Disable		120	250	I	µA
I_E	Max Pin 8 Current to Disable			30	I	µA

Note 1: The offset voltage and inverting input current can be adjusted with an external 10 kΩ pot between the Balance pins with the wiper connected to V_{CC} to make the output offset voltage zero.

Note 2: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 3: $V_{CM} = \pm 10V$.

Note 4: $\pm 4.5V \leq V_S \leq \pm 18V$.

EL2028D Die

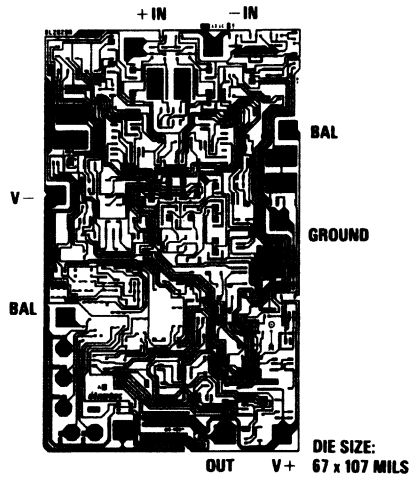
Wideband, Fast Settling, Unity Gain Stable Op-Amp

Absolute Maximum Ratings (T_A = 25°C)

	Voltage between V+ and V−	35V
	Voltage at GND Pin	V+ to V−
	Voltage between −IN or +IN Pins	26V
	Voltage at −IN or +IN Pins	V+ to V−
	Output Current	50 mA (Peak)
		30 mA (Continuous)
	Current into +IN, −IN GND, or Balance Pins	5 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.25	2	I	mV
I_B	Bias Current		250	500	I	nA
I_{OS}	Offset Current		120	250	I	nA
V_{CM}	Common Mode Range		±11	±12	I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	45	80		I	V/mV
CMRR	Common-Mode Rejection Ratio (Note 2)	80	95		I	dB
V_O	Output Voltage Swing		±11	±12	I	V
I_O	Output Current (Note 4)	±25	±50	±75	I	mA
I_S	Supply Current		14	17	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	80	95		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +11V and V_{CM} = 0V to −11V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from 5V to 15V.
Note 4: The inputs are overdriven by ±15V and the output R_L = 100Ω.

EL2029D Die

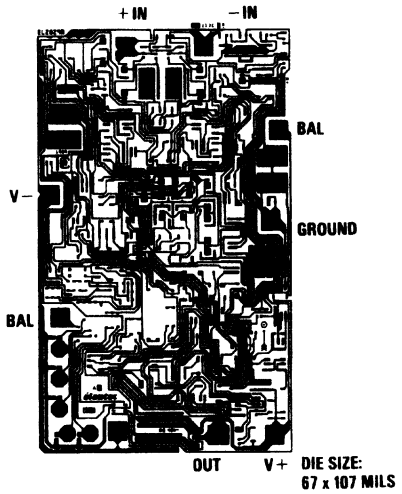
Fast Settling Precision Decompensated Op-Amp

Absolute Maximum Ratings (T_A = 25°C)

	Voltage between V+ and V−	35V
	Voltage at GND Pin	V+ to V−
	Voltage between −IN or +IN Pins	10V
	Voltage at −IN or +IN Pins	V+ to V−
	Output Current	50 mA (Peak)
		30 mA (Continuous)
	Current into +IN, −IN GND, or Balance Pins	5 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.15	0.5	I	mV
I_B	Bias Current		250	500	I	nA
I_{OS}	Offset Current		120	250	I	nA
V_{CM}	Common Mode Range		±11	±12	I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	60	140		I	V/mV
CMRR	Common-Mode Rejection Ratio (Note 2)	80	95		I	dB
V_O	Output Voltage Swing	±11	±12		I	V
I_O	Output Current (Note 4)	±25	±50	±75	I	mA
I_S	Supply Current		14	17	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	80	95		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed with V_{CM} = 0V to −11V and V_{CM} = 0V to +11V.
Note 3: Two tests are performed with V+ = +15V, V− changed from −5V to −15V. V− = −15V, V+ changed from 5V to 15V.
Note 4: The inputs are overdriven by ±5V and the output R1 = 100Ω.

EL2030D Die

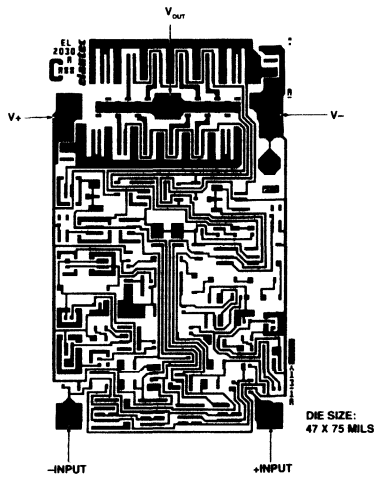
120 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V
V_{IN}	Input Voltage	±15V or V_S
ΔV_{IN}	Differential Input Voltage	±6V
I_{IN}	Input Current (Pins 2 or 3)	±10 mA
I_{NS}	Input Current (Pins 1, 5, or 8)	±10 mA
I_{OP}	Peak Output Current	Short Circuit Protected
	Ouput Short Circuit Duration	Continuous
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



Open Loop Characteristics V_S = 15V, T_A = 25°C, R_L = 200Ω, unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V V_S = ±5V		10 5	20 10	I I	mV mV
CMRR (Note 1)	Common Mode Rejection Ratio		50	60		I	dB
PSRR (Note 2)	Power Supply Rejection Ratio		60	70		I	dB
$+I_N$	Non-Inverting Input Current	V_S = ±5V, ±15V		5	15	I	µA
$+R_{IN}$	Non-Inverting Input Resistance		1.1	2		I	MΩ
+IPSR (Note 2)	Non-Inverting Input Current Power Supply Rejection			0.1	0.5	I	µA/V
$-I_N$	−Input Current	V_S = ±5V, ±15V		10	40	I	µA
−ICMR (Note 2)	−Input Current Common Mode Rejection			0.1	0.5	I	µA/V
−IPSR (Note 2)	−Input Current Power Supply Rejection			0.5	5	I	µA/V
R_{OL} (Note 3)	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$) (Note 3)	V_S = ±15V, V_{OUT} = ±10V	88	150		I	V/mA
		V_S = ±5V, V_{OUT} = ±2.5V	75			I	V/mA

EL2030D Die
120 MHz Current Feedback Amplifier

Open Loop Characteristics $V_S = \pm 15V, T_A = 25°C$ — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
A_{VO1}	Open Loop DC Voltage Gain	$V_S = \pm 15V$	60	70		I	dB
A_{VO2}	Open Loop DC Voltage Gain (Note 3)	$V_S = \pm 5V$	56	65		I	dB
V_O	Output Voltage	$V_S = \pm 15V$	±12	±13		I	V
	(Note 3)	$V_S = \pm 5V$	±3	±3.5		I	V
I_{OUT}	Output Current	$V_S = \pm 15V$	±60	±65		I	mA
		$V_S = \pm 5V$	±30	±35		I	mA
I_S	Quiescent Supply Current			15	21	I	mA

Note 1: V_{CM} = 10V for $V_S = \pm 15V$. For $V_S = \pm 5V$, $V_{CM} = \pm 2.5V$.
Note 2: V_{OS} is measured at $V_S = \pm 4.5V$ and at $V_S = \pm 18V$. Both supplies are changed simultaneously.
Note 3: $R_L = 100\Omega$.

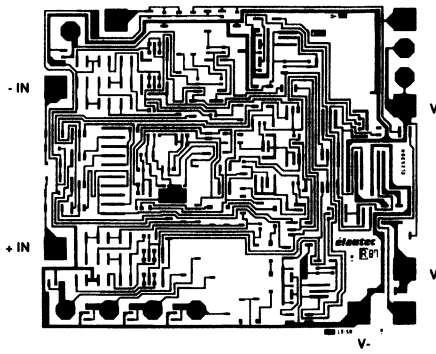
EL2038D Die
1 GHz Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	30 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



Die Size:
71 x 82 MILS

DC Electrical Characteristics V_S = ±15V, R_L = 1kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	2	I	mV
I_B	Bias Current		5	15	I	μA
I_{OS}	Offset Current		1	4	I	μA
V_{CM}	Common Mode Range	±11	±12		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	10k	15k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	60			I	dB
V_O	Output Voltage Swing	±11			I	V
I_O	Output Current (Note 4)	±25			I	mA
I_S	Supply Current		13	17	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	60	85		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 3: Two test are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 4: R_L = 200Ω.

EL2041D Die

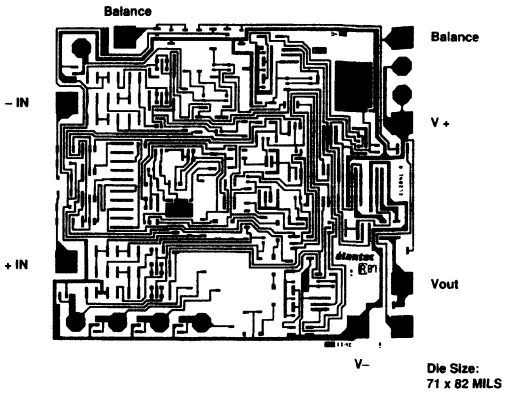
Wideband, Fast Settling, Unity Gain Stable, Operational Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	2	I	mV
I_B	Bias Current		5	15	I	μA
I_{OS}	Offset Current		1	4	I	μA
V_{CM}	Common Mode Range	±8			I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	7k	10k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	70	80		I	dB
V_O	Output Voltage Swing	±11			I	V
I_O	Output Current (Note 4)	±25	±50		I	mA
I_S	Supply Current		13	17	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	70	80		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +8V and V_{CM} = 0V to −8V.
Note 3: Two tests are perforfmed. V+ = +15V, and V− is changed from −7V to −15V. V− = −15V, and V+ is changed from +7V to +15V.
Note 4: R_L = 200Ω.

EL2223D Die

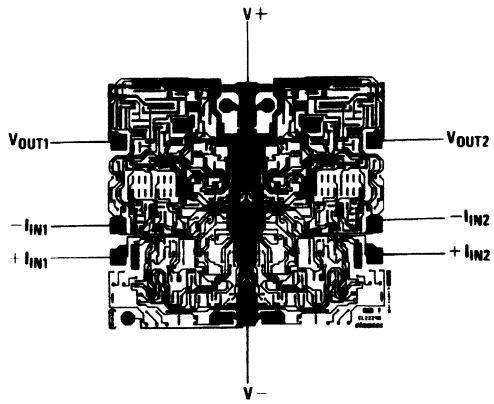
Dual, 500 MHz, High Speed Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 2 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	5	I	mV
I_B	Bias Current		1.5	4	I	µA
I_{OS}	Offset Current		0.2	2	I	µA
V_{CM}	Common Mode Range	±10	±12		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	20k	40k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	70	90		I	dB
V_O	Output Voltage Swing	±11	±12.5		I	V
I_O	Output Current		±50	±70	I	mA
I_S	Supply Current		9.5	13	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	70	90		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.

EL2224D Die

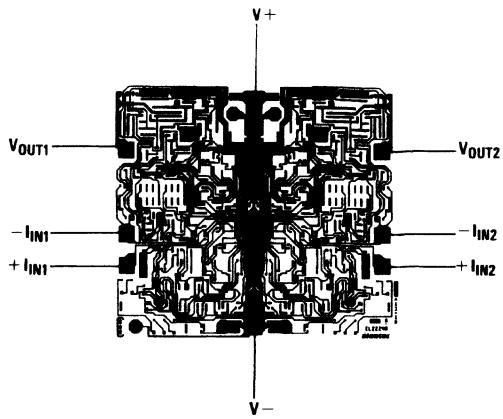
Dual, 60 MHz, Unity Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 2 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	5	I	mV
I_B	Bias Current		1.5	4	I	µA
I_{OS}	Offset Current		0.2	2.0	I	µA
V_{CM}	Common Mode Range	±10	±12		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	4k	6k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	70	80		I	dB
V_O	Output Voltage Swing	±11	±12.5		I	V
I_O	Output Current		±50	±70	I	mA
I_S	Supply Current		9.5	13	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	60	75		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.

EL2232D Die

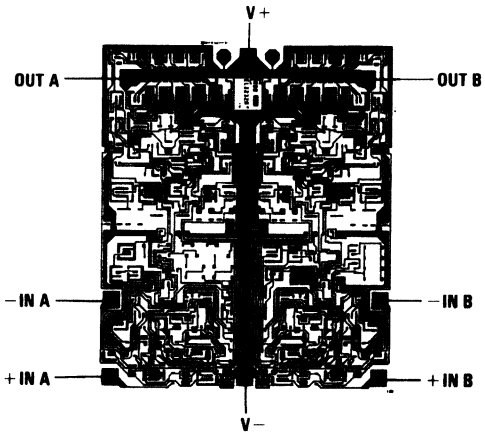
Dual 60 MHz Current Feedback Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or +36V
V_{IN}	Input Voltage	±15V or V_S
ΔV_{IN}	Differential Input Voltage	±6V
I_{IN}	Input Current (Pins 2 or 3)	±10 mA
I_{OP}	Peak Output Current	Short Circuit Protected
	Output Short Circuit Duration (Note 1)	Continuous
T_A	Operating Temperature Range	−55°C to 125°C
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 86 x 100 MILS

Open Loop Characteristics V_S = ±15V, T_A = 25°C, R_L = 500Ω, unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V		2	7	I	mV
$+I_N$	+Input Current	V_S = ±5V, ±15V		1.2	3	I	µA
$-I_N$	−Input Current	V_S = ±5V, ±15V		5	20	I	µA
$+R_{IN}$	+Input Resistance		2	20		I	MΩ
CMRR (Note 2)	Common Mode Rejection Ratio	V_S = ±5V, ±15V	56	63		I	dB
−ICMR (Note 2)	−Input Common Mode Rejection			0.25	0.75	I	µA/V
PSRR (Note 3)	Power Supply Rejection Ratio		66	80		I	dB
+IPSR (Note 3)	+Input Current Power Supply Rejection			0.03	0.06	I	µA/V
−IPSR (Note 2)	−Input Current Power Supply Rejection			0.06	0.2	I	µA/V
R_{OL} (Note 4)	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$)	V_S = ±5V, ±15V	1.2	4		I	MΩ
V_O	Output Voltage Swing	V_S = ±15V	11.5	12.5		I	V
		V_S = ±5V	2	2.5		I	V
I_{OUT}	Output Current	V_S = 15V	23	30		I	mA
I_S	Quiescent Supply Current			9.5	13	I	mA

Note 1: Junction temperature must be below absolute maximum rating when an output is shorted.
Note 2: V_{CM} = ±10V for V_S = ±15V. For V_S = ±5V, V_{CM} = ±2V.
Note 3: V_{OS} is measured at V_S = ±4.5V and at V_S = ±18V. Both supplies are changed simultaneously.
Note 4: V_{OUT} = ±10V for V_S = ±15V, V_{OUT} = ±2V for V_S = ±5V, R_L = 500Ω.

EL2242D Die

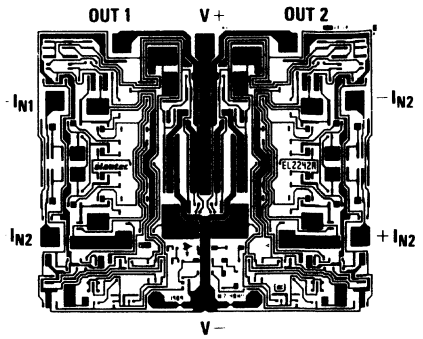
Dual Fast Single-Supply Unity Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	36V
	Input Voltage	V+ to V−
	Input Current	5 mA
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	30 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 86 x 72 MILS

DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_A = 25°C, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		2	5	I	mV
I_B	Bias Current		0.5	0.7	I	µA
I_{OS}	Offset Current		0.01	0.1	I	µA
V_{CM}+	Positive Common Mode Range	±12	13.3		I	V
V_{CM}−	Negative Common Mode Range	−15	−15.3		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	150	300		I	V/mV
CMRR	Common-Mode Rejection Ratio (Note 2)	80			I	dB
V_O	Output Voltage Swing (Note 4)	±12	±13.5		I	V
		±14.98	±15		I	V
I_O	Output Current (Note 5)	±25	±50		I	mA
I_S	Supply Current (Both Amplifiers)		8.2	10	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	76	95		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +12V and V_{CM} = 0V to −12V.
Note 3: Two tests are performed. V+ = +3V, and V− is changed from −2V to −27V. V− = −2V, and V+ is changed from +3V to +28V.
Note 4: R_L is connected to V−.
Note 5: The inputs are over driven by ±15V; R_L = 100Ω.

EL2243D Die

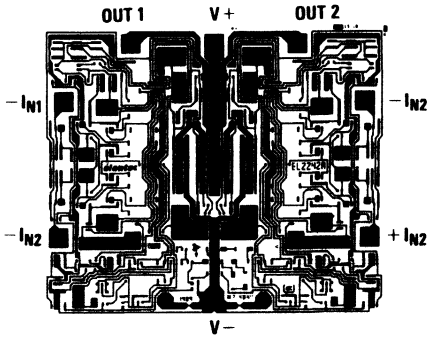
Dual Fast Single-Supply Decompensated Op-Amp

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V
Voltage between −IN or +IN Pins	36V
Voltage at −IN or +IN Pins	V+ to V−
Output Current	50 mA (Peak)
	30 mA (Continuous)
Current into +IN, −IN	5 mA

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 86 x 72 MILS

DC Electrical Characteristics V_S = ±15, R_L = 1 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		1.5	5	I	mV
I_B	Bias Current		0.5	0.7	I	µA
I_{OS}	Offset Current		0.01	0.1	I	µA
V_{CM}+	Common Mode Range	12	13.3		I	V
V_{CM}−	Common Mode Range	−15	−15.3		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	250	500		I	V/mV
CMRR	Common-Mode Rejection Ratio (Note 2)	80	100		I	dB
V_O	Output Voltage Swing R_L tied to V−	±12	±13.5		I	V
		−14.98	−15		I	V
I_O	Output Current (Note 4)	±15	±25	±50	I	mA
I_S	Supply Current		8.2	10	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	80	100		I	dB

Note 1: V_O = ±10V.

Note 2: Two tests are performed with V_{CM} = 0V to −12V and V_{CM} = 0V to 12V.

Note 3: Two tests are performed with V+ = +3V, V− is changed from −2V to −27V. V− = −2V, V+ is changed from 3V to 28V.

Note 4: The inputs are overdriven by ±15V and the output R1 = 100Ω.

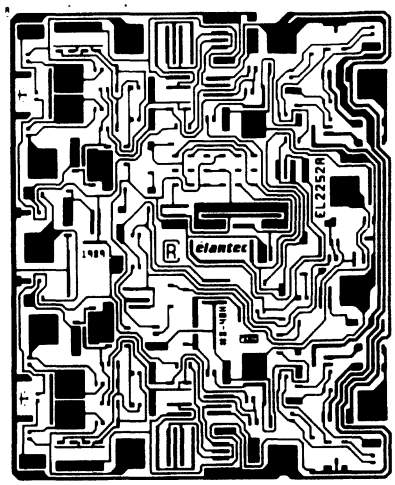
EL2252D Die
Dual 50 MHz Comparator/Pin Receiver

Absolute Maximum Ratings (T_A = 25°C)

	Voltage between V+ and V−	36V
	Voltage at V+	18V
	Voltage between −IN and +IN Pins	36V
	Output Current	12 mA
	Current into +IN, −IN, HYS, or /TTL	5 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 65 x 77 MILS

DC Electrical Characteristics V_S = ±15V; HYS and i/m TTL grounded; T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		1	6	I	mV
I_B	Input Bias Current V_{CM} = 0V, pin 2 or 3		6	12	I	µA
I_{OS}	Input Offset Current V_{CM} = 0V		0.2	1	I	µA
CMRR	Common-Mode Rejection Ratio (Note 1)	70	95		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	70	90		I	dB
V_{CM}+	Common Mode Input Range	10	13		I	V
V_{CM}−		−9	−12		I	V
A_{VOL}	Large Signal Voltage Gain (V_{OUT} = 0.8V + 0.20V)	4,000	8,000		I	V/V
V_{OL}	Output Voltage Logic Low I_{OL} = 0 MA	−0.2	0.2	0.4	I	V
	I_{OL} = 5 MA	−0.2	0.4	0.8	I	V
V_{OH}	Output Voltage Logic High CMOS Mode	4	4.6	5.1	I	V
	TTL Mode	2.4	2.7	3.2	I	V
I_S+	Positive Supply Current		16	19	I	mA
I_S−	Negative Supply Current		17	20	I	mA

Note 1: Two tests are performed with V_{CM} = 0V to −9V and V_{CM} = 0V to 10V.
Note 2: Two tests are performed with V+ = +15V, V− changed from −10V to −15V; V− = −15V, V+ changed from 10V to 15V.

EL2423D Die

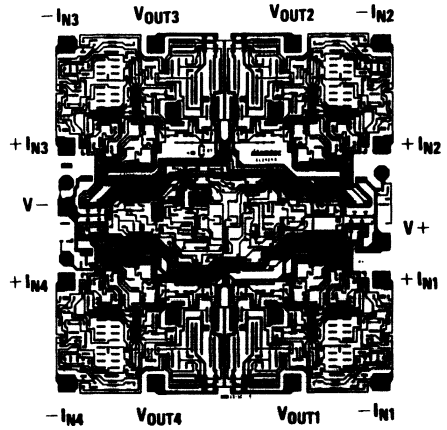
Quad De-compensated, High Speed Operational Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 101 x 95 MILS

DC Electrical Characteristics V_S = ±15V, R_L = 2 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		1.0	6	I	mV
I_B	Bias Current		1.0	4	I	μA
I_{OS}	Offset Current		0.5	2	I	μA
V_{CM}	Common Mode Range	±10	±11		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	7k	10k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	70	80		I	dB
V_O	Output Voltage Swing	±11	±12		I	V
I_O	Output Current	±25	±50	±85	I	mA
I_S	Supply Current		16	18	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	70	80		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.

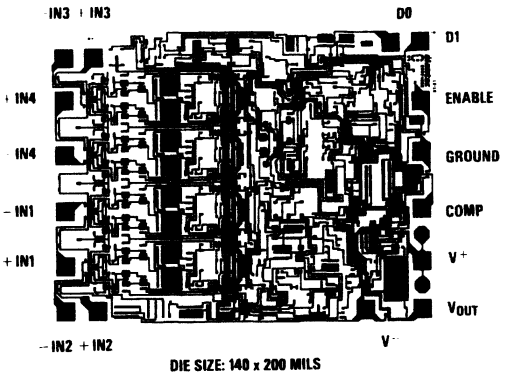
EHA0-2400-6 Die
4 Channel Programmable Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	45V
Differential Input Voltage	±V Supply
Output Current	Short Circuited Protected
T_A Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 140 x 200 MILS

DC Electrical Characteristics

V_S = ±15V, R_L = 2 kΩ. V_{IL} = 0.5V, V_{IH} = ±2.4V, limits apply to each of the four channels, when addressed, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		4	9	I	mV
I_B	Bias Current (Note 1)		50	200	I	nA
I_{OS}	Offset Current (Note 1)		5	50	I	nA
V_{CM}	Common Mode Range	±9			I	V
A_V	Large Signal Voltage Gain (Note 2)	50k	150k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	80	100		I	dB
V_O	Output Voltage Swing	±10	±12		I	V
I_O	Output Current (Note 4)	±10	±20		I	mA
I_S	Supply Current		4.8	6	I	mA
PSRR	Power Supply Rejection Ratio (Note 5)	74	90		I	dB

Channel Select Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
I_{INL}	Digital Input Current	V_{IN} = 0V		0.1	1.5	I	mA
CT	Crosstalk (Note 6)		−80	−110		I	dB

Note 1: Unselected channels have approximately the same input parameters.
Note 2: V_{OUT} = ±10V.
Note 3: Two tests are performed. V_{CM} = 0V to +5V and V_{CM} = 0V to −5V.
Note 4: A_V = +1, C_{comp} = 15 pF, R_L = 2 kΩ, C_L = 50 pF.
Note 5: Two tests are performed. V+ = +15V, and V− is changed from −10V to −20V. V− = −15V, and V+ is changed from +10V to +20V.
Note 6: Unselected input to output, V_{IN} = ±10V.

EHA0-2500-6 Die

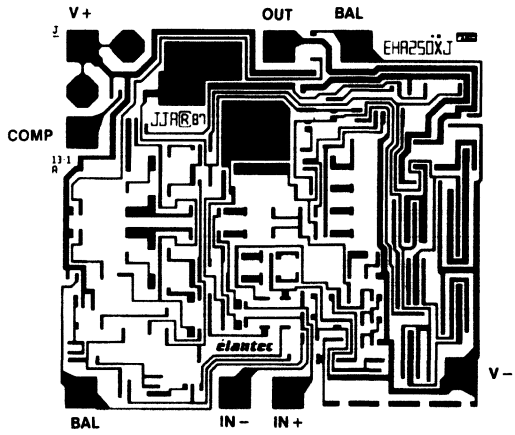
High Slew Rate Operational Amplifier Die

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±20V
V_{IN}	Differential Input Voltage	±15V
I_{OUT}	Peak Output Current	5 mA
T_J	Maximum Junction Temperature	175°C
T_A	Operating Temperature Range	−55° to +125°C
T_{SR}	Storage Temperature	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 66 x 61 MILS

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage			2	5	I	mV
I_B	Bias Current			100	200	I	nA
I_{OS}	Offset Current			10	25	I	nA
V_{CMR}	Common Mode Rate		±10			I	V
CMRR	Common Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	90		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	dB
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_{OUT} = ±10V	20	30		I	V/mV
V_{OUT}	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	V
I_{OUT}	Output Current	V_{OUT} = ±10V	±10	±20		I	mA
I_{CC}	Supply Current (Note 5)			4	6	I	mA

Note 1: Both input currents I_{B+} and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: For PSRR+, V_{S+} = +10V to +20V with V_{S-} = −15V.
For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL}+, V_{OUT} = 0V to +10V and for A_{VOL}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply current, I_{CC+} and I_{CC-}, are tested.

EHA0-2510-6 Die

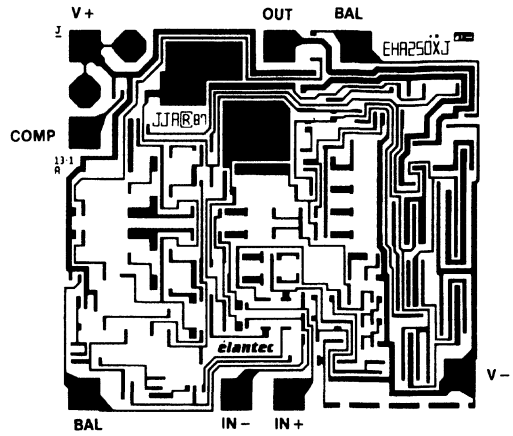
High Slew Rate Operational Amplifier Die

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±20V
V_{IN}	Differential Input Voltage	±15V
I_{OUT}	Peak Output Current	5 mA
T_J	Maximum Junction Temperature	175°C
T_A	Operating Temperature Range	−55° to +125°C
T_{SR}	Storage Temperature	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 66 x 61 MILS

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage			4	8	I	mV
I_B	Bias Current			100	200	I	nA
I_{OS}	Offset Current			25	25	I	nA
V_{CMR}	Common Mode Rate		±10			I	V
CMRR	Common Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	90		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	dB
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_{OUT} = ±10V	15	25		I	V/mV
V_{OUT}	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	V
I_{OUT}	Output Current	V_{OUT} = ±10V	±10	±20		I	mA
I_{CC}	Supply Current (Note 5)			4	6	I	mA

Note 1: Both input currents I_{B+} and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: For PSRR+, V_{S+}, = +10V to +20V with V_{S-} = −15V.
For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL}+, V_{OUT} = 0V to +10V and for A_{VOL}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply current, I_{CC+} and I_{CC-}, are tested.

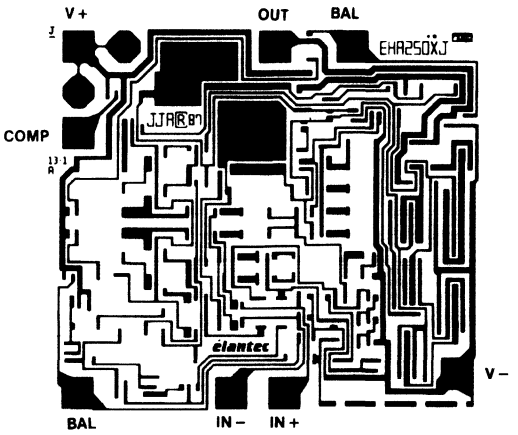
EHA0-2520-6 Die
High Slew Rate Operational Amplifier Die

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±20V
V_{IN}	Differential Input Voltage	±15V
I_{OUT}	Peak Output Current	5 mA
T_J	Maximum Junction Temperature	175°C
T_A	Operating Temperature Range	−55° to +125°C
T_{SR}	Storage Temperature	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 66 x 61 MILS

DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{OUT} = 0V, T_A = 25°C

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage			4	8	I	mV
I_B	Bias Current			100	200	I	nA
I_{OS}	Offset Current			25	25	I	nA
V_{CMR}	Common Mode Rate		±10			I	V
CMRR	Common Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	90		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	dB
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_{OUT} = ±10V	15	25		I	mV
V_{OUT}	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	V
I_{OUT}	Output Current	V_{OUT} = ±10V	±10	±20		I	mA
I_{CC}	Supply Current (Note 5)			4	6	I	mA

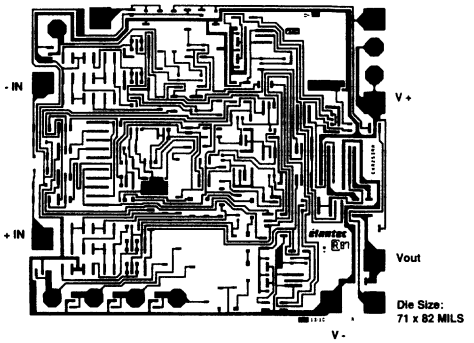
Note 1: Both input currents I_{B+} and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: For PSRR+, V_{S+}, = +10V to +20V with V_{S-} = −15V.
For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL}+, V_{OUT} = 0V to +10V and for A_{VOL}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply current, I_{CC+} and I_{CC-}, are tested.

EHA0-2539-6 Die

Very High Slew Rate Wideband Operational Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
T_J	Maximum Junction Temperature	175°C



Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.

DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	10	I	mV
I_B	Bias Current		5	20	I	μA
I_{OS}	Offset Current		1	6	I	μA
V_{CM}	Common Mode Range	±10	±12		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	10k	15k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	60			I	dB
V_O	Output Voltage Swing	±10			I	V
I_O	Output Current	±10			I	mA
I_S	Supply Current		13	23	I	mA
PSRR	Power Supply Rejection Ratio	60			I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.

EHA0-2540-6 Die

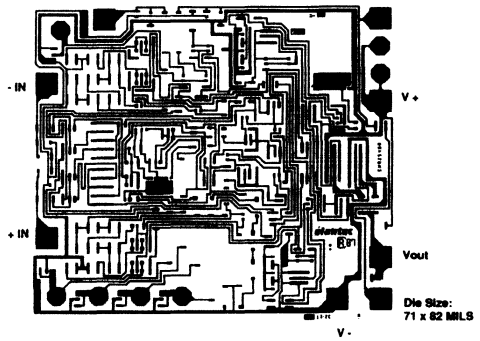
Very High Slew Rate Wideband Operational Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_A = 25°C unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	10	I	mV
I_B	Bias Current		5	20	I	μA
I_{OS}	Offset Current		1	6	I	μA
V_{CM}	Common Mode Range	±10			I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	10k	15k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	60			I	dB
V_O	Output Voltage Swing	±10			I	V
I_O	Output Current	±10			I	mA
I_S	Supply Current		13	23	I	mA
PSRR	Power Supply Rejection Ratio	60			I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.

EHA0-2600-6 Die

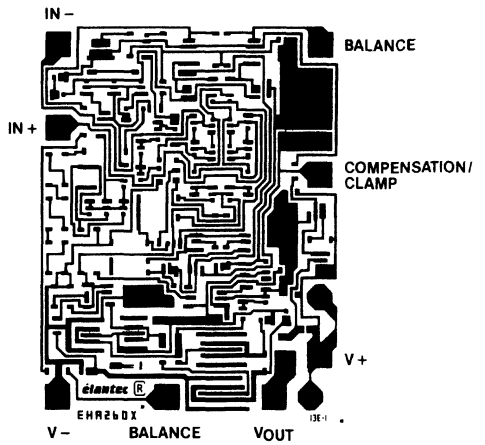
High Slew Rate Operational Amplifier Die

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±22.5V
V_{IN}	Differential Input Voltage	±12.0V
I_{OUT}	Peak Output Current	Short Circuit Protected
T_J	Maximum Junction Temperature	175°C
T_A	Operating Temperature Range	−55°C to +125°C
T_{SR}	Storage Temperature	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 58 x 73 MILS

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage			0.5	4	I	mV
I_B	Bias Current (Note 1)			1	10	I	nA
I_{OS}	Offset Current			1	10	I	nA
V_{CMR}	Common Mode Rate		±11.0			I	V
CMRR	Common Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	100		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	dB
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_{OUT} = ±10V	100	150		I	kV/V
V_{OUT}	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	V
I_{OUT}	Output Current	V_{OUT} = ±10V	±15	±22		I	mA
I_{CC}	Supply Current (Note 5)			3	3.7	I	mA

Note 1: Both input currents I_{B+} and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: For PSRR+, V_{S+}, = +10V to +20V with V_{S-} = −15V.
For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL}+, V_{OUT} = 0V to +10V and for A_{VOL}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply current, I_{CC+} and I_{CC-}, are tested.

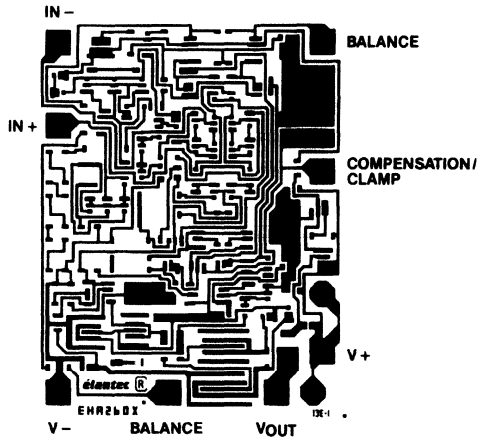
EHA0-2620-6 Die
High Slew Rate Operational Amplifier Die

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±22.5V
V_{IN}	Differential Input Voltage	±12.V
I_{OUT}	Peak Output Current	Short Circuit Protected
T_J	Maximum Junction Temperature	175°C
T_A	Operating Temperature Range	−55°C to +125°C
T_{SR}	Storage Temperature	−65°C to +150°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DIE SIZE: 58 x 73 MILS

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100 kΩ, V_{CM} = 0V, V_{OUT} = 0V, T_A = 25°C

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage			0.5	4	I	mV
I_B	Bias Current			1	15	I	nA
I_{OS}	Offset Current			1	15	I	nA
V_{CMR}	Common Mode Range		±11			I	V
CMRR	Common Mode Rejection Ratio (Note 2)	ΔV_{CM} = ±10V	80	100		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	ΔV_S = ±5V	80	90		I	dB
A_{VOL}	Large Signal Voltage Gain (Note 4)	R_L = 2 kΩ, V_{OUT} = ±10V	100	150		I	kV/V
V_{OUT}	Output Voltage Swing	R_L = 2 kΩ	±10	±12		I	V
I_{OUT}	Output Current	V_{OUT} = ±10V	±15	±18		I	mA
I_{CC}	Supply Current (Note 5)			3	3.7	I	mA

Note 1: Both input currents, I_{B+} and I_{B-}, are tested individually.
Note 2: For CMRR+, V_{CM} = 0V to +10V and for CMRR−, V_{CM} = 0V to −10V.
Note 3: For PSRR+, V_{S+}, = +10V to +20V with V_{S-} = −15V.
For PSRR−, V_{S-} = −10V to −20V with V_{S+} = +15V.
Note 4: For A_{VOL}+, V_{OUT} = 0V to +10V and for A_{VOL}, V_{OUT} = 0V to −10V.
Note 5: Both positive and negative supply current, I_{CC+} and I_{CC-}, are tested.

EHA0-5190-6 Die

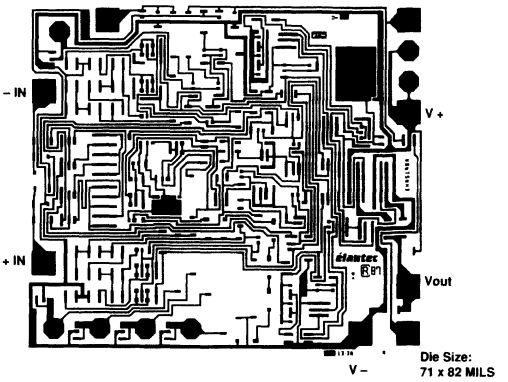
Wideband, Fast Settling Operational Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
ΔV_{IN}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	30 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_L = 200Ω, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		0.5	5	I	mV
I_B	Bias Current		5	15	I	µA
I_{OS}	Offset Current		1	4	I	µA
V_{CM}	Common Mode Range	±5	±10		I	V
A_{VOL}	Large Signal Voltage Gain (Note 1)	15k	30k		I	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	74	90		I	dB
V_O	Output Voltage Swing	±5	±8		I	V
I_O	Output Current (Note 4)	±25	±40		I	mA
I_S	Supply Current		13	28	I	mA
PSRR	Power Supply Rejection Ratio (Note 3)	70	80		I	dB

Note 1: V_O = ±10V.
Note 2: Two tests are performed. V_{CM} = 0V to +5V and V_{CM} = 0V to −5V.
Note 3: Two tests are performed. V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 4: R_L = 200Ω, $C_L \leq$ 10 pF, V_O = ±5V.

Elantec Applications Articles

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Applications Articles

The following is a list of informative applications articles written by Elantec engineers, as well as editors from the major electronics publications. Reprints are available, consult factory.

HDTV Differential Phase and Gain Test Methodology	James Argenal, Elantec—Dec. 1989
Alternative to Laser Trim: Zapping Zenners, Blowing Fuse Links	Caleb Brown Electronics Test—Sept. 1989
Build a Circuit Board Tester with Your PC	Barry Harvey, Elantec Electronic Design—Feb. 9, 1989
Current-feedback Amplifiers Benefit High-speed Designs	Sergio Franco, San Francisco State Univ. EDN—Jan. 5, 1989
Current-mode Speed Video Amps	Electronic Design—July 27, 1989
Current Feedback Op Amps Raise Gain-bandwidth Product	Jon Dutra Electronic Design—July 14, 1989
Current-feedback Op Amps Ease High-speed Circuit Design	Peter Harold, European Editor EDN—July 7, 1989
Delta Modulators Simplify A/D Conversion	Barry Harvey, Elantec EDN—June 22, 1989
Simple Techniques Help You Conquer Op Amp Instability	Barry Siegel, Elantec EDN—March 31, 1989
Precision Comparators Ease Oscillator and Data-converter Design	Jon Dutra, Barry Harvey EDN—Feb. 18, 1989
Special Circuit Simplifies Testing of Voltage Comparators	Barry Harvey, Elantec EDN—Oct. 15, 1987
Take the Guesswork Out of Settling-time Measurements	Barry Harvey, Elantec EDN—Sept. 19, 1985

Ordering Information

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Ordering Information

In North America, Elantec has three levels of sales support. Regional Sales Managers are located in the Boston, Dallas and San Francisco areas. Field Applications Engineers are located in the Boston and Milpitas offices. Elantec also maintains a network of sales representatives covering the United States and Canada. Finally, major nationwide and regional distributors provide local stock. Elantec maintains an up-to-date distributor inventory status and provides an inventory referral service through Distribution Sales in Milpitas. Orders may be placed through the sales representatives or distributors. If a list of sales representatives and distributors was not included with this Elantec 1990 Databook, please contact any of the regional sales offices.

In Europe, Elantec has a Regional Sales Office in London. Local sales support is provided through stocking representatives in all of the major countries and by stocking distributors in France, West Germany and the U.K. A list of representatives and distributors may be obtained from the London office.

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Elantec Proprietary and NSC Alternate Source

E L 2006 A G /883B

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FAMILY
- LH NSC Alternate Source
- L Proprietary Linear
- DH NSC Alternate Source
- P PNP Array
- N NPN Array
- SCD DIE

PART NUMBER

OPTIONAL SUFFIX
- A Selected Electrical Performance
- C −25°C to +85°C
- None −55°C to +125°C

PACKAGE
- D Dice
- G TO-8 Metal Can
- H TO-5 or TO-99 Metal Can
- J CerDIP
- K TO-3
- L Leadless Chip Carrier
- N Plastic DIP
- PL Plastic Leaded Chip Carrier
- T TO-220
- M SOIC

RELIABILITY PROGRAM
/883B 100% MIL-STD-883 Class B, Revision C Processing

Harris Semiconductor Alternate Source

EHA 2 2520 /883B

FAMILY PREFIX
- E ELANTEC
- H HARRIS
- A ANALOG

PACKAGE
- 1 14-Pin Ceramic DIP
- 2 TO-99 Metal Can
- 3 Plastic DIP
- 4 Leadless Chip Carriers
- 7 8-Pin CerDIP
- 0 Dice

PART NUMBER

QUALITY ASSURANCE LEVEL
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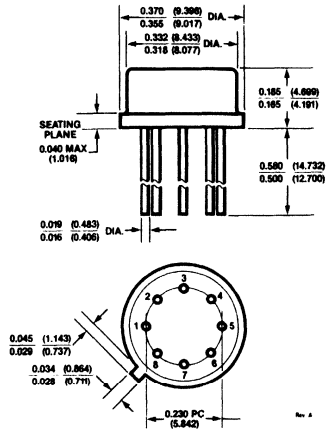
- 2 −55°C to +125°C
- 4 −25°C to +85°C
- 5 0°C to +75°C
- 6 100% 25°C Probe Tested (Dice Only)
- /883B Processing per "Elantec's Military Processing—Monolithic Integrated Circuits"
- 9 −40°C to +85°C

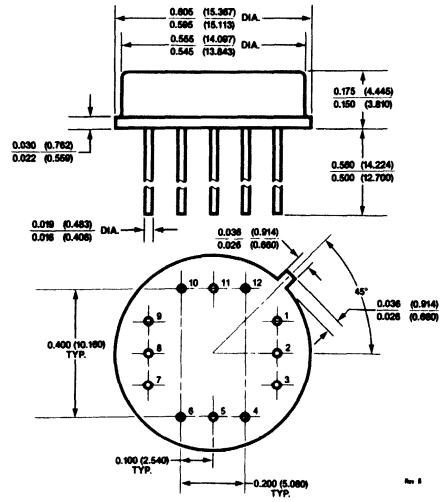
Package Outlines

élantec

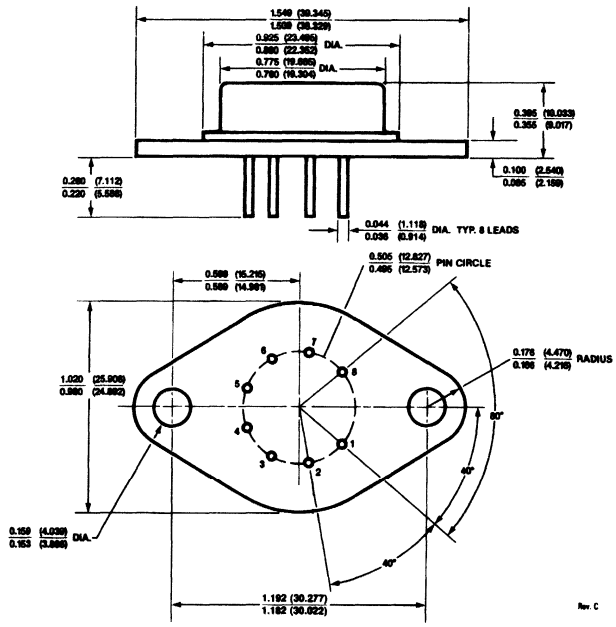
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS



MDP0001 Rev. A
8-Lead TO-5 Metal Can Package
Lead Finish (Coml)—Tin Plate
Lead Finish (Mil)—Gold or Hot Solder DIP

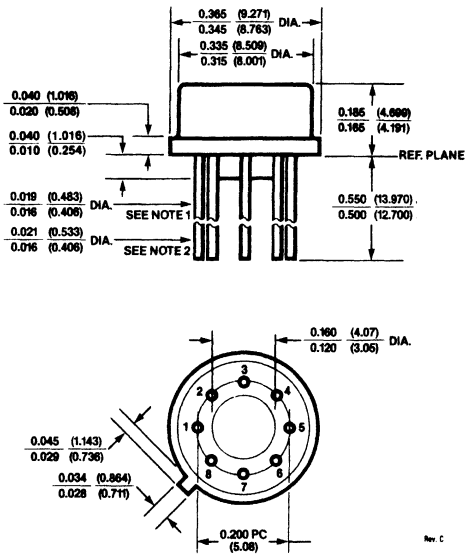


MDP0002 Rev. B
12-Lead TO-8 Metal Can Package
Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Gold or Hot Solder DIP



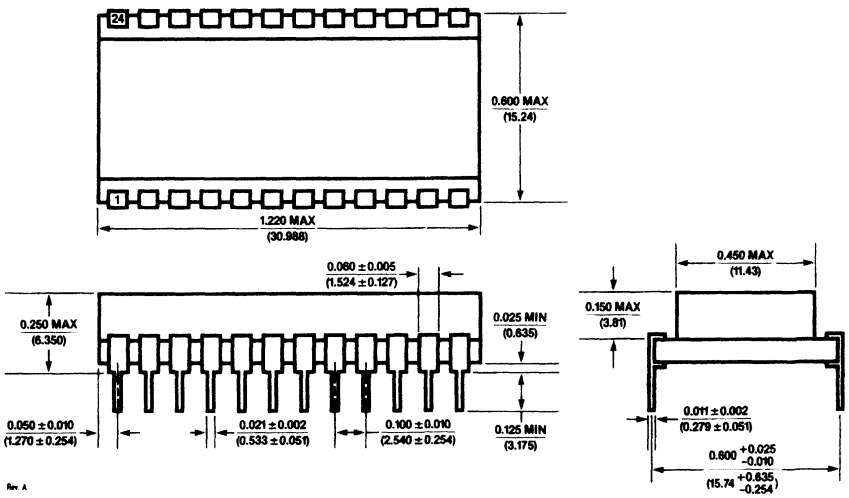
MDP0003 Rev. C
8-Lead TO-3 Metal Can Package
Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

Package Outlines

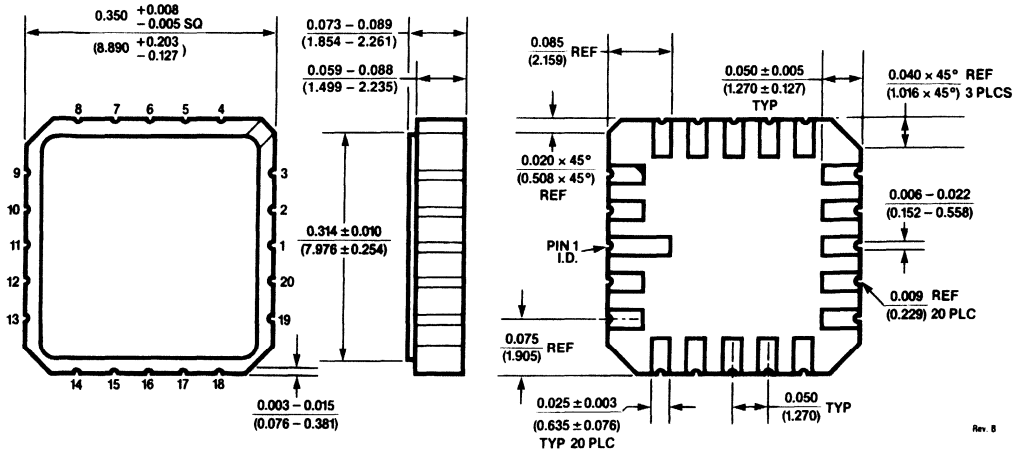


Note 1: Tolerance applies between the seating plane and 0.250 from the reference plane.
Note 2: Tolerance applies between 0.250 and 0.500 from the reference plane.

MDP0004 Rev. C
8-Lead TO-99 Metal Can Package
Lead Finish (Coml)—Tin Plate
Lead Finish (Mil)—Gold or Hot Solder DIP



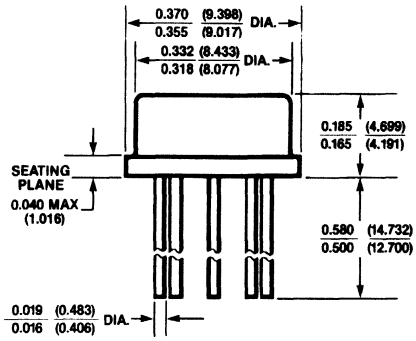
MDP0005 Rev. A
24-Lead Ceramic Substrate
Lead Finish—Hot Solder DIP

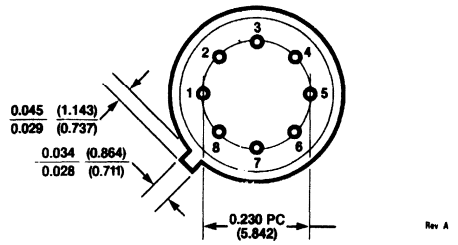


MDP0007 Rev. B

20-Lead Chip Carrier

Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP



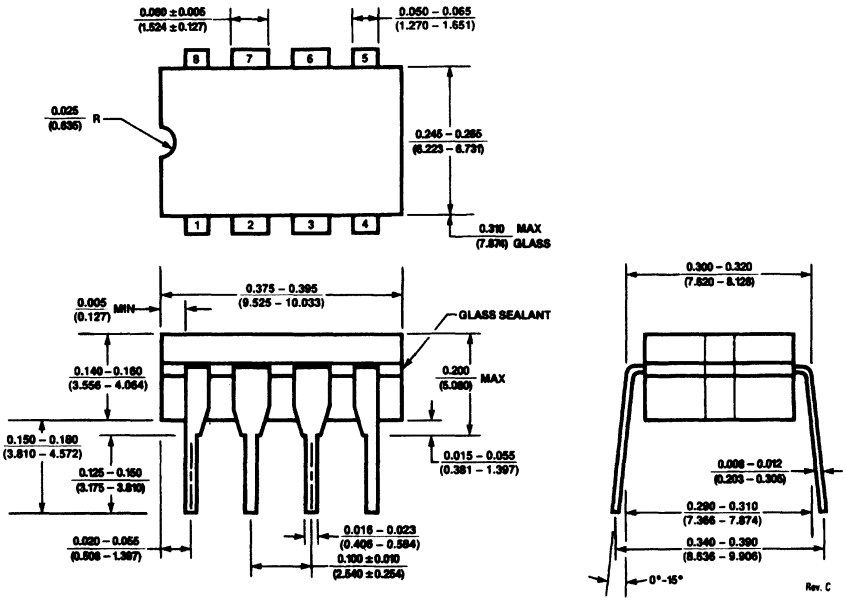


MDP0009 Rev. A

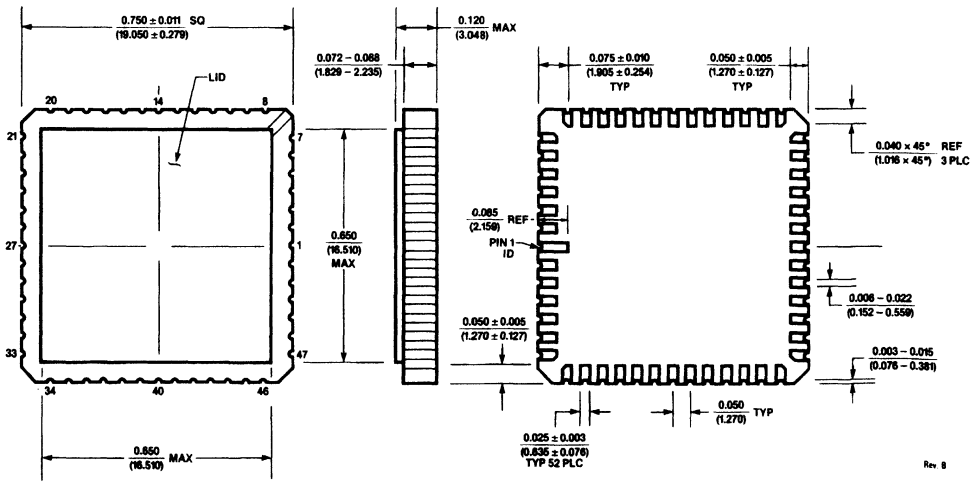
10-Lead TO-5 Metal Can Package

Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Gold or Hot Solder DIP

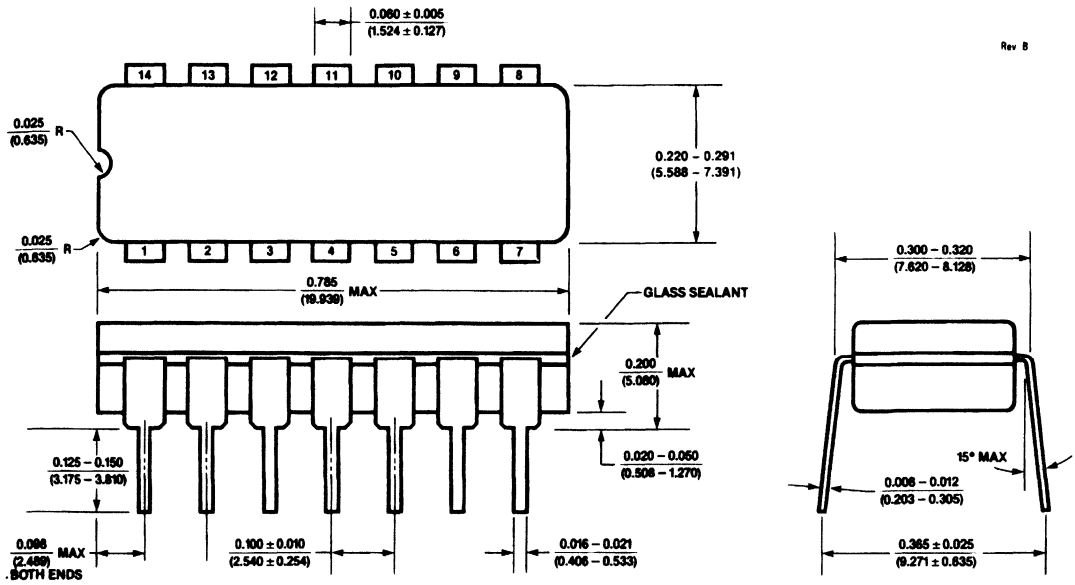
Package Outlines



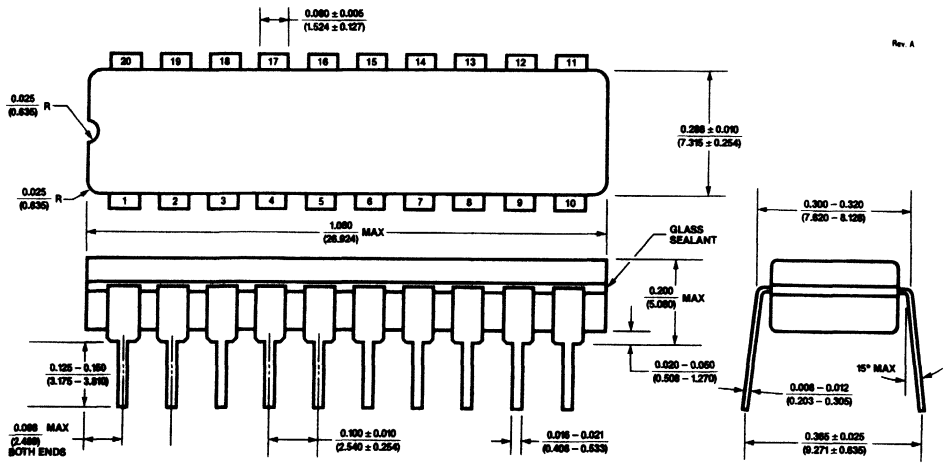
MDP0010 Rev. C
8-Lead CerDIP
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP



MDP0013 Rev. B
52-Lead Ceramic Chip Carrier
Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

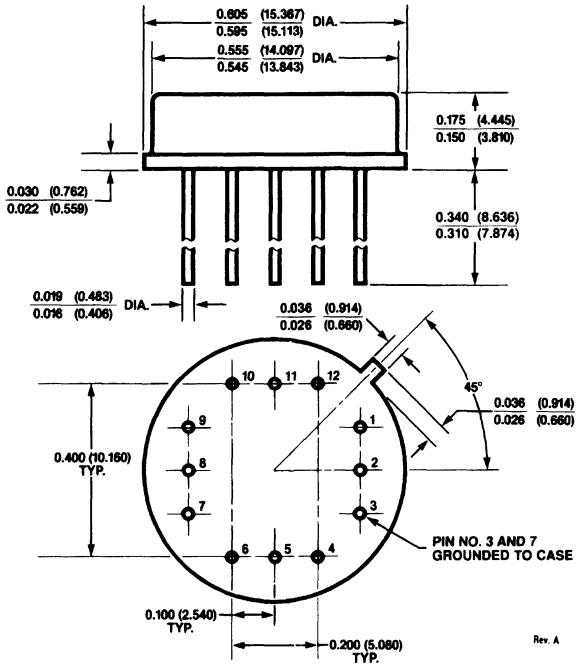


MDP0014 Rev. B
14-Lead CerDIP
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP



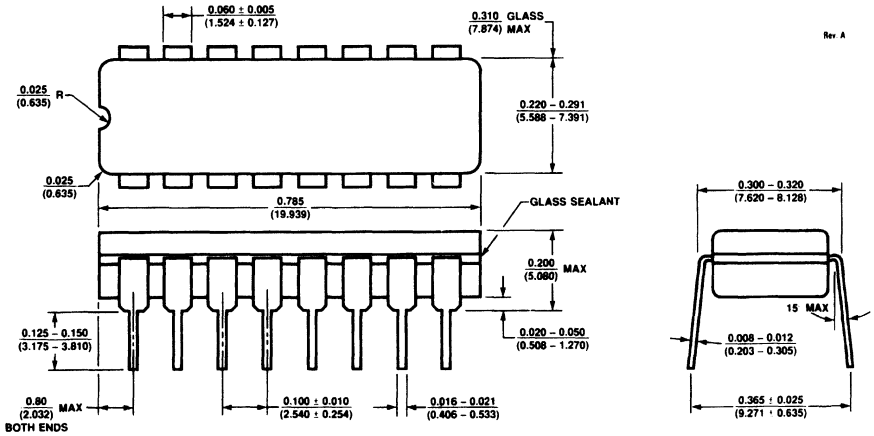
MDP0016 Rev. A
20-Lead CerDIP
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

Package Outlines



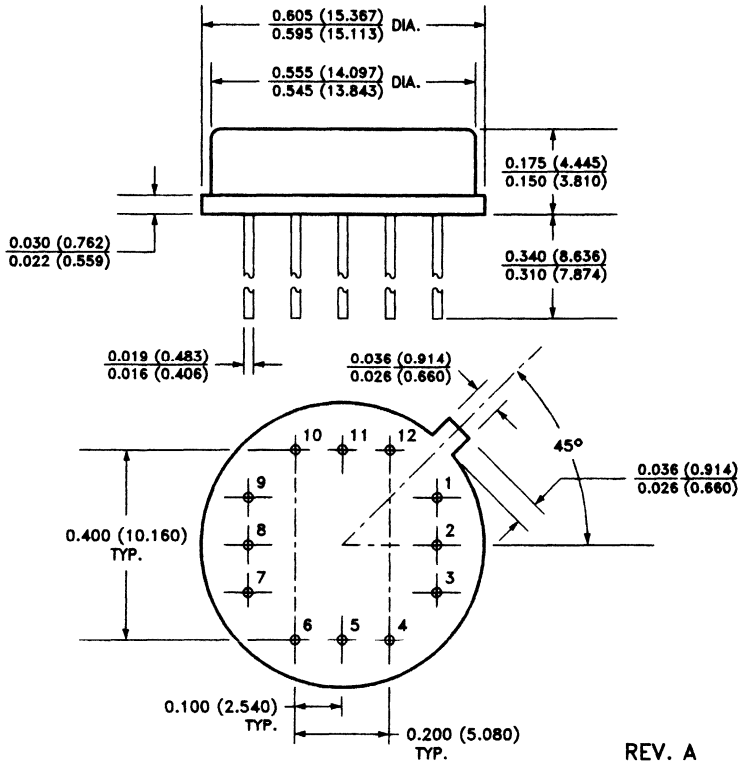
MDP0019 Rev. A
12-Lead TO-8 Metal Can Package
Pins 3 and 7 Grounded to Case

Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Gold or Hot Solder DIP



MDP0021 Rev. A
16-Lead CerDIP

Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

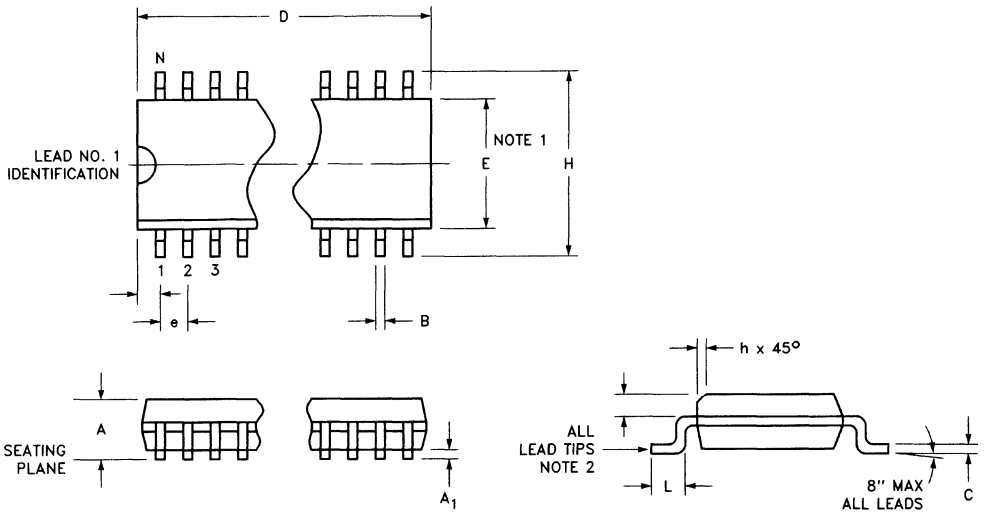


MDP0026 Rev. A

12-Lead TO-8 Metal Can-Short Lead

Commercial—Gold or Hot Solder DIP

Package Outlines



REV. A

Note 1. These dimensions do not include mold flash.

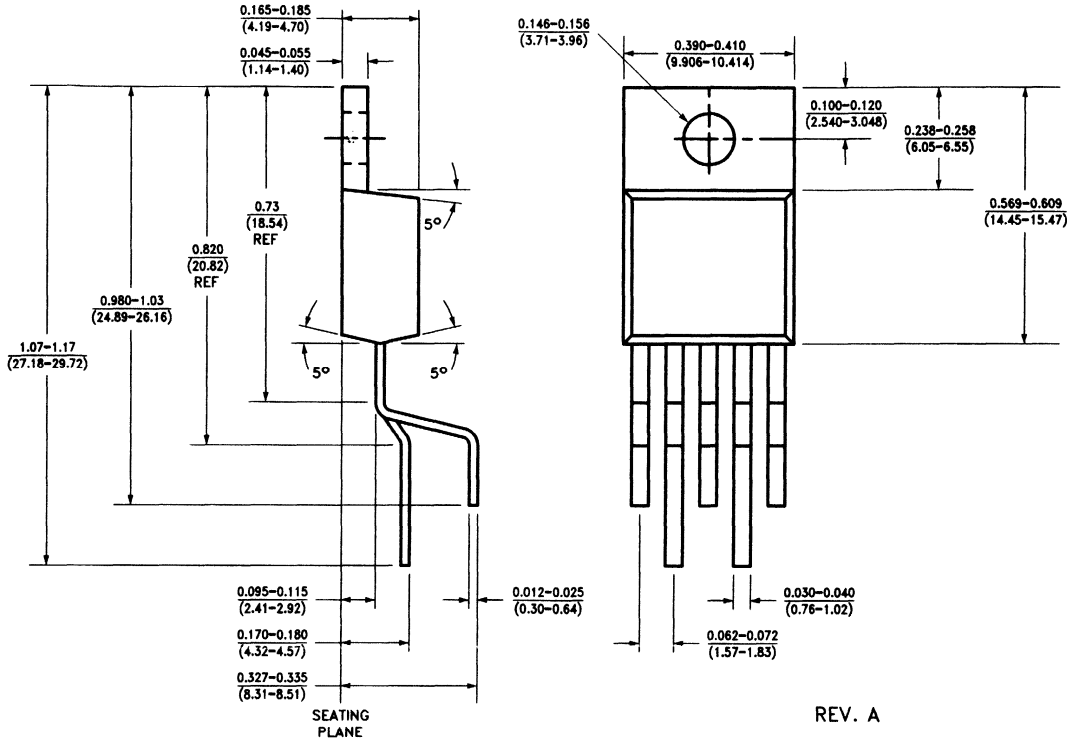
Note 2. Formed leads shall be planar with respect to one another within 0.004 inches at seating plane.

MDP0027 Rev. A

16 & 20-Lead Wide Body SO

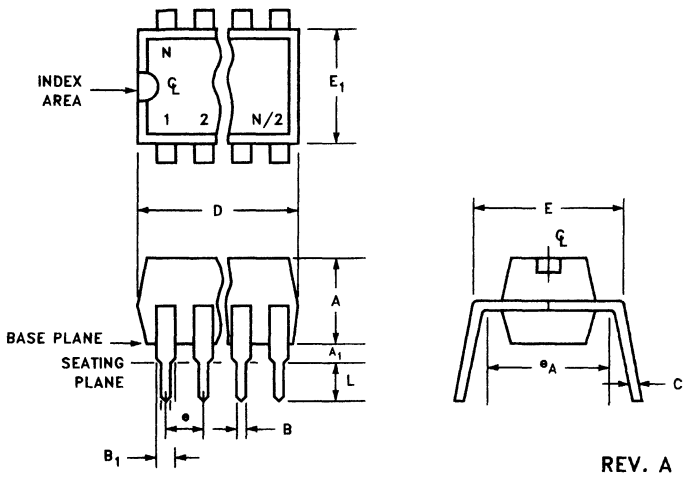
Lead Finish—Solder Plate

Symbol	Lead Count			
	20		16	
	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104
A_1	0.004	0.011	0.004	0.011
B	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012
D	0.498	0.510	0.397	0.430
E	0.291	0.299	0.291	0.299
e	0.050 Typ		0.050 Typ	
H	0.398	0.414	0.398	0.414
h	0.016 x 45°		0.016 x 45°	
L	0.016	0.398	0.016	0.398



MDP0028 Rev. A
5-Lead TO-220
Lead Finish—Solder Plate

Package Outlines



MDP0031 Rev. A
Plastic Package
Lead Finish—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020	0.016	0.020	0.015	0.021
B_1	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.350	0.385	0.750	0.770	0.745	0.755	0.925	1.045
E	0.290	0.310	0.300	0.320	0.300	0.325	0.300	0.320
E_1	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref	
L	0.130	0.150	0.115	0.150	0.125	0.150	0.130	0.150
N	8		14		16		20	